



## Concept, Realization and Results of the Mechanical and Electronics Integration Efforts for an Analog Hadronic Calorimeter

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### Abstract

Within the EUDET framework package JRA3, the concept of an analog hadronic calorimeter (AHCAL) for the International Linear Collider (ILC) based on scintillating tiles and silicon photomultipliers (SiPMs) has been developed. The concept has been validated by the realization of the three main deliverables of the HCAL work package, namely the mechanical, stainless steel absorber structure, the basic unit of the integrated inner detector electronics including the interface electronics to the data acquisition; and a suitable channel-wise calibration and gain monitoring system for the SiPMs based on LEDs.

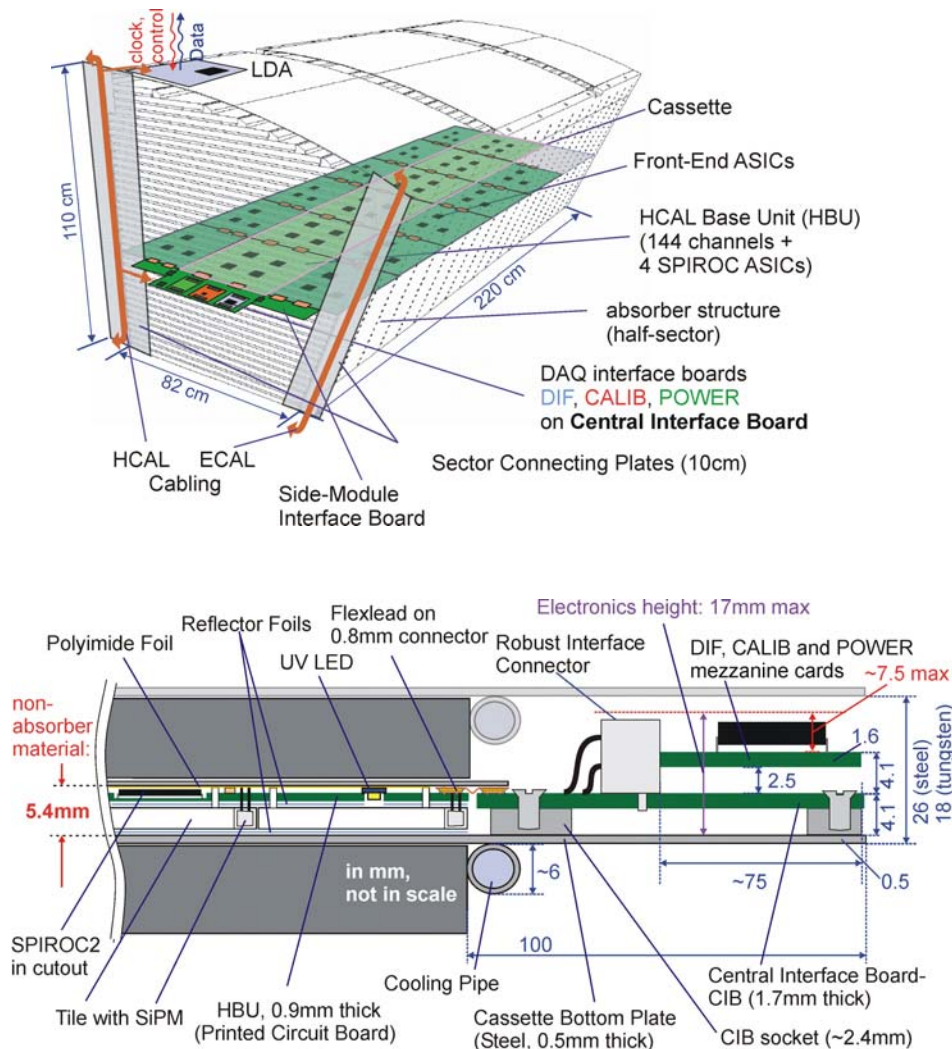
Measurement results obtained with the realized prototypes confirm the suitability of the developed concept for an application as ILC calorimeter, achieving a high granularity and compactness. The final generation of the modules will be used to set up a ~2500 channel prototype, addressing among others the important aspect of power-pulsing to avoid the warm-up of the calorimeter structure.

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# 1 AHCAL general concept

The envisaged AHCAL architecture is inspired by one variant of the ILD detector concept, but is very similar to those envisaged for SiD or CLIC. The aim is to build a detector with very high granularity to measure the details of hadron showers and finally distinguish between neutral and charged particles inside a jet by combining the energy information with the tracking information (particle flow concept). This requires a high integration level of the active inner detector electronics with a high pressure on the thickness. The required high transverse resolution and energy-measurement capability is achieved by the use of scintillating tiles that are read out by silicon photomultipliers (SiPMs). Important mechanical design aspects have been the reduction of dead space and a minimization of the barrel diameter, while maintaining a maximum of hadronic absorption length, in order to optimize the costs for the surrounding magnet. At the same time the architecture allows easy access to the electronics and service interfaces once the detector end-cap is opened.



*Fig. 1: Proposed integration concept for the inner detector electronics and the interface boards (-electronics) to the data acquisition (one layer shown, top). The cross section shows a height of 5.4mm of non-absorbing material for the inner detector part. The layer pitch results in 26mm with steel as absorber material (bottom), while the use of tungsten would lead to reduced pitch of 18mm.*

The huge number of almost 4 million detector channels inside the barrel requires the development of a reliable and at the same time simple assembly and commissioning procedure for the active detector units. The applicability of the proposed concept for an ILC calorimeter taking into account all of the high mechanical and electrical requirements has to be proved in different, partly realized prototype setups that are described in this report.

The general concept for the AHCAL barrel is shown in Fig. 1 [1, 2]. In the current extension it consists of 48 layers of absorber plates with embedded electronics and interface electronics at the absorber end-face. The electromagnetic calorimeter (ECAL) is placed inside the AHCAL, while the AHCAL is surrounded by the magnet coil. Inner and outer radius of the AHCAL is 1.8m and 2.8m, respectively. The cylindrical structure of the barrel is divided into 16 segments in  $\Phi$  and two parts with respect to the beam axis.

The inner detector electronics of one layer integrates the scintillation tiles with SiPMs [3], the front-end electronics for the SiPM readout together with a calibration system for gain monitoring. The electronics is subdivided into three slabs (Fig. 1, top), while each slab is further subdivided into six so called HCAL base units (HBUs). Since no active cooling is foreseen inside the detector volume, the warm-up of the detector has to be avoided by the application of very low-power electronics and switching off all possible parts of the electronics within the gaps of the ILC bunch-train structure (power-pulsing, resulting in  $25\mu\text{W}$  per channel). A typical detector layer of  $1 \times 2.20\text{m}^2$  size consists of 2592 detector channels (144 channels per HBU). As absorber plates the current concept foresees 17mm thick stainless steel plates per layer. With the steel cassette of the inner-detector electronics of 1mm-strength, the absorber thickness results to 18mm and the layer pitch to 26mm. But also tungsten as absorber material (10mm-plates) is currently being investigated in a testbeam effort, which would lead to a layer pitch of 18mm.

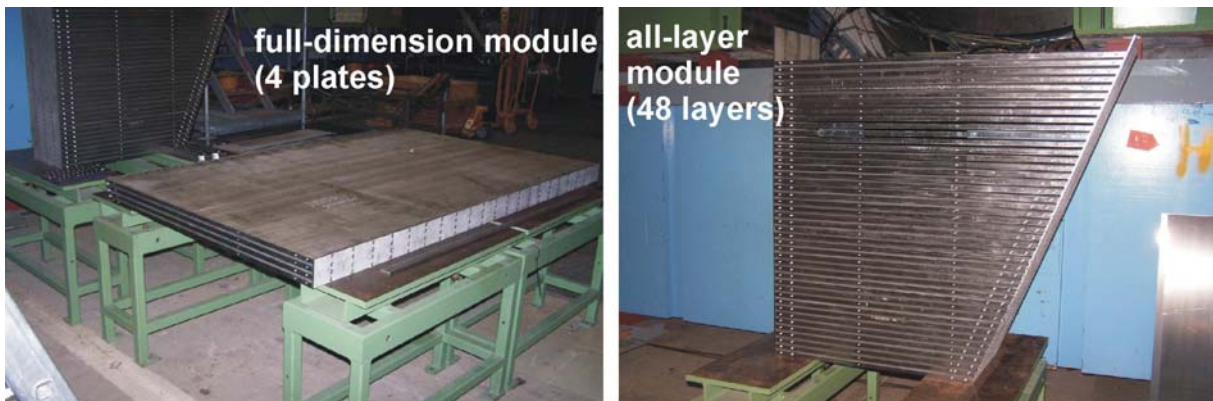
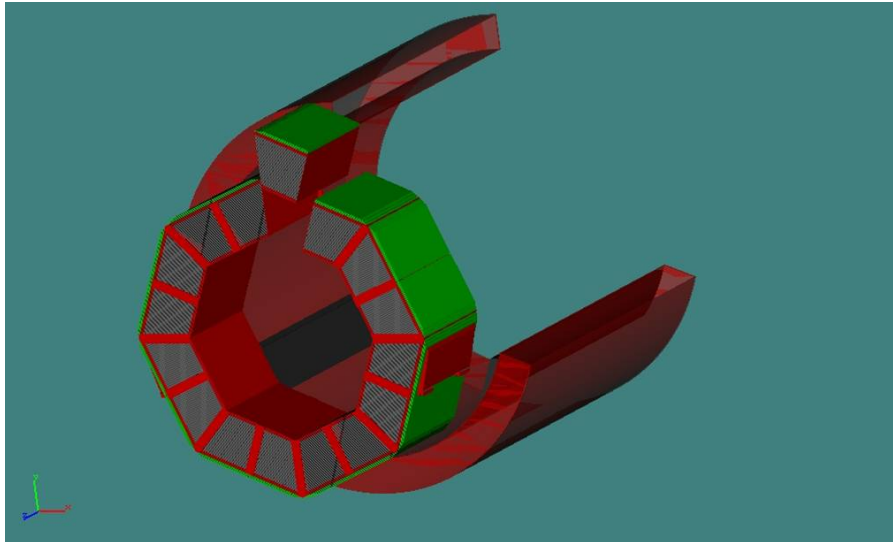
At the end of the absorber plates (detector end-face), the communication with the inner detector electronics, the power supply and operation of the calibration system is accomplished by the DAQ interface boards on the so called Central Interface Board (CIB). For stability reasons of the absorber structure, so called sector connecting plates will be connected to both end-face sides (cf. Fig 1). Therefore, each layer will be equipped with three slabs. During assembly, the side-slabs are inserted first and moved to the layer's sides, and finally the middle slab is inserted into the structure. The interface modules are connected to the middle slab. For the necessary differences of the layer widths, only the side-cassettes will change from layer to layer, while the more cost intensive central interface board stays the same for all layers. The space in front of the connecting plates is used for the necessary cabling trees for ECAL and HCAL sub-detectors.

The cross section of a detector layer is shown in Fig. 1 (bottom). By the placement of larger components of the HBU into cut-outs of the HBU PCB and the usage of ultra-thin interconnections, the height of non-absorbing material could be reduced to 5.4mm. At the end-face, the electronics height is limited to 18mm in order to allow steel and tungsten as material for the absorber plates.

## 2 Mechanical Integration

An in-depth analysis of the mechanical structure of the AHCAL, including not only the absorber plates and support structures but also the enclosed ECAL has been carried out. The proposed setup is shown in Fig. 2 (top) for the AHCAL half-barrel, which is subdivided into 16 segments in  $\Phi$  (one segment shown disassembled, c.f. Fig. 1, top) and surrounded by the magnet. Although the mass of the half-barrel comes to about 300 tons, the 16 segments are

supported only by 5mm thick side panels. The concept and its mechanical stability has been studied and optimized by detailed finite-element calculations. Deformations of the individual segments as well as of the overall barrel structure were validated, taking external support and the suspension of the ECAL into account. For the horizontal and vertical aligned segments, maximum deformations of individual absorber plates of 0.09mm and 0.35mm have been calculated, respectively [2, 4].



*Fig. 2: Conceptual view of one half of the AHCAL barrel, which is subdivided into 16 sectors (top) and surrounded by the magnet, and realized mechanical test modules for a horizontal setup with the full half-barrel length of 2.20m (bottom left), and for the vertical setup with 48 layers (bottom right).*

The developed mechanical concept has been validated by two prototypes, shown in Fig. 2 (bottom):

- a horizontal test structure (Fig. 2, bottom left) to establish the mechanical tolerances over the full area of an AHCAL half-barrel segment. Heat dissipation and installation procedures can be studied in full scale.
- a vertical test structure (Fig. 2, bottom right) to establish the mechanical stability under various orientations and stresses. The vertical test structure can be stacked in a flexible way, according to the envisaged analysis.

Both test structures can be equipped with the active-layer's electronics in order to test the full-scale performance of the electronics, especially the signal integrity, crosstalk behaviour and grounding strategies. The vertical test structure can be used for testbeam studies of the detector concept in various orientations with respect to the beam.

The optimization (minimization) of the gap between the absorber plates requires tight tolerances concerning the flatness of the absorber plates. The typical flatness of commercially available, rolled steel plates at sizes of  $1 \times 2.20 \text{m}^2$  is not better than 2-3mm. A flatness of below 1mm of commercial plates would increase the costs by a factor of 2 to 3. Since cost optimization is important for a realistic design concept, the commercial standard plates have been used for the test structures, which have been optimized before assembly in a so called roller-levelling process, by which flatness below 1mm could be achieved.

### 3 Electrical Integration

The electronics is subdivided into the inner detector part located between the absorber plates and the interface electronics at the end of the absorber plates that forms the interface to the global data acquisition (DAQ). Additionally, the AHCAL specific LED calibration system for the SiPMs (gain calibration and monitoring) with its control located on the interface electronics and its LEDs distributed in the inner detector is described. Finally, selected measurement results are presented that document the achieved performance of the proposed concept.

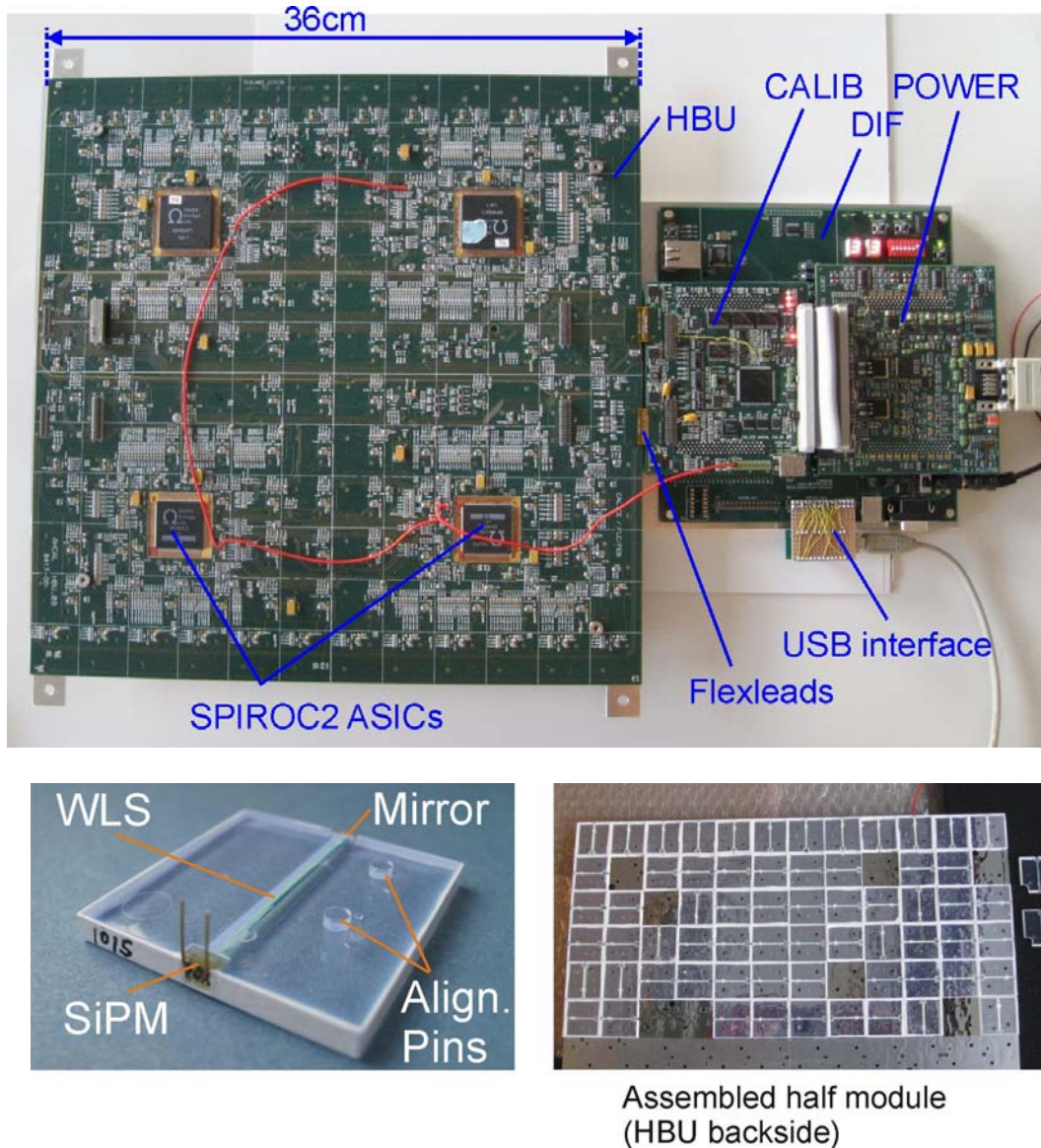
#### 3.1 Inner detector electronics (HBU)

In Fig. 3 the realized prototype electronics is shown. The electronics of the segment's layers will be divided into HCAL base units (HBUs) in order to keep the single modules at reasonable sizes concerning the production and handling. The HBU with a typical size of  $36 \times 36 \text{cm}^2$  integrates 144 scintillating tiles each with SiPMs together with the front-end electronics and the light calibration system. The analog signals of the SiPMs are read out by four front-end ASICs (compare Fig. 1) [5], while in the HBU prototype version, two of the 4 ASICs are from the older version SPIROC1 in a larger package (3.5mm high). In order to cover the full depth of 220cm of a segment's layer, 6 HBUs are connected together, forming an electrical layer unit within a layer cassette (slab). The HBU is a six-layer PCB with a total thickness of around  $850 \mu\text{m}$ , top- and bottom layer provides  $100 \Omega$ -differential impedance controlled routing.

In Fig. 3 (bottom) a scintillation tile with SiPM is shown (left) and the assembly of the tiles with SiPMs to the backside of the HBU PCB (Fig 3, bottom right). The tiles are mounted to the HBU PCB by so called alignment pins, which are plugged into respective holes of the HBU PCB. The current design proposes a straight wavelength-shifting fiber (WLS) and a mirror at the WLS end. Currently a tile size of  $3 \times 3 \text{cm}^2$  and a nominal distance between two tiles of  $100 \mu\text{m}$  is proposed. Different concepts for the scintillating tiles are under investigation, addressing the need for low-noise SiPMs, but also for an efficient light coupling between tile and SiPM. The detection uniformity of tiles without WLS, tiles with a lens structure on the top side that focus the light to an external SiPM, and for different positions of the SiPM within the tile are under investigation.

Before the tile assembly, an about  $100 \mu\text{m}$ -thick reflector foil 3M DF2000MA is placed between HBU and tiles in order to increase the light-detection efficiency. Special attention is needed during the assembly of the self-adhesive foil, which contains holes at the positions of

the scintillating tile's alignment and SiPM's signal pins and the UV-LEDs. Holes in the reflector foil and the HBU PCB that belong together have to be aligned with a high accuracy in the range of 0.1mm over the full HBU length of 36cm. Finally, a second reflector foil is placed below the tiles (cf. Fig. 1, bottom).



*Fig. 3: Prototype of the realized inner detector module HBU and the interface modules (top), one scintillating tile with SiPM (bottom left) and assembled tiles on the HBU backside (bottom right).*

In order to achieve the aimed detector module thickness of 5.4mm (c.f. Fig. 1 bottom), two strategies have been applied. At first, the HBU interconnection with the necessary high number of signals has been realized in a very small volume. Two types of flexleads have been realized for this purpose, one type for the signal-, the other type for the power-supply interconnection. The flexleads contain two 0.8mm thick 80-pin connectors (Kyocera 5801 series), a four-layer, rigid PCB below the connectors and a two-layer flexible part in between. A flexlead and its connection scheme is shown in Fig. 4 (top). In total, a thickness of 1.15mm above the HBU PCB can be achieved. The flexible part can compensate (distance)

misalignments between HBUs of about  $100\mu\text{m}$ . No significant signal distortions for the fast signals or voltage drops of the supply voltages have been observed.

The second strategy for limiting the HBU height is the placement of thick components into  $\sim 500\mu\text{m}$  deep cutouts of the HBU PCB, as shown for a SPIROC2 ASIC in Fig. 4 (bottom). The automatic soldering of the components in the cutouts is accomplished by a special solder-paste mask, which has electro-plated structuring at the positions of the cutouts.

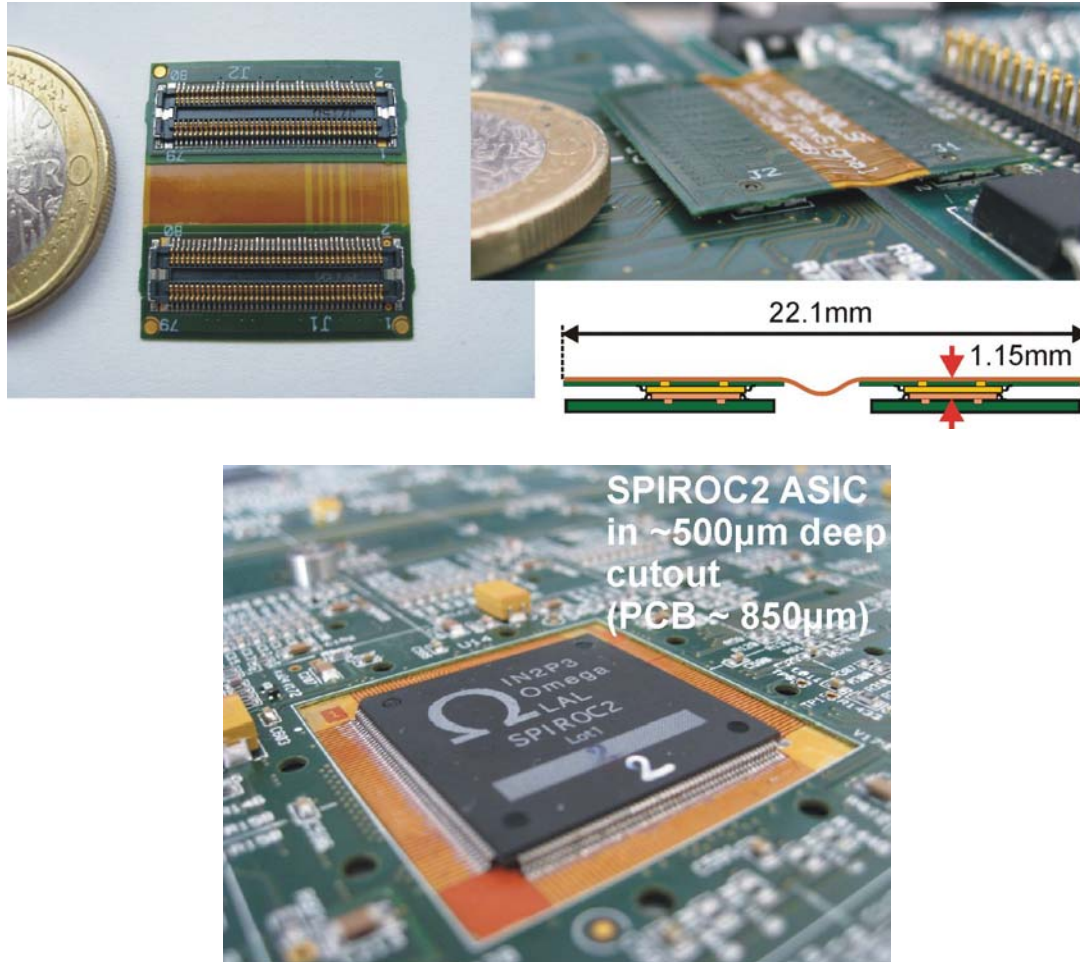


Fig. 4: Applied techniques for the height reduction of the inner-detector electronics: Usage of ultra-thin connectors (stacking height of  $0.8\text{mm}$ , top) and placement of the readout ASICs SPIROC2 into cutouts of the PCB (bottom).

### 3.2 Interface electronics and (preliminary) System Control

The DAQ interface boards DIF, CALIB and POWER form the interface between the inner detector electronics and the global data acquisition (via the CALICE DAQ module LDA [6]). In the final ILC setup, the interface boards are located at the endface of the absorber structure (c.f. Fig. 1). A liquid-based active cooling system with cooling pipes at the bottom sides of the cassettes prevents a heat-transfer from the interface electronics to the absorber structure (and to the inner detector electronics).

The prototype modules of the interface boards are depicted in Fig. 3 (top right). The main tasks of the boards are:

Module DIF is based in a first extension stage on a commercial SPARTAN3-1500 FPGA board in order to keep the development time of the prototype system small. The DIF is the only interface to the global data acquisition and therefore hosts both, the fast interface path to the front-end ASICs, e.g. for the data readout, and all slow-control tasks as for example detector configuration.

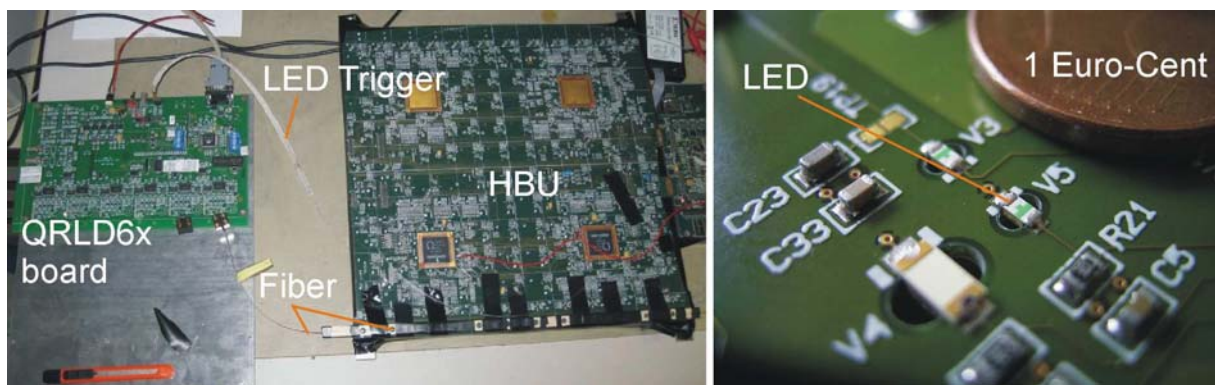
Module CALIB with a size of 11x10cm<sup>2</sup> is based on an ARM7 microcontroller and controls the light-calibration system for the SiPMs on the HBU. Additionally, module CALIB reads out the slow-control monitors for temperature, supply-voltages and -currents. For the calibration task, an analog bias voltage for the ultraviolet LEDs has to be generated in the range of +5V to +10V with a high stability and accuracy along with a differential fast LED trigger pulse with a width of about 40ns.

Module POWER with a size of 12.5x11cm<sup>2</sup> derives from three input voltages all necessary inner detector supply voltages, including the bias voltages for the SiPMs. It enables the power-cycling of the inner-detector electronics in the ILC bunch train scheme.

Since the CALICE DAQ chain [6] will be commissioned for the AHCAL not before spring 2011, the system control of the prototype system has been realized with Labview 8.6. The electrical interface to the DIF module is established via USB bus. The new developed Labview DAQ system allows full operation of the prototype system and can easily be modified for special debugging tests of the system.

### 3.3 LED calibration and monitoring systems

Due to the high sensitivity of the SiPMs' gains on temperature and bias-voltage changes, a dedicated calibration and gain monitoring system is crucial for a reliable definition of the detector response. Additionally, the saturation behaviour of the SiPMs should be determinable. Two approaches have been investigated and respective prototypes have been realized, both are based on the usage of blue or ultraviolet LEDs. The first approach is based on only few strong LEDs outside the inner detector, and a light distribution via optical fibers into the detector on top of and across the HBU PCBs [7, 8]. The light is coupled through notches in the fiber and holes in the PCB into the tiles. A uniformity of the light radiated by the notches has been measured to be constant within 20%.



*Fig. 5: Concepts of the in parallel investigated LED calibration systems: Fiber based system (left) and distributed LED system (right).*

In the second approach, one LED is assembled per tile (144 pieces per HBU), offering the advantage that no fibers are needed. The LED trigger can be distributed electrically and differentially. Measurements with a test system have shown no crosstalk from the LED trigger



to the SiPMs. The channel-to-channel uniformity is under test and will be optimized in the next integration step by a new LED driving circuit and a new type of LEDs.

In Fig. 5, the two principles of the two approaches are shown. The fiber-based system is operated from a six-channel LED driving board (QRLD6x), the fiber is routed from the QRLD6x board to the HBU, while the LED trigger is provided from the CALIB board to the QRLD6x board (Fig. 5, left). The integrated LED of the second approach (distributed LED system) is shown in Fig. 5 (right). With both systems, the characteristic single-pixel spectra of the SiPMs (c.f. Fig. 6, bottom right) could be reliably measured, in which the distance of the pixel-peaks are a measure for the channel's gain and can be used for gain monitoring.

The fiber-based approach has been tested together with the HBU and the interface modules in the DESY testbeam environment within the EUDET Transnational Access Program. Linearity and dynamic range of the approach are under investigation.

### 3.4 Measurement Results

Two systems of the prototype as shown in Fig. 3 (top) have been realized. After the initial tests and commissioning [9, 10], one system is now placed in the DESY electron testbeam facility and the other is still used in the laboratory for basic characterizations. Besides basic tests of the setups, the current tests have the main task to prove the suitability of the developed concept for a large-scale detector with around 2500 channels. Fig. 6 (top) shows the DESY electron testbeam setup with the HBU placed in a light-tight aluminum cassette. The beam of 2-6 GeV electrons traverses the scintillator tiles behaving close to a minimum ionizing particle (MIP). With the setup placed on a movable stage, the electron beam can be directed to any channel, allowing a MIP energy calibration of each channel. For the initial MIP tests, an external trigger has been provided, which originates from the coincidence of two 10cm-long scintillator counters in front of the setup. In Fig. 6 (bottom left), a typical MIP spectrum is shown, which has been measured with 50ns shaping time and 100fF preamplifier feedback capacitor (highest gain) of the SPIROC2 front-end ASIC. The single-pixel structure is distinguishable from pedestal up to far behind the most probable value of the MIP. With this setup all tiles have been scanned and the light-yield for a MIP signal was extracted. The average light yield for 26 channels resulted to be 8.04pixels/MIP with a spread of 0.9 pixels (standard deviation) as shown in Fig. 7 (left).

The integrated LED calibration system has been tested in both setups. For most of the channels characteristic single-pixel spectra as shown in Fig. 6 (right) were obtained, for which the maximum could be shifted within the histogram by adjusting the LED light output (LED bias VCALIB). The distances of the pixel-peaks in the histogram are a measure for the respective channel gains and will be used in dedicated LED calibration runs for gain monitoring. In the current prototype, the spread of the channels gain is rather large, the pixel distances vary between 17 and 55 ADC channels. Some of the channels show very small gains, for which a gain extraction from the single-pixel spectrum is not possible. A possible tuning of the operation voltage for these SiPMs may lead to a reasonable gain, but would also affect the light yield increasing the spread of this quantity.

Since in the ILC experiment no central trigger is provided to the front-end electronics, the SPIROC2 ASICs have self-triggering capability. The ASICs compare the analog input signal after amplification and fast-shaping with a predefined threshold and generate a trigger decision. The threshold can be adjusted by an internal 10-bit DAC, the output voltage of the

DAC is set within the SPIROC2 slow-control configuration. In a dedicated analysis, the threshold dependence on the DAC value has been determined for different detector channels. The resulting significant spread among the channels leads to the requirement of defining the trigger threshold individually per channel.

In order to determine the MIP detection efficiency in self triggering mode, the threshold has been set in a way that the ratio of the number of noise events and the number of MIP events is below  $10^{-4}$ . With this threshold cut applied, a MIP detection efficiency of 95% for the analyzed channels could be achieved as shown in Fig. 7 (right) [11].

The self-triggering mode of the system is the most important mode of operation with respect to an application for the ILC and therefore its performance has to be tested carefully.

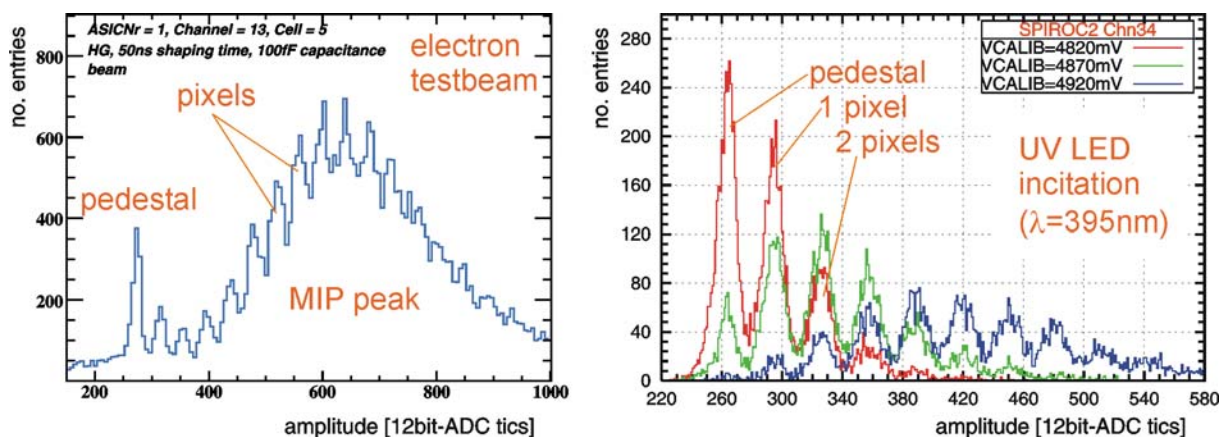
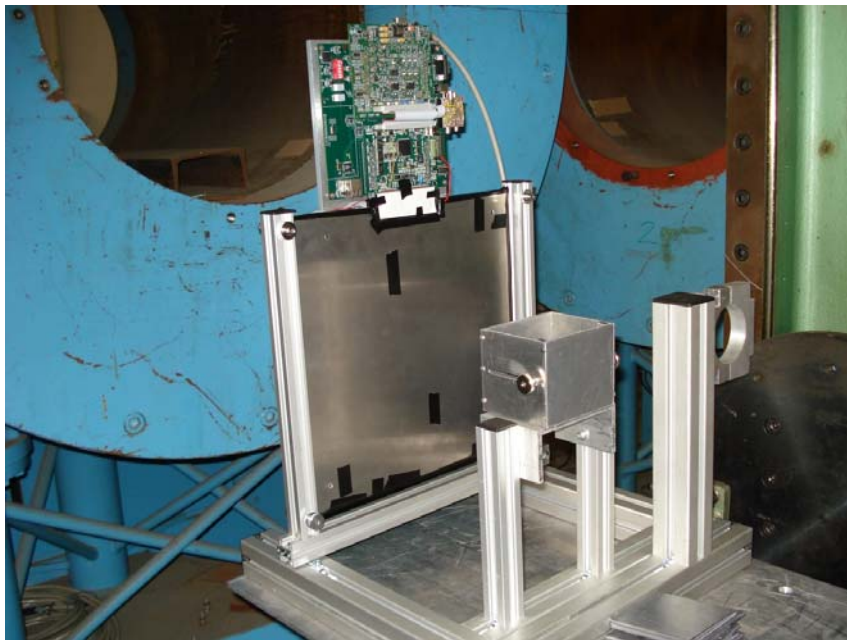


Fig. 6: Exemplary results from single-channel analysis with testbeam and the LED calibration system. Shown is the DESY electron testbeam setup (top), a single-tile response of one channel (bottom-left) and the characteristic single-pixel spectrum of one channel for three different LED-light amplitudes (bottom-right).

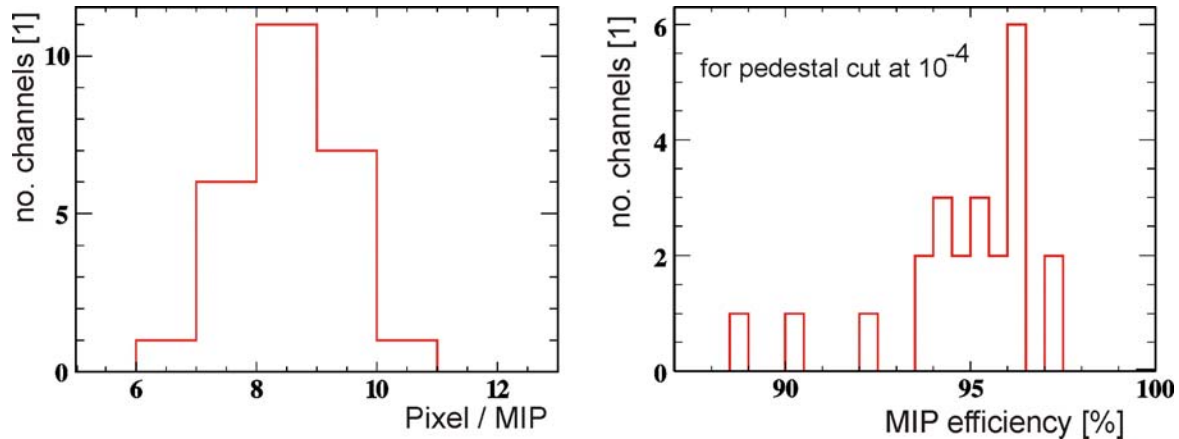


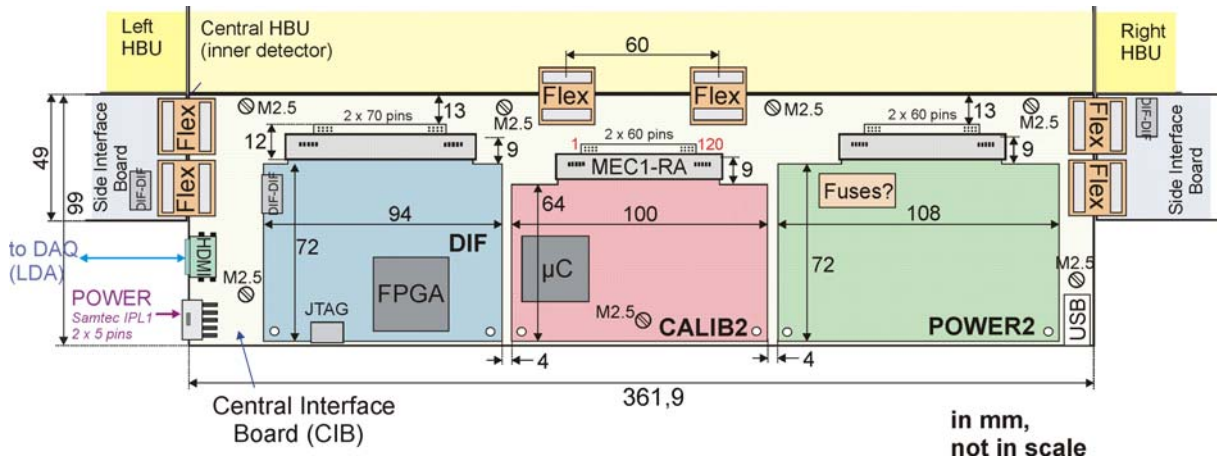
Fig. 7: Exemplary results from multi-channel analysis of the ASICs showing the distribution of the number of pixels firing for a MIP signal (left), and the achieved MIP efficiency of about 95% for the proposed pedestal cut in self-trigger mode (right).

## 4 Next Integration Step

In order to achieve the high integration level as shown in Fig. 1, the prototype modules shown in Fig. 3 have to be redesigned. The HBU redesign (HBU2) retains its general shape and outer dimensions of 36x36cm<sup>2</sup>, but the SPIROC ASICs are replaced by 4 ASICs of the newest generation SPIROC2b which are currently under test. Solder jumpers ensure, that older versions of the SPIROC can be assembled as well (SPIROC2 and -2a). The proposal for the final interface module's setup is shown in Fig. 8 (top) and in cross section in Fig. 1 (bottom). The commercial FPGA board is replaced by an own development (DIF, realization taken over by the National Illinois University NIU), still based on a SPARTAN3 FPGA in order to be design-consistent with the other CALICE DIF modules. The modules DIF, CALIB2 and POWER2 are realized as mezzanine modules on the so called central-interface board (CIB). All active electronics on the interface boards that might need an exchange due to a failure over time are connected with robust interface connectors to the CIBs (Samtec MEC1-RA type) in order to guarantee an easy replacement. The CIB has a typical width and length of 36cm and 10cm, respectively. While the CIB connects to the layer's middle slab, the Side Interface Boards (SIBs) connect to the side-slabs (c.f. Fig. 1). The SIBs only contain passive electronics and act similar to a cable. As interconnection between CIB and slab, CIB to SIBs and SIB to HBUs, the flexleads of the physics prototype can be used.

The status of the redesigns in November 2010 is depicted in Fig. 8 (bottom), while a photograph of the already finished modules CALIB2 and POWER2 is shown in Fig. 8 (middle). In the first test with a full slab, the SIBs are not needed and their production has been delayed in consequence.

With up to six of the HBU2s and the CIB with the mezzanine interface boards the layer performance using the mechanical prototype shown in Fig. 2 (left) can be tested, a tower module with only one HBU connected to the CIB in each of the 48 layers of the mechanical prototype of Fig. 2 (right) can be realized as well.



	DIF	CALIB2	POWER2	HBU2	CIB	SIB	Flexleads
concept dev., circuit design	X	X	X	X	X	X	X
schematic entry	X	X	X	X	X	X	X
Layout	X	X	X	X	X	X	X
Production	X	X	X	X	X	X	X

X = done    X = in preparation    X = to be done

Fig. 8: Dimensional sketch of the final integration step for the interface boards (top), and photographs of the already realized modules CALIB2 and POWER2 (middle) and status of the final redesigns (Nov. 2010, bottom).

## Acknowledgement

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