



## The Concept of LumiCal Readout Electronics

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### Abstract

The concept of readout electronics for LumiCal detector at ILC is discussed. The challenges of LumiCal readout are identified and the solutions are proposed together with the chosen overall architecture. Present work concentrate on front-end electronics and digital to analog conversion. Two considered front-end types and ADC design are discussed in details. First prototypes of electronics blocks have been designed and submitted to production.

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## 1 Introduction

The project of LumiCal readout electronics depends on several assumptions concerning detector architecture. At present development stage it is assumed that the LumiCal detector is built of 30 layers of  $300\ \mu\text{m}$  thick DC-coupled silicon sensors whereas each layer is divided into 48 azimuthal sectors. Each sector, with the inner radius of 8 cm and the outer of 35 cm, is segmented into 96 radial strips with a constant pitch. Such design results in a very wide range of sensor capacitance [1] which is connected to the front-end input.

The LumiCal readout should work in two modes: the physics mode and the calibration mode. In physics mode the detector should be sensitive to electromagnetic showers of high energy deposition (up to about 15 pC of ionized charge) in a single sensor. In calibration mode it should detect signals from relativistic muons, i.e. it should be able to register the minimum ionizing particles (1MIP  $\sim 4\text{fC}$ ). Because of very high expected occupancy the front-end electronics should resolve signals from particles in subsequent beam bunches and so should be very fast. The requirements on power dissipation of front-end electronics can be strongly relaxed if a total or partial power supply switching off is applied in the periods between the bunch trains.

The general concept of the readout electronics was outlined as shown in fig. 1. The main blocks in the signal flow are: front-end electronics, A/D conversion plus zero suppression and data concentrator with optical driver. The first two blocks of fig. 1, i.e. the front-end and the ADC need to be design as dedicated multichannel ASICs.

In the following the designs of these blocks are discussed and simulation results are presented. The data concentrator and optical driver block will be studied on further development stage. The prototype designs of discussed ASICs are done in the AMS  $0.35\mu\text{m}$  technology [2] through the Europractice service.

## 2 Front-end electronics

The front-end electronics detect signals from silicon sensor, amplify and shape them in order to obtain the required signal to noise ratio and finally sample and store their amplitudes. The memorized amplitudes are sent to the A/D conversion block. These operations are done in parallel in all channels of the front-end ASIC. The already mentioned features of the LumiCal set important constraints and requirements on the front-end electronics. They concern mainly the wide input capacitance range 10-100 pF per channel, the wide range of charge 2 fC-15 pC deposited in a single sensor and the high speed (pulse duration of about 360 ns). The low noise requirements are driven by calibration mode operation where the S/N ratio of about 10 should be sustained even for the largest sensor capacitance. At present stage the power dissipation per channel is constrained to 10 mW. In order to fulfil the requirements concerning low noise operation and wide range of input capacitance a charge sensitive preamplifier configuration was chosen. Two architectures of front-end using this configuration are currently under study: one with continuous pulse shaping and other based on Switched-Reset scheme

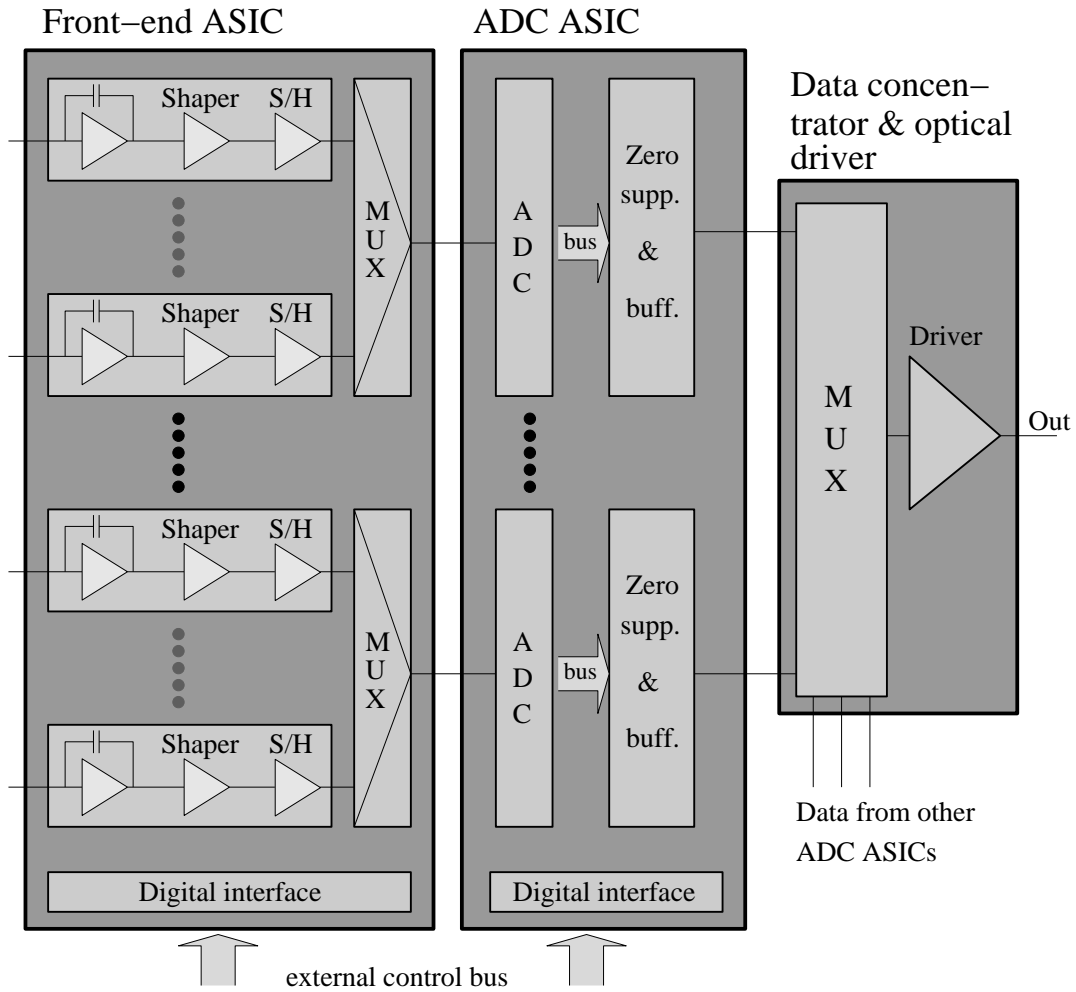


Figure 1: Block diagram of the LumiCal readout electronics

[3]. Both architectures with simulation results are discussed below. The sample and hold circuit (S/H) and the multiplexer circuit (MUX) are not discussed here since they have not been designed yet.

## 2.1 Front-end with continuous pulse shaping

Each front-end channel is built of the preamplifier, pole-zero cancellation circuit (PZC) and shaper as shown in fig. 2. The preamplifier integrates the signal from a sensor on the feedback capacitance. The PZC circuit is used in order to shorten a slow tail of the preamplifier response and in this way to improve high input rate performance. To optimize the signal to noise ratio and high speed performance the preamplifier and PZC is followed by a pseudo-gaussian shaper with a peaking time of about 70 ns.

To cover the amplitude range of input signals, from MIP in the calibration mode to more than 10 pC in the physics mode a variable gain scheme is implemented. The gain control is realized by the switches in the preamplifier and shaper feedback which allow

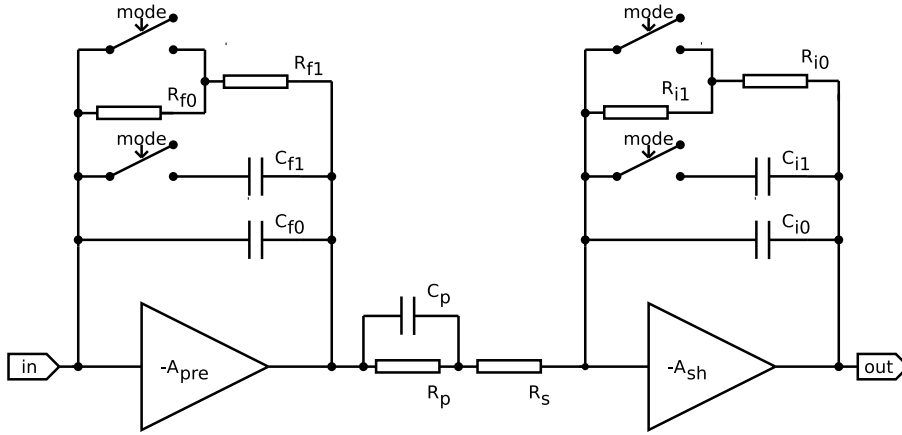


Figure 2: Schematic of preamplifier, PZC and shaper. Switches set to calibration mode.

to change between the low gain physics mode and the high gain calibration mode. As can be easily calculated the transfer function of the circuit in fig. 2 is equivalent to a standard CR-RC first order shaping. Both the preamplifier and shaper circuit are designed as folded cascodes with active loads, which are followed by buffers, as shown in fig. 3.

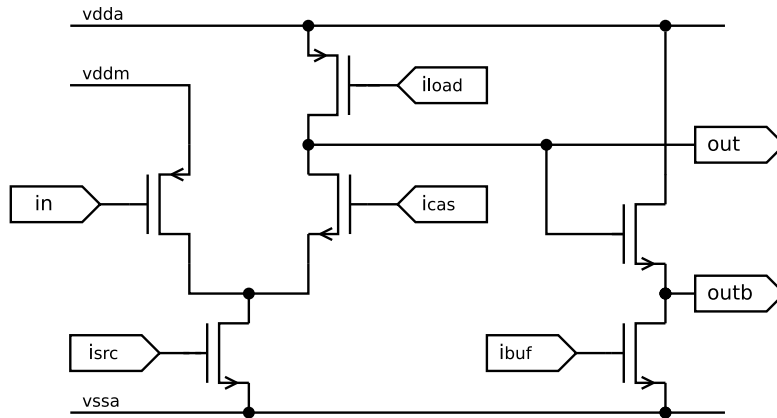


Figure 3: Schematic of folded cascode and buffer circuit

The front-end is designed as a multichannel ASIC. In order to match the sensor segmentation a single ASIC containing 32, 48 or 64 channels is considered. Such segmentation will allow for either 3 (2) ASICs per 96 radial strips in a single sector or 3 ASICs per pair of sectors. The final choice will depend mainly on power dissipation of a single ASIC and on the fanout scheme.

Simulations of the proposed front-end were done using Cadence [4] package with Hspice [5] and Spectre [4] simulators. The typical simulated responses for sensor capacitances

in the range 10-100 pF are shown in fig. 4 for the calibration mode (mode0) and for the physics mode (mode1).

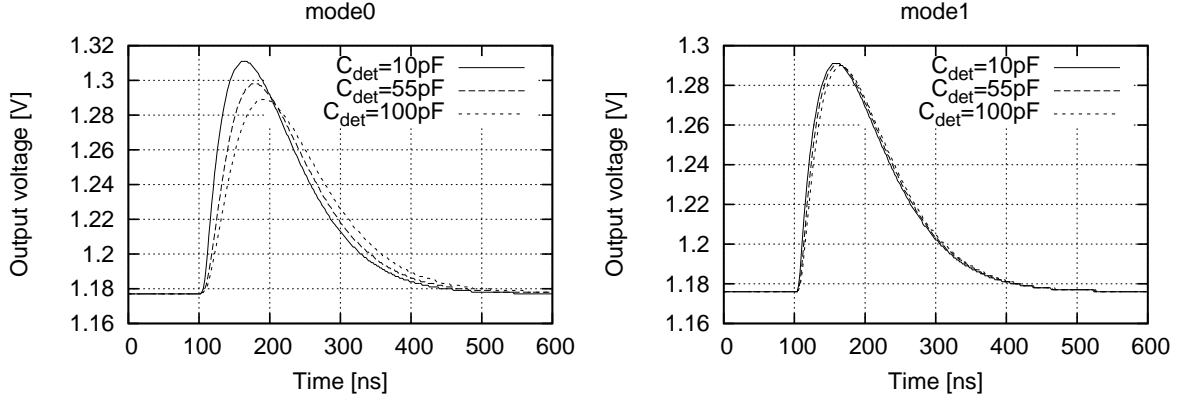


Figure 4: Example of shaper output in calibration mode for 10fC input charge (mode0) and in physics mode for 1pC input charge (mode1)

One can notice that in the calibration mode the amplitude and peaking time depend on the input capacitance. This happens because in the calibration mode, where the preamplifier's feedback capacitance  $C_f$  is small ( $\sim 400\text{fF}$ ), the ratio of the sensor capacitance  $C_{det}$  to the effective input capacitance  $C_{eff} \simeq A_{pre} \cdot C_f$  is not negligible since the preamplifier gain  $A_{pre}$  is below 1000 while the sensor capacitance reaches 100 pF. In such case some part of the charge is lost on the sensor capacitance and the preamplifier can not be considered as purely charge sensitive. In the physics mode, when the feedback capacitance is large ( $\sim 10\text{pF}$ ) the aforementioned ratio may be neglected and the preamplifier behaves as charge sensitive. This is seen in fig. 4 (mode1) where the dependence on input capacitance is hardly noticeable.

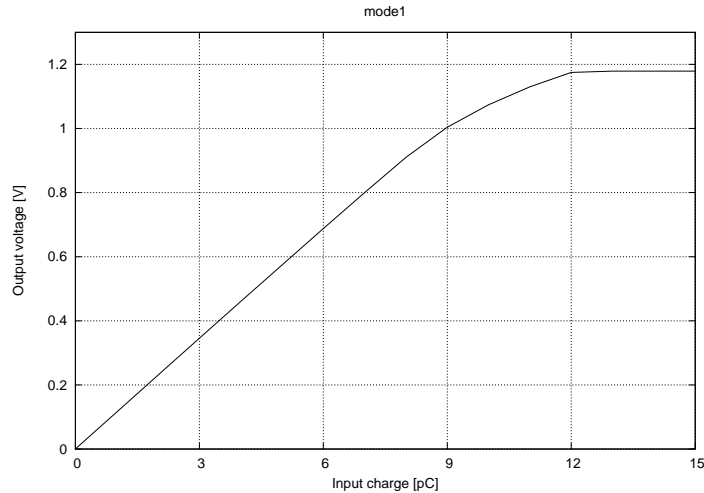


Figure 5: Example of front-end output amplitude vs input charge

In fig. 5 the amplitude of front-end response versus input charge is shown for the physics mode. The circuit is linear up to about 7 pC and saturates for higher input charges.

## 2.2 Switched-Reset front-end

The preamplifier with feedback reset instead of feedback resistance could be a very attractive configuration because such solution does not need a shaper and has large output dynamic range. For this reason a charge sensitive configuration equipped with reset switch as shown in fig. 6 is also investigated. The preamplifier is designed as a folded cascode. To allow variable gain operation different values of feedback capacitances are implemented. The calibration mode configuration is obtained using the smallest capacitance  $C_{f0}$ .

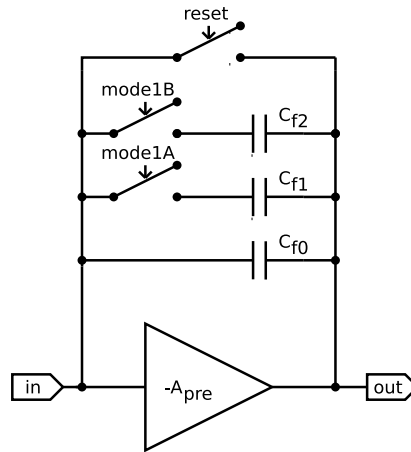


Figure 6: Schematic of switched-reset preamplifier

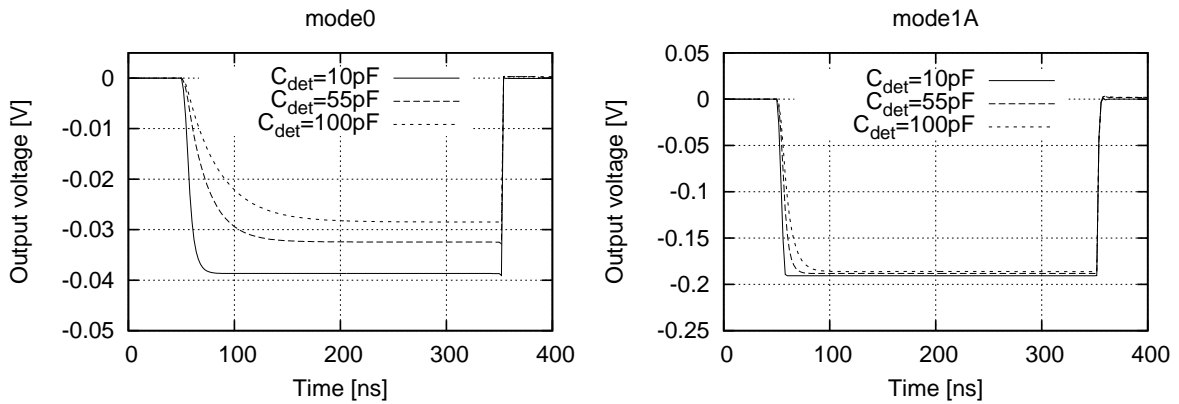


Figure 7: Example of Switched-Reset front-end output in the calibration mode for 10fC input charge (mode0) and in the physics mode for 1pC input charge (mode1)

Simulations of this configuration were performed for a wide range of input capacitances and input charges. The typical front-end responses for different sensor capacitances are shown in fig. 7 for the calibration mode (mode0) and for the physics mode (mode1). In all cases signal rise time is below 300 ns. Since the simulated reset time of the preamplifier never exceeds 40 ns the full cycle of pulse response and the reset can be performed between two bunches.

In fig. 8 the preamplifier amplitude versus input charge is shown for different gain settings. The mode0 case corresponds to the calibration mode while the other modes correspond to physics mode with different gain. In the calibration mode the circuit is linear up to about 300 fC and saturates for higher input charges. In the physics mode the linearity region can be extended to tens of pC by increasing the feedback capacitance. The circuit noise performance is currently under study.

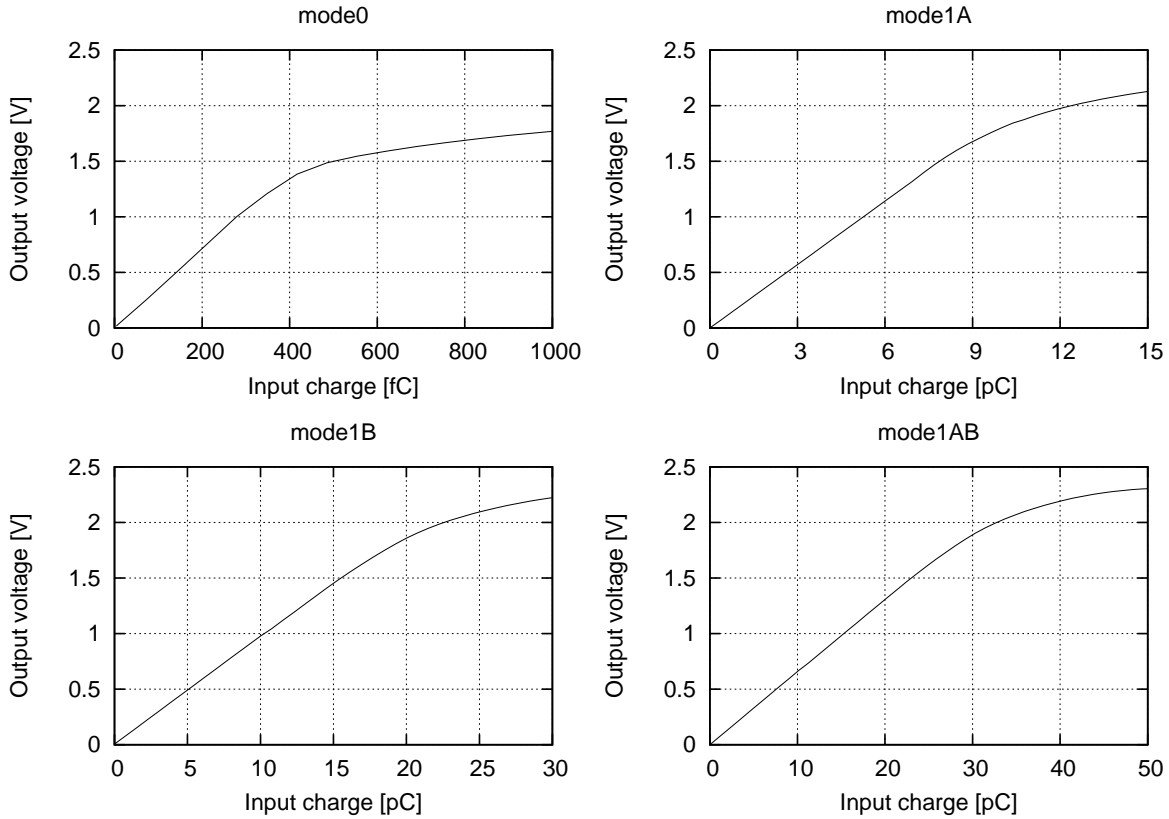


Figure 8: Example of front-end output amplitude vs input charge

### 3 Analog to Digital conversion

In the LumiCal detector the energy deposited in a sensor, detected and amplified in the front-end electronics, needs to be digitized and registered for further analysis. This is done in the ADC and zero suppression block. Simulations of LumiCal indicate that the

reconstruction procedure needs about 10 bit precision on the measurement of deposited energy. Considering the number of detector channels needed and the limitations on area and power, a best choice for the analog to digital conversion seems a dedicated multichannel ADC. To save the area a reasonable solution is to make one faster ADC for 8 channels of the front-end electronics. Since the LumiCal detector requires a sampling rate of about 3 MHz per channel an ADC should sample the data with at least 24 MHz rate. On the other hand a single 3 MHz ADC per each channel would be the simplest solution from the designer point of view. Both solutions are still under consideration. One of the most efficient architecture assuring a good compromise between the speed, area and power consumption is the pipeline ADC [6, 7], and this architecture was chosen for the LumiCal data conversion. Below, the design of main blocks of pipeline ADC is briefly described. The part of ADC block responsible for zero suppression is not discussed here since it is not implemented yet.

### 3.1 ADC Architecture

Pipeline ADC is built of several serially connected stages as shown in fig. 9. In the proposed solution a *1.5 bit stage* architecture was chosen because of its simplicity and immunity to the offsets in the comparator and amplifier circuits. Because single stage generates only three different values coded on 2 bits it is called *1.5 bit stage*. Each stage from fig. 9 generates 2 bits which are sent to digital correction block. In the correction block 18 output bits from 9 stages are combined together resulting in 10 bits of ADC output.

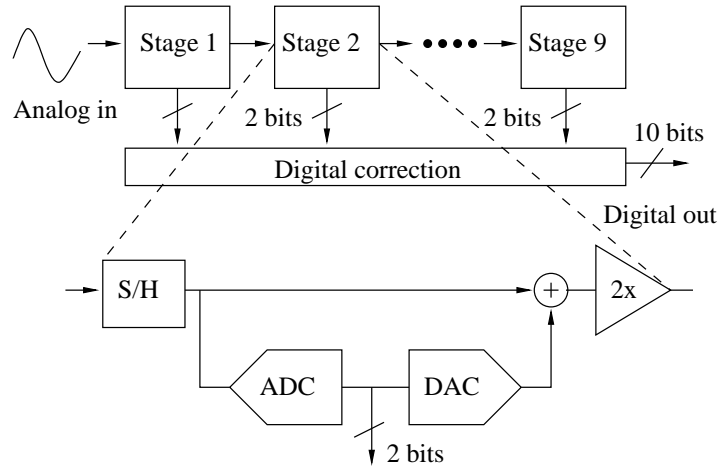


Figure 9: Pipeline ADC architecture

The block diagram of single stage is shown in fig. 10. Each *1.5 bit stage* consist of two comparators, two pairs of capacitors  $C_s$  and  $C_f$ , an operational transconductance amplifier, several switches and small digital logic circuit. To improve the ADC immunity to digital crosstalks and other disturbances a fully differential architecture is used. The operation of the stage is performed in two phases. In phase  $\varphi_1$  capacitors connected to



ground through switch  $S_1$  (in reality to common voltage, ground is used in description only for simplicity) are charged to voltages  $V_{i\pm}$ . In phase  $\varphi_2$  the switches  $S_2$  and  $S_3$  change positions and  $S_1$  is open. The  $C_f$  are now in the amplifier feedback while the  $C_s$  are connected to DAC reference voltages ( $\pm V_{ref}$  or 0 depending on comparators decision). In the *1.5 bit stage* architecture  $C_f = C_s$  is chosen to obtain a gain of two in the transfer function.

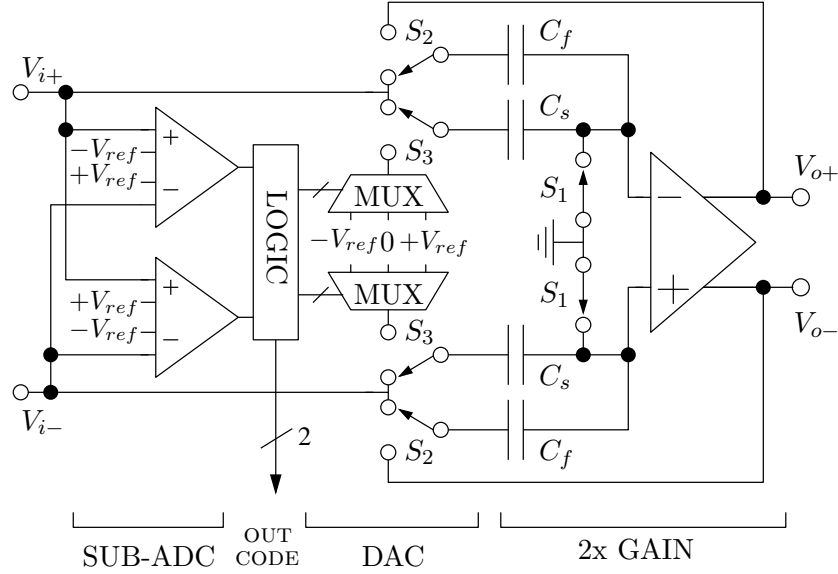


Figure 10: Simplified schematic of a 1.5 bit stage. Switches set to  $\varphi_1$  phase.

### 3.2 Simulation results

The critical block of a pipeline ADC is a fully differential amplifier. A telescopic cascode amplifier configuration is used since it represents the most efficient solution with respect to speed vs power. In order to obtain high enough gain (of about 80 dB) required for 10 bit resolution a gain boosting amplifiers are used in both upper and lower cascode branches [8, 9]. Since a *1.5 bit* architecture leaves very relaxed requirements on the comparators ( $\sim 100\text{mV}$  threshold precision) a simple dynamic latch architecture was chosen [6]. For the present prototype all reference voltages are assumed to be applied externally. An example of the simulated output of a single 1.5 bit stage for a staircase input is shown in fig. 11. The stable output level value corresponds to a sum of the input signal and DAC voltage multiplied by two.

## 4 Conclusion

To summarize it should be stressed that the work on the LumiCal readout electronics has just started. The configuration of the core readout circuits i.e. the front-end and the ADC are designed and simulated and first prototypes are submitted. In the

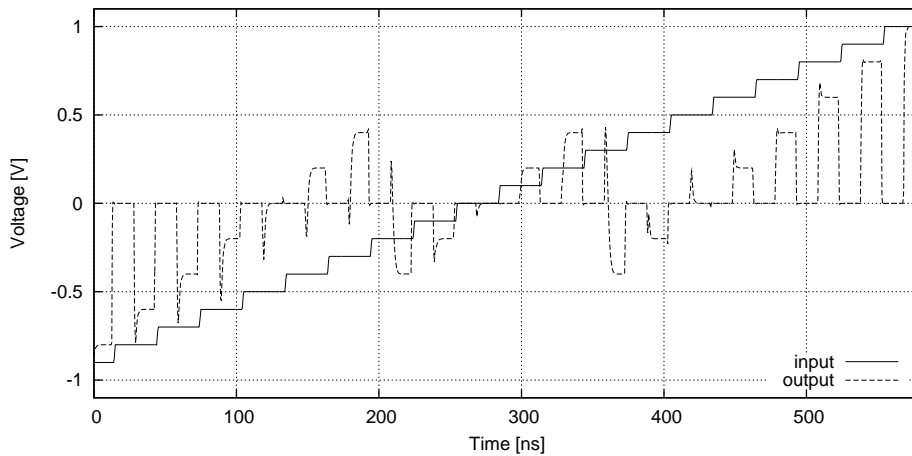


Figure 11: Example of a single 1.5 bit stage output for a staircase function

next evaluation stage the sub-circuits not yet designed like sample and hold (S/H) or multiplexer (MUX) will be integrated and prototyped as well. Then the integration of multichannel ASICs with all channels and full functionality comprising all necessary controls, DACs, zero suppression etc. will be added. More studies are needed to draw the detailed architecture and the implementation of the Data Concentrator and Optical Driver blocks.

## Acknowledgement

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