



JRA3 Calorimeter Conceptual Report

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Abstract

We present our present understanding of the conceptual design for a realistic calorimeter prototypes and infrastructure to be developed in the framework of the JRA3 ECAL task of the EUDET infrastructure initiative for ILC detector R&D.

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1 Electromagnetic Calorimeter (ECAL)

1.1 Introduction

Beyond the validation of the physics, the silicon tungsten electromagnetic calorimeter R&D program shall include a technologic prototype. That state-of-the-art detector allowing imaging calorimetry involves ambitious technological R&D that need to be validated in a demonstrator.

As described below, the thickness of the active layer of the detector as to be minimized to optimize the moliere radius and the whole ILC detector cost. Achieving a compact calorimeter involves also many constraints on the mechanics.

The main point of that EUDET ECAL demonstrator is to validate the technologic assumptions necessary to the full detector construction.

The full detector will embed around 82 million channels and 112 tons of tungsten. It is shown on Figure 1.1

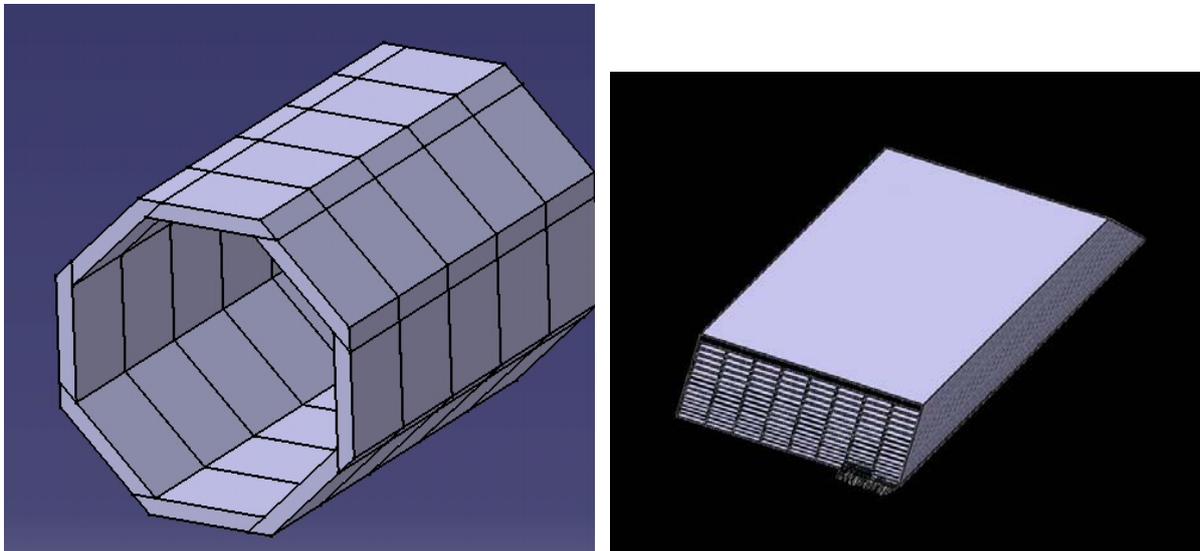


Figure 1.1 - Full ECAL barrel / One module of the full ECAL barrel

1.2 ECAL demonstrator description

The aim of the EUDET ECAL demonstrator is to validate the feasibility of a full detector. A strong condition is therefore to have a life-size demonstrator. The final ECAL barrel will be a 7*15 alveolar carbon-fiber-wrapped tungsten structure. The length of the structure will be around 1.5m.

To validate the long alveolar structure, it is necessary for the demonstrator to be as long as the final module. The validation of the carbon fiber alveolas abutment involves at least a 3-alveola wide structure. To allow that demonstrator to take physics run, a 24 radiation length thickness structure has been chosen with 30 detection layers, as in the final detector parameters.

The final design of the EUDET ECAL demonstrator is shown in Figure 1.2.

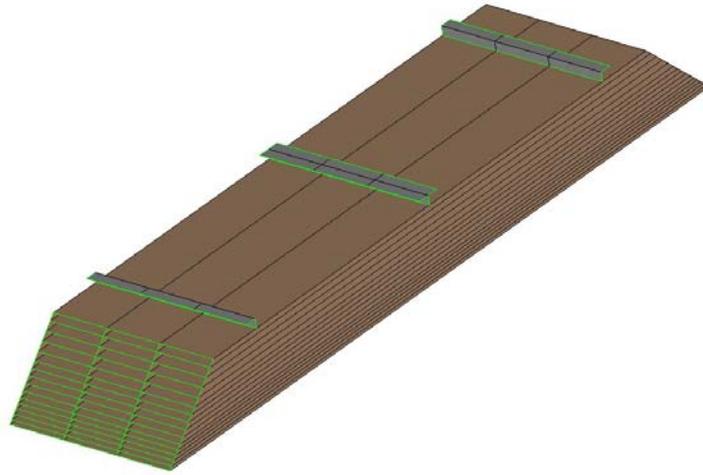


Figure 1.2 - EUDET ECAL demonstrator mechanical structure

The structure is full-length and full height to be as representative as possible of the final detector. The number of alveolas has been set to the minimum value of 3 to fit the cost constraint. That structure embeds 500kg of tungsten and 1.3 million channels if fully equipped.

Detector slabs will be slid in the alveolas.

1.3 ECAL demonstrator electronics

The active layers will be equipped with PIN diodes matrix wafers. The size of a pixel has been optimised. A $5 \times 5 \text{mm}^2$ pad size has been shown as a good trade-off between front-end power consumption and resolution. The number of channel for each active layer is therefore around 7200 per alveola. To read out such a huge number of channel with calorimetry dynamic range and linearity it is necessary to embed the front-end electronic in the detector instead of driving as many lines as the number of channel to the edge of the detector.

When the embedded electronic assumption is done, constraints on the electronic are set. The consumption per channel has to reach an unprecedented level to avoid any active cooling which would kill the molier radius and the compactness of the detector. Having the electronic embedded involves also a good immunity of the electronic to very high energy electromagnetic shower.

In order to keep the cost low, the demonstrator is not due to be fully equipped. A long slab will be built to validate the data flow through the front end ASIC daisy chain and a tower will be equipped to do physics with this new ECAL prototype featuring power pulsing and embedded front-end ASIC.

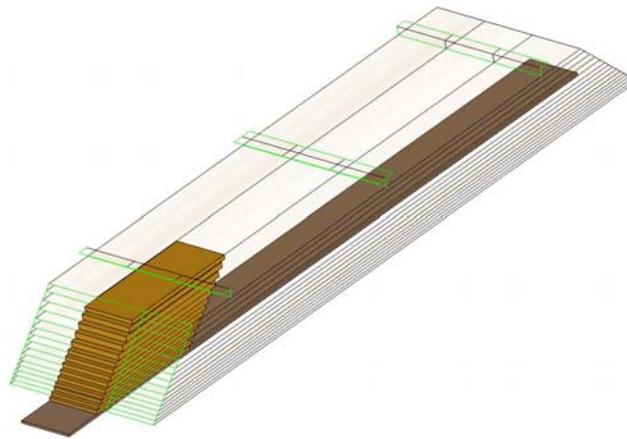


Figure 1.3 - EUDET demonstrator detector equipment

1.4 Slab design

To optimize compactness, the slab structure that slides in the alveolar structure embed on layer of tungsten and two layers of detection. One slab is therefore assembled around a carbon-wrapped tungsten H-structure core. The active layer is made of a PCB hosting the wafer on one side and the front-end electronic on the other side. The wafers are glued to the wafer with a conductive epoxy glue. The naked die of the front-end electronic is directly bonded on the back of the PCB. Using such a new process of chip-on-board saves 1mm per layer on the thickness.

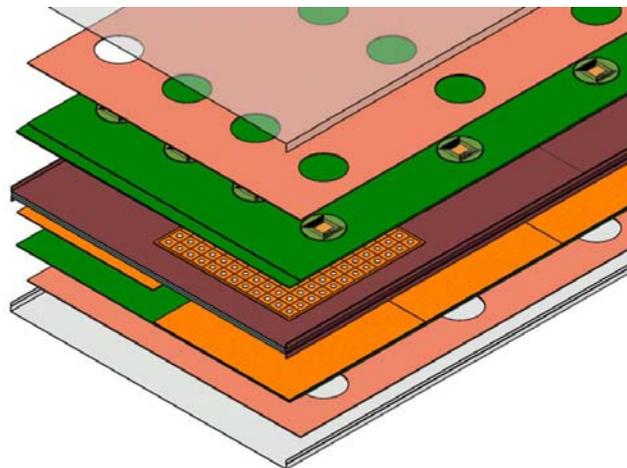


Figure 1.4 - Slab exploded view

1.5 PCB design

The final length of a detector slab is 1.5m. The industry is not capable of producing such long PCB. The chip on board bonding yield does not allow such long PCB. A 1.5m long PCB involves between 100 and 200 chips per board. Assuming – obviously - that every bonded chip has to be good, the yield of the PCB assembling would have been 200 times lower than the yield of one bonding. Last but not least, the bonding of such long PCB cannot be done by industry.

All these point have conducted to the design of stitchable small PCB. To avoid loosing thickness with connection between PCB, an innovative step structure has been designed. The PCB can then be glued one to another with the same process than the wafers are glued to each small PCB. This is done without increasing the thickness of the PCB.

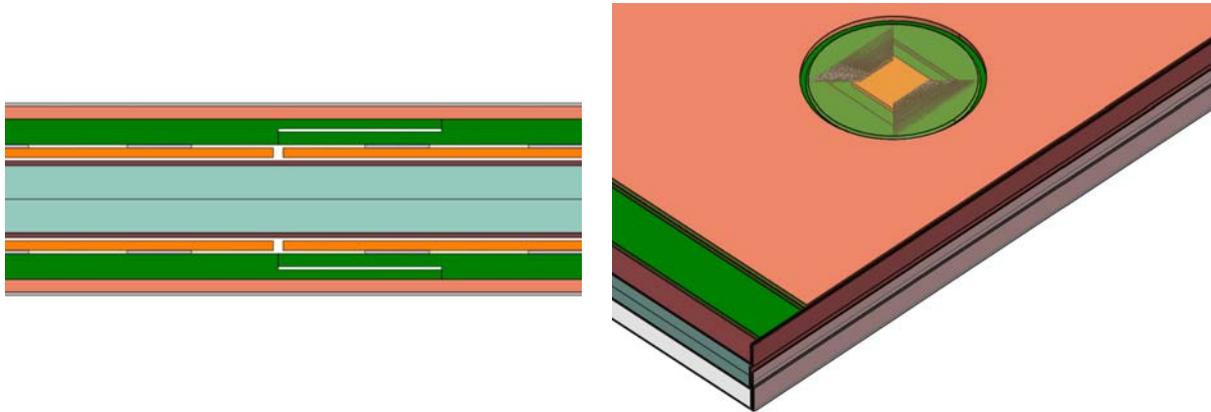


Figure 1.5 - Slab view - PCB stitching / Chip on board

2 Hadron Calorimeter (HCAL)

2.1 Introduction

The calorimeter system of a future detector at the International Linear Collider (ILC) has to measure the energy of hadronic jets with unprecedented precision. In currently proposed detector concepts this is achieved using very compact and finely segmented structures. With the advent of novel silicon-based high-gain photo-sensors (SiPMs), high granularities can be realized with scintillator as active medium.

This technology is presently being used for the very first time in an 8000 channel prototype of a steel scintillator hadron calorimeter (HCAL) currently exposed to test beams at CERN in the framework of the world-wide CALICE R&D collaboration. The test beam experiment is set up to validate the high granularity approach and the photo-sensor technology in principle, but technical solutions which can be scaled up to a full collider detector system are not yet addressed.

The goal of the HCAL task within the EUDET joint research activity JRA3 is to develop a realistic mechanical structure and calibration concept, which together with the electronics and DAQ activities provide a scalable detector architecture for embedding upcoming new sensor technologies.

2.2 Present HCAL test beam prototype and experience

The aim of the test beam experiment is to collect large amounts of data with high special resolution in order to validate the simulations and demonstrate in principle that the claimed detector performance can be achieved. At the same time it serves to identify critical operational aspects of the new technology and to optimize calibration and monitoring procedures. It thus provides important input for the next generation technical prototype.



Figure 2.1: Scintillator tile layer (left), complete module with front end electronics (right).

Given the proof-of-principle purpose of the test beam prototype, its design is rather conservative, apart from the SiPM. It consists of 38 layers with 216 or 145 scintillator tiles individually read out by SiPMs produced by Russian industry. A number of features cannot be translated into a full detector concept and need to be re-addressed in this task:

- The very front end (VFE) electronics components are mounted outside the detector volume. In order to minimize dead space and signal path lengths, the VFE ASIC chips need to be integrated into the layer structure.
- The electronic characteristics of the analogue part of the VFE are not optimized for the fast SiPM signal; this is being addressed by the next generation ASICs being developed in the FEE task.
- The prototype has a very versatile and redundant calibration system, in order to ensure reliable data taking with a not yet proven sensor technology, and to allow for comparison of different calibration and monitoring concepts. For a full-scale system, it is too complicated and must be simplified.
- The thickness of the readout layer and the scintillator itself has not yet been minimized. The overall HCAL thickness has significant cost implications, as it has to fit into the bore of the superconducting solenoid of the ILC detector.
- The assembly is quite labour-consuming due to the signal routing via micro-coaxial cables. Printed circuit board technologies amenable at large scale mass production need to be applied instead.

On the other hand, there exists no precedence for a scintillator based calorimeter with integrated light readout sensors and electronics from which the design could be extrapolated. A realistic structure must be invented and built in order to validate the concept from the technological side.

The test beam prototype was successfully commissioned at CERN in 2006. Detector operation was very robust and stable. With up-times well above 90% about 60 million electron and hadron induced events were collected. An example which demonstrates the excellent imaging capabilities of the device is shown below.

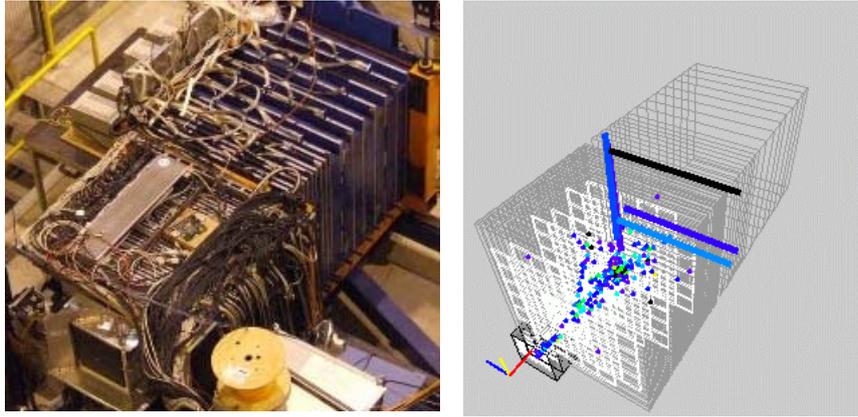


Figure 2.2: Test beam set-up at CERN, consisting of electromagnetic and hadronic calorimeters plus tail catcher (left), online event display with a 10 GeV pion shower (right)..

The test beam set-up has followed the same unified readout electronics concept for electromagnetic (ECAL) and hadronic calorimeter which is also underlying the FEE and DAQ tasks of this JRA. This approach reduced the system integration effort to an absolute minimum and resulted in a combined and unified calorimeter system from the very beginning. This experience has lent strong support to the approach for future test environments and the final detector system.

The built-in redundancy of the test beam calibration and readout system allows several different monitoring concepts to be applied and cross-checked. Feedback from the ongoing analysis will be crucial to identify the most efficient strategy. However, the SiPM auto-calibration capabilities – resulting from the clear separation of individual photo-electrons - have been of so manifold use, from production quality control to commissioning diagnostics, linearity correction and temperature monitoring, that they should be preserved in future design evolutions in any case. This directly translates into performance requirements for the SiPM as well as for the very front end electronics.

SiPMs mass production is still a pioneering endeavour. It turned out that the electronics had to accommodate a certain spread of the input signal characteristics. The dark rate was a carefully tuned compromise between detector occupancy and the production yield. In practice the noise hit occupancy of the detector was dominated by the SiPM dark current and with about 10^{-3} just small enough to not deteriorate the shower structure pattern recognition. A further reduction by an order of magnitude would be desirable for the unambiguous identification of neutron induced signals, and to gain some safety margins for the adjustment of operation parameters.

2.3 HCAL architecture and system integration

For the detector layout we presently limit our considerations to the barrel section. As an example, the subdivision into modules foreseen in the large detector concept (LDC), is shown in the figure below. The hexagonal structure ensures good filling of the volume with absorber material. The longitudinal division into only two half-barrels is preferred with respect to a larger number of barrel “rings” because of the reduced amount of dead material and the easier accessibility of readout electronics from the two end faces of the barrel sections. In this design the total thickness of the HCAL is about 1.1m, the modules are about 2.2m long. The basics sampling structure consists of 2mm thick stainless steel absorber plates interleaved by readout

gaps of about 7mm width to accommodate the active layers: the scintillator tiles, reflector foils, printed circuit boards and VFE ASICs.

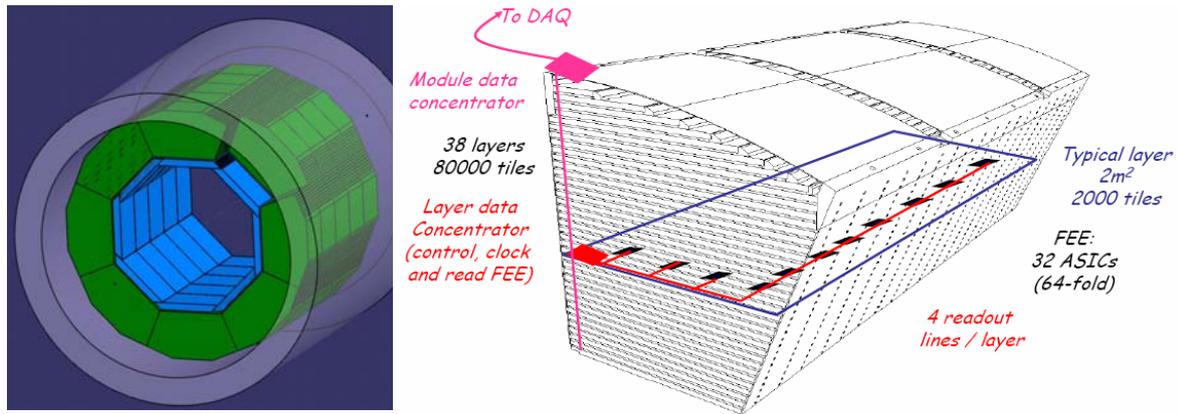


Figure 2.3: Barrel section of the electromagnetic and hadronic calorimeter in the large detector concept (left), a half-octant HCAL sector (right)

We consider these dimensions as indicative. The prototype structure must not exactly reproduce the dimensions of the final detector, but it should demonstrate that technical solutions exist for a number of issues:

- The structure must be compact, have minimal dead regions (cracks), be rigid and self-supporting in any of the required orientations and respect the tolerances for easy insertion of active layers. It should be strong enough to support the heavy silicon tungsten ECAL modules mounted on the first absorber layer.
- Electrical readout and control signals as well as optical calibration signals and electrical power must be routed reliably over the up to two metre long active layers, thereby respecting constraints from assembly procedures as well as requirements for maintenance accessibility.
- The connectivity issues at the barrel end (layer-to-layer connection and communication with off-detector components) can be realized within the very limited spatial constraints at the barrel end face, thereby incorporating readout and calibration systems, power supply and cooling.
- Conditions for heat dissipation must be realistic.

For the scintillator transverse segmentation we assume that square tiles with a size of 3cm as optimized for the test beam prototype are also typical for the full detector. More recent particle flow studies support this: the improvements with 1cm tiles are too small to justify a 10-fold increase in channel count, whereas 10cm tiles are too large to resolve shower substructure. About 1000 to 2000 tiles per layer should thus form a realistic starting point for the expected channel density.

For the electronics architecture we again follow the ECAL concept. The VFE ASICs include the analogue stage (pre-amplifier and shaper, sample-and-hold circuit) and the ADC. The front end electronics which controls the VFE and communicates with off-detector components – see DAQ section – will be located at the barrel end. We foresee two stages of concentration, first layer wise, then module wise. The FE must also control calibration electronics and power cycling with respective components integrated on the layer FE board.

2.4 Active layer

The barrel HCAL will contain about 2.5 million scintillator tiles on a surface of about 2500 m², the corresponding numbers for the two end caps together are about the same. The active

layer structure must be compact and amenable at mass production techniques. The issues to be addressed are

- The coupling between the scintillator and the photo-sensor is a research field in its own, driven by advances in the sensor technology. Important simplifications are possible with improved SiPM performance. We aim at 3mm scintillator thickness and an active layer design which leaves more than one option open for the choice of the photo-sensor and its coupling to the tiles. For reasons of optical coupling stability and motivated by quality control chain considerations we regard the scintillator photo sensor system as a unit. This approach was successful in the test beam prototype.
- The tile positions must be controlled in a manner which accommodate mechanical tolerances resulting from cost-effective tile production techniques but minimize inefficient regions and still respect the precision requirements of the printed circuit board with its dense electrical signal lines connected to the SiPM.

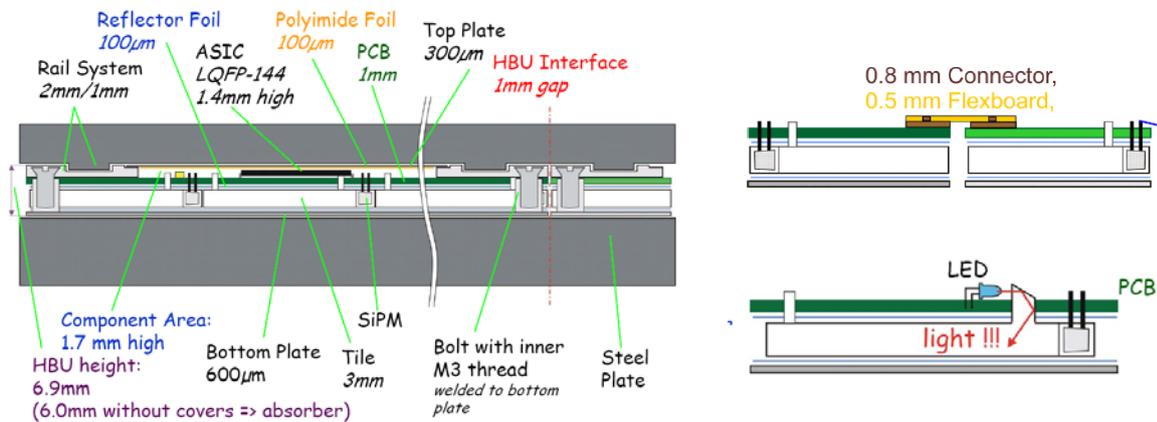


Figure 2.4: Active layer cross section, with details for PCB inter-connection and calibration light injection.

- The surface of one module layer needs to be sub-divided into several PCBs; the interconnection must be realized in a way which allows exchange of PCBs in case of need for repair and still ensures high reliability. The subdivision must take the many different layer sizes into account.
- Optical calibration signal routing must be integrated.
- The thermal coupling between ASICs and absorber structure must ensure efficient heat dissipation.

A possible solution is sketched in cross-section above. The heat dissipation in such a structure has been estimated with analytic methods. With power-cycled VFE ASICs but permanent bias voltage supply to the SiPMs, a power consumption of $40\mu\text{W}$ per channel induces a gradient of 0.3K over the 2m length after typically 6 days of operation. This means that no active cooling is necessary for the bulk of the detector. The currents – 3A per layer during the bunch train – also seem to be manageable.

2.5 Calibration system considerations

The calibration system of the test beam prototype is highly redundant and provides a variety of possibilities to monitor the SiPM parameters. It is presently assumed that a much simpler system can be built which relies on the auto-calibration properties of the SiPMs alone. Since the response to individual photo-electrons provides the relevant scale, the light intensity does not need to be precisely stabilized or monitored with PIN diodes. Furthermore it requires only

small and fixed light intensities to be injected within a comfortable amplitude range, thus relaxing the constraints on the optical signal distribution.

2.6 HCAL conclusion

The concept for a scalable HCAL prototype is taking shape, and critical technical design issues have been identified. Next, small prototypes of individual components should be built and tested, e.g. for PCB tile SiPM connection, board interconnection and calibration system integration. In parallel the readout chain must be established, the SiPM ASIC interplay verified and the ASIC communication with the DAQ extended to the HCAL case. As the mechanical design of the absorber stack and layer integration proceeds, the FE electronics chain can be implemented into a compact design of the challenging end face region.

3 Very forward calorimeter (VFCAL)

3.1 Introduction

Two calorimeters, BeamCal and LumiCal, are planned for the ILC detector to extend the coverage to small polar angles, to measure precisely the luminosity and to assist beam tuning to optimize the luminosity. The calorimeters must be fine-grained and compact. The innermost calorimeter has to withstand harsh radiation conditions and must be readout bunch-by-bunch. LumiCal must be positioned extremely precise and the inner acceptance radius must be controlled on μm level.

The goal of the VFCAL project is to design these special forward calorimeters and to develop the infrastructure for tests of all subcomponents, i.e. to develop position monitoring on μm level, to investigate radiation hard sensors, to design and test ultra-thin sensor planes and fast FE electronics.

3.2 Positioning Control using Laser Beams

The luminosity measurement requires extremely precise alignment of the two LumiCal detectors to each other and very precise positioning with respect to the beam line and the interaction point. Monte Carlo simulations have shown that the inner radius of the calorimeter has to be controlled with the accuracy of about $4\ \mu\text{m}$, the distance between calorimeters along the beam axis must be known to an accuracy of $60\ \mu\text{m}$ over the $6\ \text{m}$ distance and the transversal displacement (x, y) with respect to the beam is required to be known to $500\ \mu\text{m}$ accuracy.

Laser beams, mirrors placed at reference positions on the calorimeter and the beam-pipe, and CCD sensors will be used for position control. The principle simplified scheme is shown in Figure 3.1. A laser beam is split by a semi-transparent mirror or prisma into two beams, one hits the CCD sensor directly, the other is deflected by a second mirror and hits the sensor under a certain angle. The CCD sensor detects the movement of the spot from the direct beam in the (x - y) plane. The distance between the two spots measures the displacement in the z direction.

A test bench will be installed at INP Cracow to demonstrate that this system matches the required accuracy. It will be computer controlled and special hard- and software will be developed for the CCD readout and the laser spot position determination.

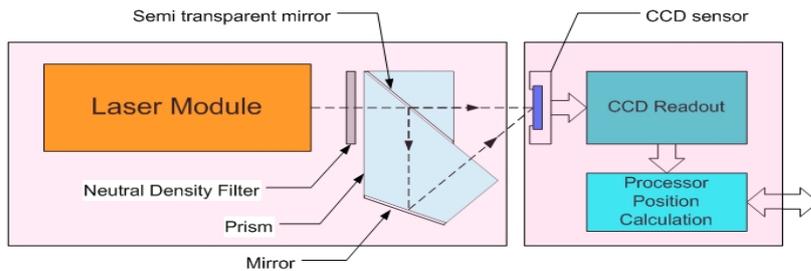


Figure 3.1. The principle of the position measurement using two laser beams of a given angle with respect to each other and a CCD sensor. The position and the relative distance of the two laser spots allow to control the x, y and z positions.

The position of the sensors planes will be controlled by an optical system. The beam from an infrared semiconductor laser module placed in a hole of the support frame traverses the semitransparent CMOS position sensors. Another possibility is to use a wire tensed between front and rear C shape steel frame passing through the holes in all detector planes. Capacitive sensors can measure the transversal displacement of the sensor planes with respect to the wire. Both set-ups will be studied by INP in Cracow.

3.3 Studies on Sensors

For electrical tests of sensors laboratories are planned in Cracow, DESY and Tel Aviv. Probe-stations will be installed in 10k clean rooms and equipment to measure leakage currents and capacitances will be procured and brought into operation.

Beam-tests will be done for radiation hardness tests of several sensor materials in a high intensity electron beam and for performance measurements of pad sensors in a low intensity high energy beam.

The design of the test-beam equipment for sensor tests in low-energy and high intensity electron beams is shown in Figure 3.2.

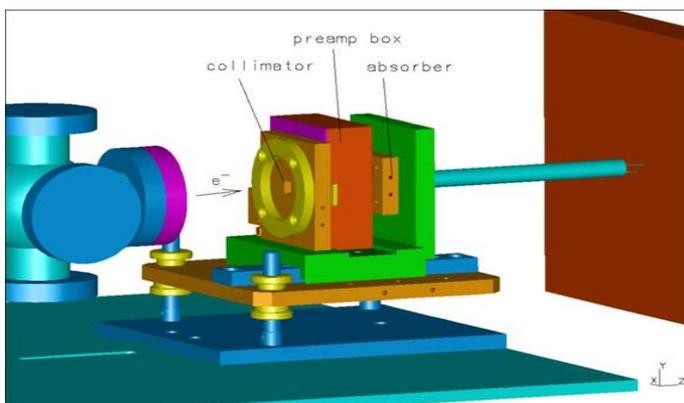


Figure 3.2. The design of the test-beam set-up to be used for radiation hardness studies in low-energy electron beams of high intensity. An electron beam leaving the beam-line exit window on the left is shaped by a brass collimator to traverse the sensor inside the box. The beam current is measured by a Faraday cup (absorber).

The electron beam coming from the left crosses the sensor inside the box. Currents are measured from the collimator and the Faraday cup, to adjust the beam and to measure the amount of electrons having crossed the sensor.

Measurements using a low intensity beam of high energy electrons are necessary to understand the response of the sensors to single ionizing particles, notably the homogeneity of the response and the behavior near the pad boundaries. In a second stage parts of sensor planes will be tested to understand the performance of the full system including FE electronics.

For these studies a movable table and a DAQ will be developed at DESY to be used within the EUDET test-beam infrastructure.

3.4 Sensor Design and Procurement

Both BeamCal and LumiCal are planned as sandwich calorimeters with tungsten as absorber and silicon or a more radiation hard material as sensor. The design of sensors for a prototype calorimeter will be pursued in parallel with the creation of the infrastructure. As an example, the design of a sector made of silicon pad sensors planned for LumiCal is shown in Figure 3.3. The design is based on a 6-inch silicon wafer of 300 μm thickness.

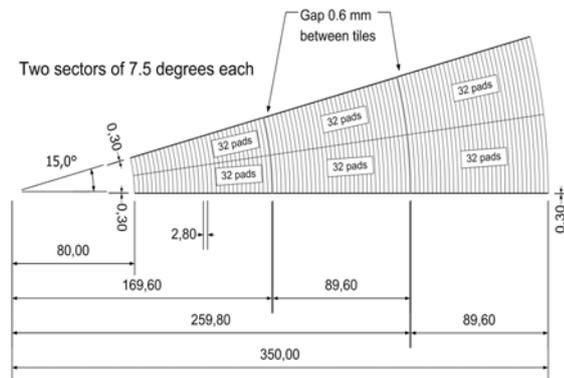


Figure 3.3. The design of a sector for LumiCal. Several tiles which are subdivided into pads will be combined on a carrier to form a sensor plane.

The groups in Cracow and Tel Aviv will search for partners in the industry to develop these pad sensors. Diamond and GaAs sensors for the BeamCal are studied by DESY in collaboration with the FAP Freiburg and Russian partners.

3.5 VFCAL FE electronics

The requirements on the FE electronics are different with respect to the other calorimeters. LumiCal has a higher occupancy, BeamCal must be read out after each bunch crossing and the signal size varies strongly when beam-parameters are changed. Monte Carlo simulations are planned to estimate the conditions for the FE design.

The group from the AGH University of Science and Technology in Cracow will work on the design of an integrated FE readout circuit. In a first stage a chip containing a few channels will be designed and produced. Infrastructure for tests will be developed also in DESY, including the development of dedicated FE hybrids. In case the results are satisfactory the chip will be supplemented by an ADC and a memory.

4 Front end electronics (FEE)

4.1 Introduction

The very high level of integration is a new and challenging feature of ILC calorimeter electronics. What used to occupy racks and racks of electronics around detectors will now be embedded inside the detector and only send out zero-suppressed digital data. It is thus essential for ILC to establish the feasibility of this high level integration and operate it on prototypes on testbeam.

Several features of the readout electronics are common to the electromagnetic and hadronic calorimeters, in particular the readout protocol, which led to the simultaneous development of the 3 types of ASICS :

- HaRDROC (Hadronic Rpc Detector Read-Out Chip) for the digital hadronic calorimeter (DHCAL)
- SKIROC (Silicon Kalorimeter Integrated Radout Chip) for the electromagnetic calorimeter (ECAL)
- SPIROC (Silicon Photomultiplier Integrated Read-Out Chip) for the analog hadronic calorimeter (AHCAL)

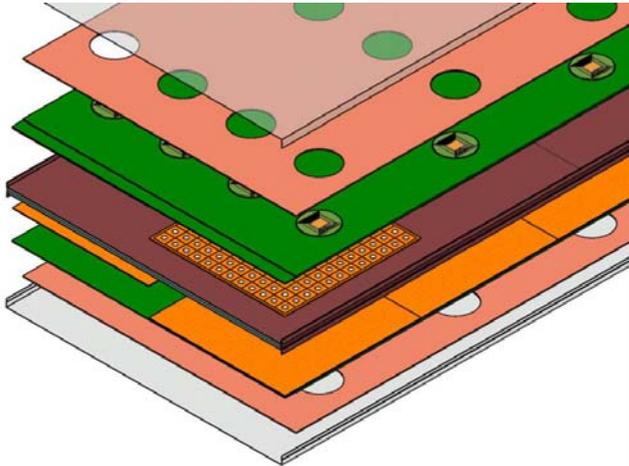


Figure 4.1 – integrated electronics for the ECAL

4.2 HaRDROC ASIC description

The HARDROC ASIC is the first milestone of the JRA3-FEE program. It is used to readout gaseous detectors (RPCs or GEMS or Micromegas). The analog part is derived from a 64ch ASIC developed by CNRS/LAL/Orsay for the ATLAS luminometer, with emphasis on reducing power dissipation and adding full power pulsing capability. It feeds 2 discriminators which code the signals on 2 bits per channel. The digital part stores up to 128 events and allows sequential daisy-chain readout. This chip is the first chip for a second generation ILC-like DAQ as developed in JRA3-DAQ. The synoptic is shown in Fig 4.2.

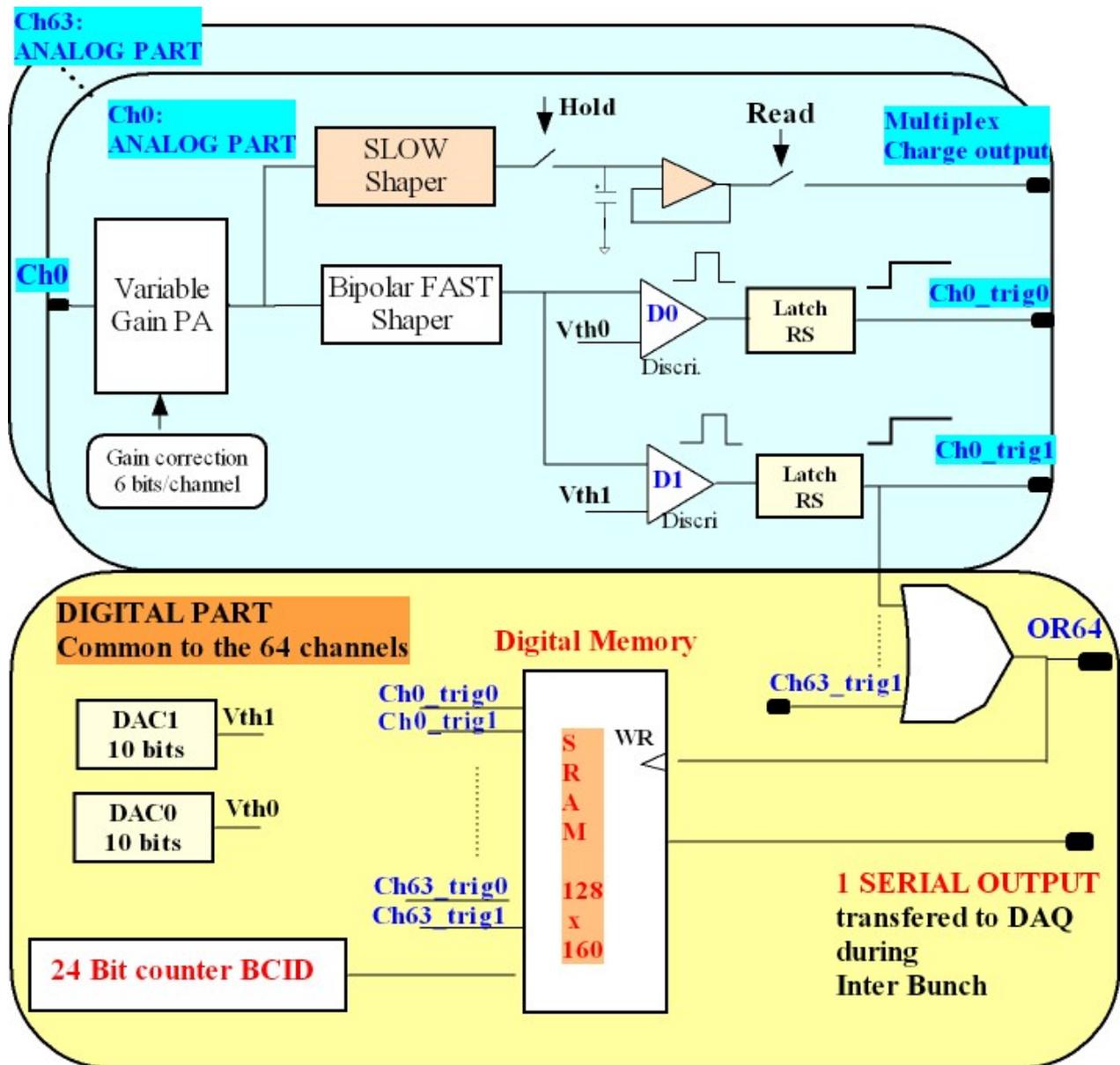


Figure 4.2 – synoptic diagram of HARDROC ASIC

The signal from the detector is fed into a variable gain preamp (0 to 4 over 6 bits) which allows to tune the gain depending on the detector used. It then feeds a slow channel that allows a multiplexed charge readout with CALICE standard DAQ. A second path drives a fast shaper (15ns) followed by 2 discriminators that register the hit channels. The thresholds are loaded digitally thanks to two 10bit DACs. The hit pattern is stored in a 128*140 SRAM memory that also stores the bunch crossing number (BCID) coded on 24 bits. Up to 100 chips are read serially on a daisy chain mode, during the interbunch.

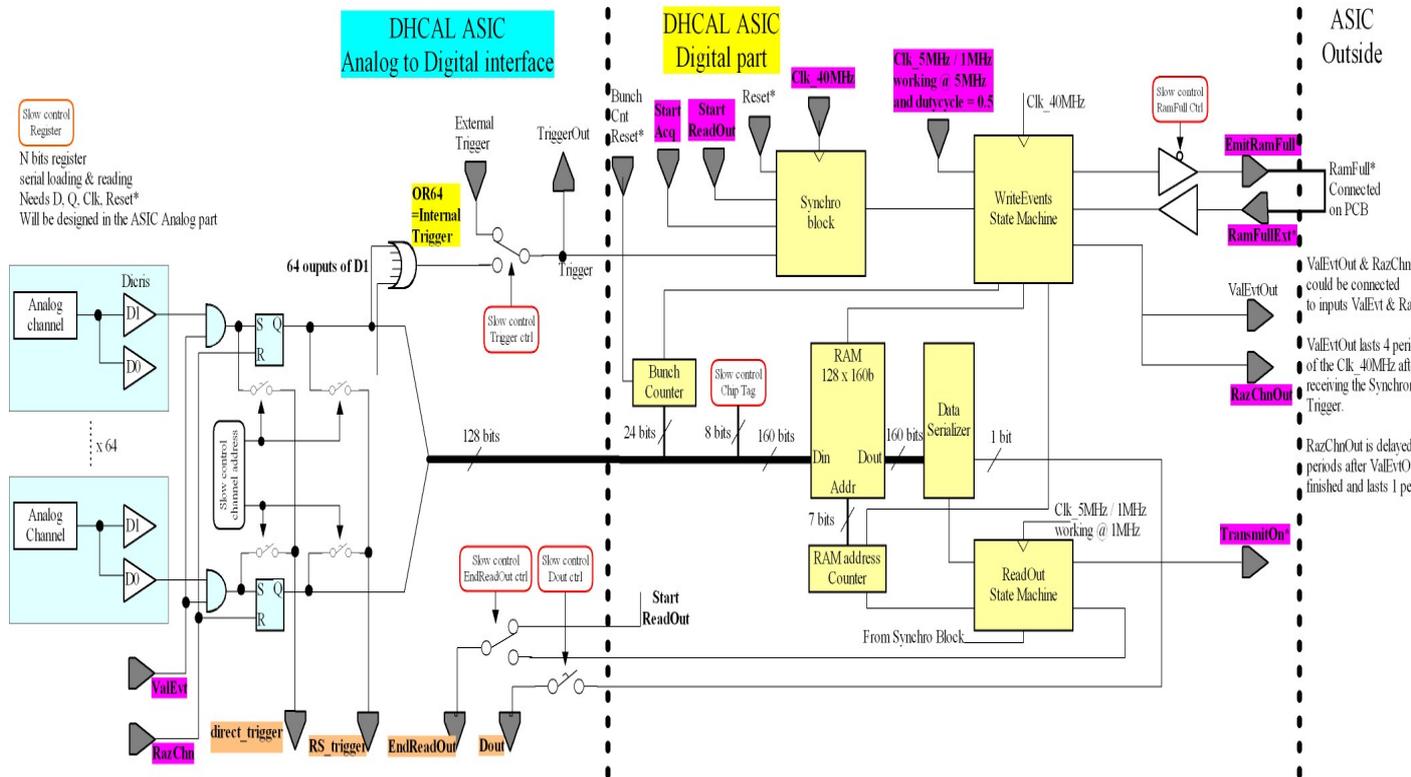


Figure 4.3 – synoptic of the digital part of HARDROC

The chip has been fabricated in september 2006 in Silicon Germanium 0.35µm foundry from AustriaMikroSystem. The layout is shown below, it covers an area of 16 mm². The chip has been received in December 2006 and is currently under test, with good preliminary results. It will be used by various groups to test the DAQ principle and to test the first prototypes of DHCAL.

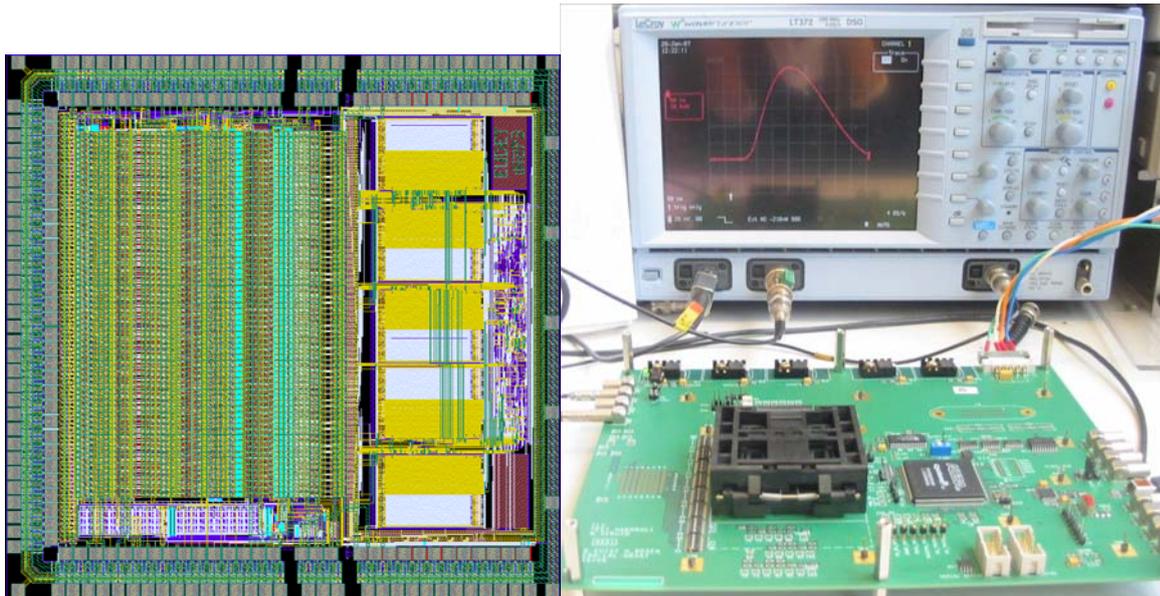


Figure 4.4 – layout of HARDROC and chip on testboard

4.3 SKIROC ASIC description

Starting from HARDROC, the second chip developed is for the ECAL, where the detector is now 1 cm² Si diodes. The chip must now integrate low noise charge preamp, bi-gain shaper and handle signals up to 3000 MIPs, corresponding to a dynamic range of 16 bits.

The synoptic diagram is shown below :

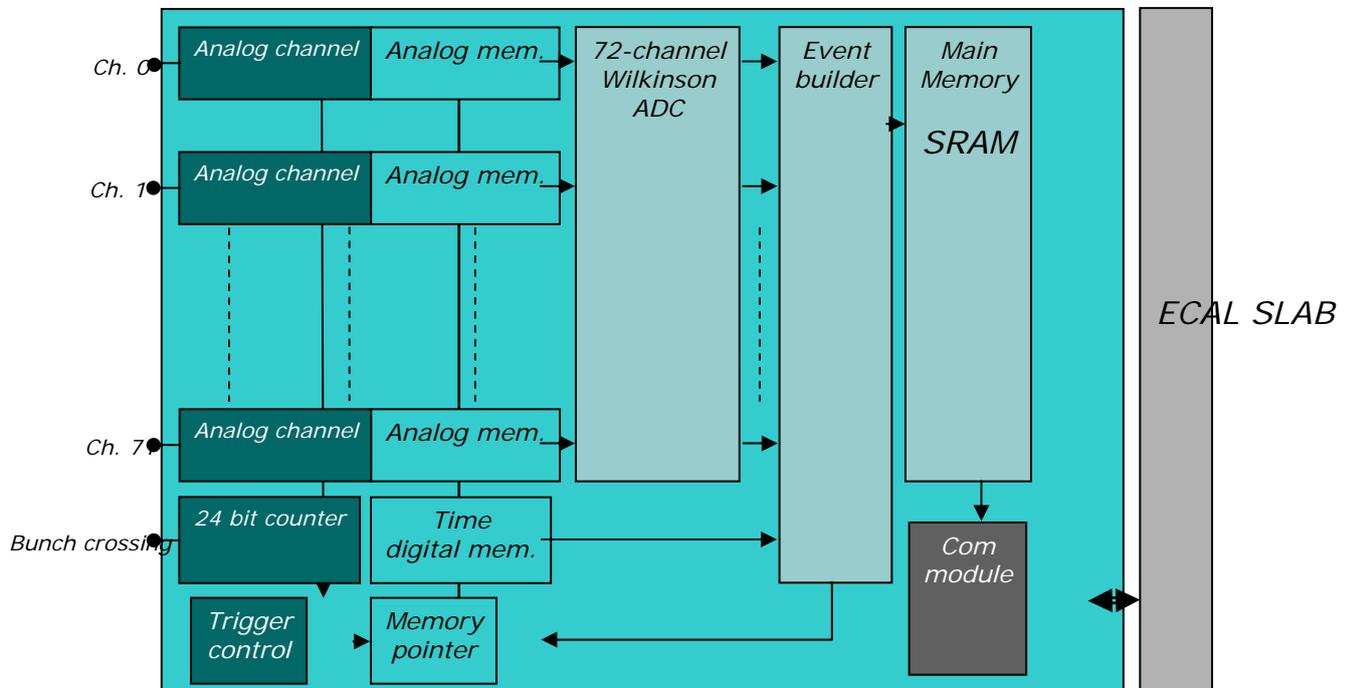


Figure 4.5 – synoptic of the digital part of SKIROC

The chip also incorporates 64 12bit Analog to Digital converters (ADCs). Due to the high level of complexity in the analog design and digital sequencing, it has been found too risky to

integrate the digital part, which has been left outside in an FPGA. A complete VHDL description of this part has been written and be tested in 2007.

The chip has been realized in SiGe 0.35 μ m technology by AustriaMikroSystem GmbH. It covers an area of 20 mm² and has been fabricated in December 2006.

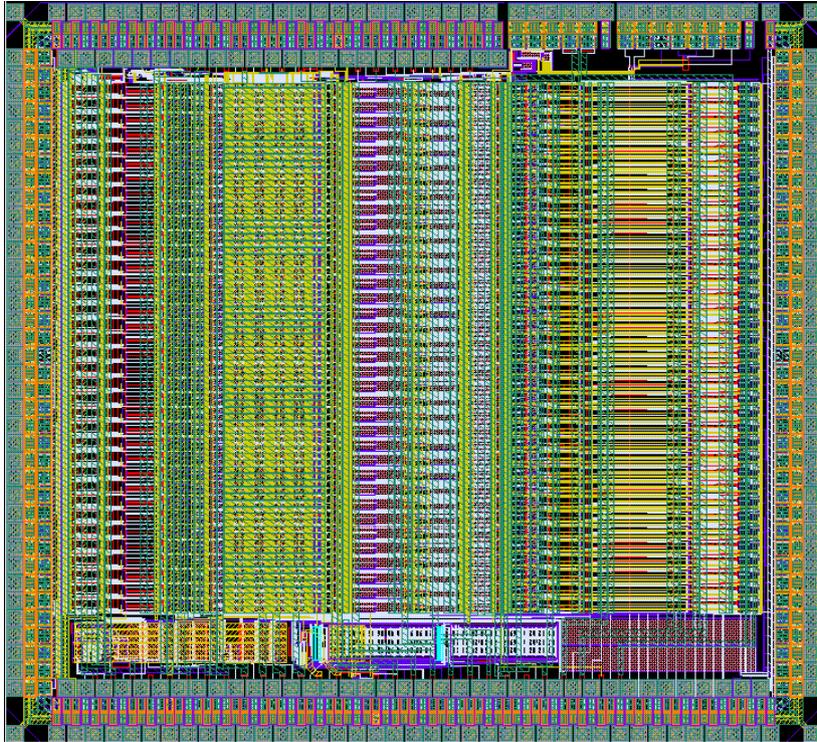


Figure 4.6 – layout of SKIROC

4.4 FEE conclusion

Two major ASICs have been realized in 2006, which will allow the study of on-detector electronics integration throughout 2007 and the 2nd generation DAQ. Good performance of these ASICs will be a key element for series production in 2008 to equip the EUDET ECAL and DHCAL modules.

5 Data acquisition (DAQ)

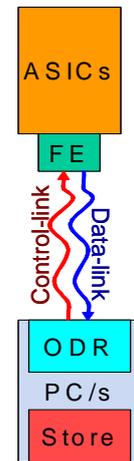
5.1 Introduction

Although JRA3 DAQ is in its infancy, it builds upon a well established DAQ used by the CALICE collaboration. Much of our effort involves using commercial equipment where bespoke hardware was used before. It follows, therefore, that the central component of this package is the development of detector readout hardware and interfaces.

We have specified and purchased a prototyping card that will facilitate the development of both ends of the detector to PC link, as well as later work on transferring clock and control signals in the opposite direction.

The conceptual DAQ can be divided into 6 parts;

1. Front-End interface to sub-detector (FE)
2. Data-link (FE to Off-Detector Receiver)
3. Off-Detector Receiver (ODR) card
4. Control data-link (Clock, Control to FE)
5. Data Store
6. Software



The commercial hardware constraint allows for a simplified design process. Although much of the design detailed here is no more than a block diagram, the use of real-world components will hopefully allow development of the first system prototype to proceed efficiently.

5.2 DAQ Goals

- Use commercial components where possible:
 - Readout links use standard connectors and protocols
 - Fibre-optic links
 - PCI-Express readout board hosted in a standard PCs
- Modular, general purpose design:
 - Generic readout board for all users
 - Detector specific interfaces as plug-in modules
 - Other ‘bespoke’ functionality in firmware
- Front end ‘Control-link’ attempts to use commercial hardware too
 - Extract ‘fast’ signals from commercial signalling
 - Reconfigure FE firmware using control-link
- Software general purpose for possible EUDET wide use
 - Use plug-ins for specific detectors and environments
- Failure protection (fail-over)
 - PCs not reliable – reroute signals on-the-fly

5.3 Component Detail

5.3.1 Front End (FE) Interface

The FE is tasked with interfacing directly with sub-detector ASICs. It is assumed to be an FPGA for maximum flexibility. Data is collected (or accepted) from the ASICs by the FE, buffered (if needed) and packaged and transmitted off-detector. The FE will be responsible for formatting it in the desired data link protocol (S-Link, Ethernet, raw etc.)

The FE also receives configuration signals from off-detector, and packages and distributes them as needed to the ASICs.

As the detector slabs will be constructed from shorter sections, the FE assumes to connect at the end of the slab. Work is already underway at Cambridge¹ to mimic the digital operation of the ECAL FE ASICs. This will provide a first attempt at defining an ASIC/FE interface.

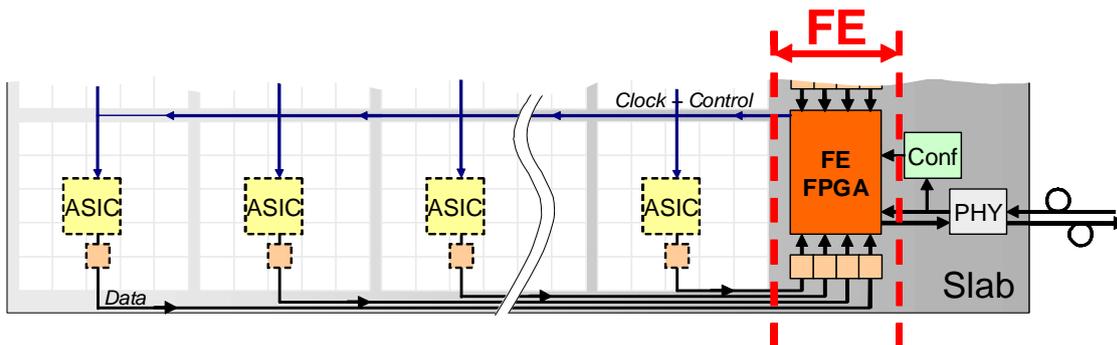


Figure 5.1. FE in context of an ECAL ‘slab’

5.3.2 Data-link

The data-link represents the physical link (regardless of protocol) from FE to off-detector, covering the path of data from the FE FPGA to a off-detector FPGA. It is presumed to be fibre-optic, and makes use of commercial interfaces and protocols; e.g. HSSDC2, SFP (see 5.2) using Ethernet or S-Link protocols. They are expected to operate above 1Gbit.

Using FPGA’s with manufacturer provided firmware for their gigabit transceivers allows for the whole link to be built using standard components. It can also be modelled and tested the off detector receiver.



Figure 5.2. Giga-bit connector formats: HSSDC2 for (mainly) copper, SFP for fibre-optic

5.3.3 Off-Detector Receiver (ODR)

Data from the FE is collected by the Off-Detector Receiver cards. These cards are hosted by a PC with PCI-Express bus. The goal is to keep the hardware as generic as possible, allowing for use on multiple (sub-)detectors. Conceptually each card consists of a large FPGA (with embedded CPUs, if needed), some buffer RAM and sites for attaching data and control link hardware as needed by those interfaces. It is envisaged that cards could host FE firmware (and similar link hardware) to facilitate testing without real FE’s (FE emulation).

Provision is also made for interfacing with fast-control (clock and trigger) sources, as well as transmitting these signals to the FE. The ODR concept is shown in 5.3.

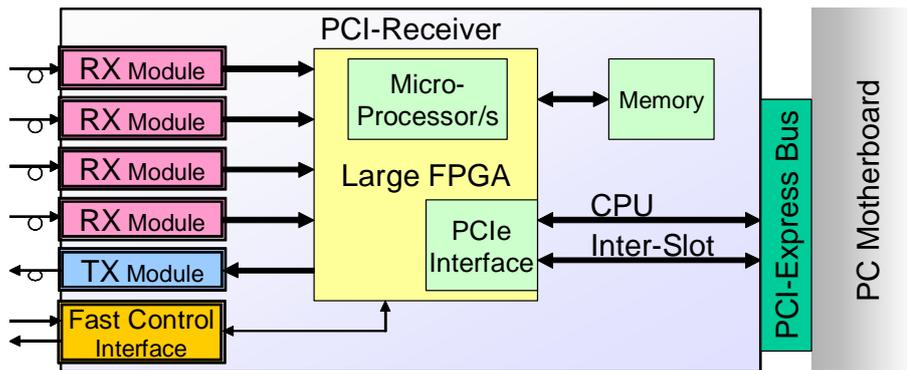


Figure 5.3. Conceptual design of the Off-Detector Receiver

We have found a development board that suits our requirements extremely well: the *PLDA XpressFX100*ⁱⁱ (shown in Figure 5.4). It is supplied with a PCI-Express firmware core, that has allowed us to side-step that development work.

The board is based on a Xilinx Virtex 4 FX100 FPGA, which has extensive logic resources as well as a pair of 400MHz CPUs. Two pairs of gigabit interfaces are already fitted, with room to add four more via plug-in modules. It supports 8x PCI-Express (a bandwidth of 10Gbit), and has 128Mbyte of DDR2 RAM onboard. All round this seems a very powerful and versatile board, suitable for test-beam use.

It is envisaged that the firmware developed for this board will be portable enough to be used on custom boards if needed.



Figure 5.4. XpressFX prototyping and development board.

The ODR is a central component of the DAQ the focus of our activity at present. Cambridge, Manchester, RHUL, UCL have a board each, along with a hardware development PC. A basic Linux driver has been written for SLC4 and we can communicate with the board (e.g PCI-Express core is working).

Separately an Ethernet interface is working, with the only outstanding code for a first-order receiver being a DDR2 memory controller, which is under active development. We expect to complete a test data transfer system by end of year.

5.3.4 Control-Link (Clock and Control)

The control-link transports configuration data to the FE, as well as clock and timing synchronisation signals. For data it uses exactly the same hardware as the data-link but in the opposite direction. Timing synchronisation poses some additional challenges; we will attempt

to recover a machine clock and synchronising signals from the link electronics, but this might be difficult on the test-beam schedule. As a fall-back, discrete interfaces for clock, trigger and possibly power-pulsing will be provided. 5.5 shows the concept.

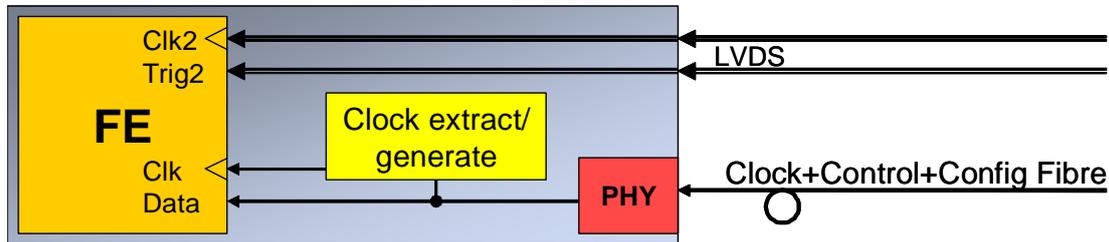


Figure 5.5. Control link concept.

5.3.5 Datastore and Software

Data needs to be stored for processing. It is unlikely that the volume will exceed bandwidth and storage limits at this stage, so the first-order prototype will write it directly to disc. The data will then be available to higher level DAQ software via e.g. NFS. If data volume increases it could be zipped in firmware.

Higher level software is in the very early design phase and will likely be derived from the existing CALICE structure where possible, although detector configuration and usage models need to be finalised before work begins.

5.4 DAQ conclusion

Work has started on the DAQ, with the primary being focus on the read-out hardware, which is progressing well. As detector specifics and areas of use stabilise development will expand to incorporate these.

Acknowledgement

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References

ⁱ Study of data paths on ECAL Slab

<http://ilcagenda.cern.ch/materialDisplay.py?contribId=71&sessionId=4&materialId=slides&confId=737>

ⁱⁱ PLDA PCI Express XpressFX Development Board

http://www.plda.com/products/board_pcie_fx.php