
# Description of the JRA1 Trigger Logic Unit (TLU)

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## Abstract

This document describes the interfaces and operation of the EUDET JRA1 Trigger Logic Prototype ( TLU v0.1a ) with firmware version 14. The TLU is intended for test-beam use and provides a simple interface between the beam-trigger, the DAQ and the device-under-test[2].

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[2]Any good ideas are due to the collaborative efforts of members of the JRA1 working group. Any errors in documenting or implementing them are due to the author.

# 1 Introduction

The TLU is based around an “off-the-shelf” FPGA board[1]. It has LVDS and/or TTL interfaces to the beam-telescope readout and any devices under test, PMT signal and/or NIM level signal interfaces to the beam-trigger and a USB interface to the DAQ. The most up-to-date version of this document can be found at http://svn.phy.bris.ac.uk/svn/uob-hep-pc017a/trunk/www/Docs/tlu_v0_1_manual_eudet_note.pdf

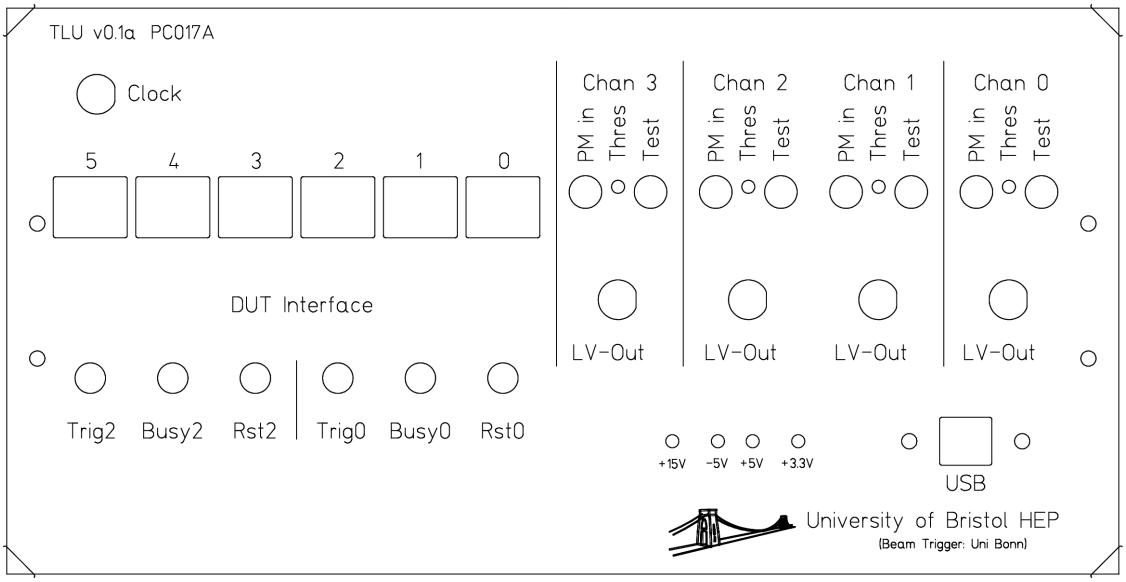
# 2 Power Requirements

5V @ 1A supplied on a 2.5mm connector on rear panel. Centre conductor positive.

# 3 Interface

## 4 Front Panel

The front panel for the TLU is shown below:




## 5 Control

USB2.0 , “B” type connector on front panel.

# 6 Clock

There is a 2-pole LEMO-OB connector on the front panel for input or output of the internal clock. (the internal clock sets the “tick” for the trigger time-stamp). When used as an output the 100-ohm termination resistor R23 should be removed. Input can be either LVDS or LVPECL (3.3V referenced). Pin-1 (red dot) is the non-inverting signal. Not used by the current version of the firmware.

## 7 Beam Trigger

Four LEMO-00 single pole connectors on front panel, terminated into 50-ohms. Negative going pulses. The discriminator produces fixed length output pulses. If the pulses are too short and/or too close to the threshold narrow “glitches” rather than full length output pulses are produced. Pulse of greater than 3ns at -500mV are sufficient to produce correctly recognized pulses. The signal from the “Test” outputs can be used to monitor the output of the discriminators

(terminate test outputs into 50-ohms at oscilloscope for a 21:1 probe of the discriminator output). Details of the discriminator unit can be found elsewhere[2].

Four 2-pole LEMO-OB connectors, marked LV-out, provide power for internally powered PMT bases. By default a 15V DC-DC 300mA regulator is fitted, but this can be changed on request. Pin-1 ( red dot ) is positive.

# 8 Telescope and DUT

### 9 LVDS Interfaces

Six RJ45 connectors on front panel. LVDS levels. Pin out:

1. Trigger+
2. Trigger-
3. Busy+
4. Reset+
5. Reset-
6. Busy-
7. Data-clock+
8. Data-clock-

### 10 TTL Interfaces

Two of the six DUT interfaces (0 and 2) can be connected to LEMO-00 connectors carrying 3.3V LVTTL signals. Only Trigger, Busy and Reset are connected. Outputs ( Trigger, Reset ) are always active, input ( Busy ) is only active if selected by changing a link on the TLU motherboard ( Remove R8,R9, replace with zero-ohm links at SB1, SB2. See schematics[3] ). When TTL inputs are selected the corresponding LVDS "BUSY" inputs are not active.

The TTL outputs can be driven into 50-ohms biased to $V_{cc}/2$. The TTL inputs are terminated into 50-ohms biased to $V_{cc}/2$ by default, but can be changed to terminate into 50-ohms in series with 100pF to ground ( remove R16, R20. Replace R38, R39 with 100pF capacitors).

# 11 Direction of Data-clock

The data-clock lines can either be an input to or an output from the TLU. The direction is set by a switch, "U7" on the TLU motherboard. Moving the switch towards the silk-screen legend "Rx" configures the lines as inputs. Moving the switch towards "Tx" configures them as outputs from the TLU. **N.B. For normal operation U7 should be set to "Rx".**

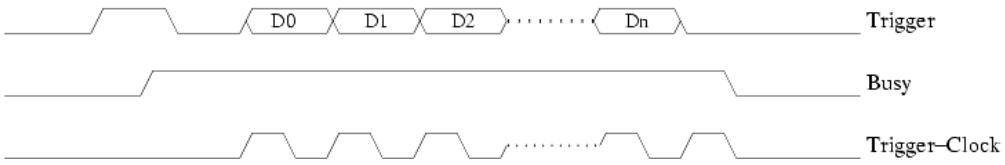
# 12 Handshake between TLU and DUT

There are two modes of hand-shake between the TLU and the DUT. A "simple handshake" and a "trigger data handshake" where data is transferred from the TLU to the DUT on each trigger.

# 13 Trigger Data Handshake

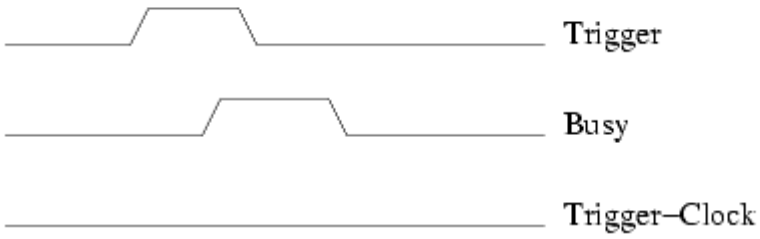
1) TLU receives trigger from beam scintillators
2) TLU asserts TRIGGER
3) On receipt of TRIGGER going high, the detector asserts BUSY

4) On receipt of BUSY going high, TLU de-asserts TRIGGER and switches the TRIGGER line to the output of a shift register holding the trigger number/data.
5) The DUT clocks data out of the shift register by toggling TRIGGER_CLOCK. Data changes on the rising edge of TRIGGER_CLOCK. The least significant bit of the trigger data is shifted out first.
6) After clocking out the trigger number ( and the detector being ready to take more data, the DUT de-asserts BUSY)
7) System is ready for triggers again.




## 14 Simple Handshake

1) TLU receives trigger from beam scintillators
2) TLU asserts TRIGGER
3) On receipt of TRIGGER going high, the detector asserts BUSY
4) On receipt of BUSY from DUT, the TLU de-asserts TRIGGER
5) On receipt of TRIGGER going low and the detector being ready to take more data, the DUT de-asserts BUSY
6) System is ready for triggers again.




( state of Trigger-Clock is irrelevant in this mode)

## 15 Trigger Latency

The time interval between the beam-trigger arriving at the TLU and trigger(s) being issued to the DUT(s) is 69 +/- 10 ns. The large jitter is because, in the current version of the firmware, incoming triggers are sampled onto an internal clock before being processed. Future versions of the firmware will have lower latency and asynchronous logic (with respect to the system clock) to allow for fixed latency (jitter determined by electrical noise rather than clock frequency).

# 16 Control Interface

The ZestSC1 FPGA module uses a Cypress EZ-USB micro-controller to implement a USB 2.0 interface. There are two modes of operation – register and block transfer. The register interface is one byte wide. The block transfer mode transfers blocks of 16-bit words.

# 17 Address Map

For register mode transfer the address map is as follows ( the names refer to constants defined in TLU_address_map.h and TLU_address_map.vhdl )

| *Location* | *Read/ Write* | *Function* |
|---|---|---|
| BUSY_REG_ADDRESS | R | Value of the busy lines coming from DUTs |
| DUT_RESET_ADDRESS | W | Asserts reset line on DUTs for one clock cycle. |
| DUT_TRIGGER_ADDRESS | W | Asserts trigger line on DUT for one clock cycle. Active even when beam-triggers have been inhibited by writing to TRIG_INHIBIT_ADDRESS. Activates TRIGGER/BUSY handshake |
| TRIG_INHIBIT_ADDRESS | R/W | Writing '1' to bit 0 (LSB) vetoes triggers. Writing '0' to bit 1 re-enables triggers Reading gives current state of veto in bit-0 and current state of overall veto (including vetoes caused by beam_trigger) in bit-1 |
| RESET_REGISTER_ADDRESS | W | Writing '1' to a bit issues a reset.<br>Bit mapping:<br>TIMESTAMP_RESET_BIT 0<br>TRIGGER_COUNTER_RESET_BIT 1<br>BUFFER_POINTER_RESET_BIT 2<br>TRIGGER_FSM_RESET_BIT 3 |
| INITIATE_READOUT_ADDRESS | W | Puts block transfer state machine into INITIATE_TRANSFER state. |
| STATE_CAPTURE_ADDRESS | W | Writing causes BUFFER_POINTER, TIMESTAMP and TRIGGER_COUNTER to be copied to registers ready for reading, |
| TRIGGER_FSM_STATUS_ADDRESS | R | Status of the finite state machines controlling the trigger outputs. 0=idle, 1=busy. One bit per DUT. |
| REGISTERED_BUFFER_POINTER_ADDRESS_0 | R/W | Next location of time-stamp buffer to be written. 0 is LS-Byte, 1 is MS-Byte. Updated when STATE_CAPTURE_ADDRESS is written to |
| REGISTERED_BUFFER_POINTER_ADDRESS_1 | R/W | |
| REGISTERED_TIMESTAMP_ADDRESS_0 | R | 64-bit value of the time-stamp captured when STATE_CAPTURE_ADDRESS is written to. |
| REGISTERED_TIMESTAMP_ADDRESS_1 | | |
| REGISTERED_TIMESTAMP_ADDRESS_3 | | |
| REGISTERED_TIMESTAMP_ADDRESS_4 | | |
| REGISTERED_TIMESTAMP_ADDRESS_5 | | |
| REGISTERED_TIMESTAMP_ADDRESS_6 | | |
| REGISTERED_TIMESTAMP_ADDRESS_7 | | |
| REGISTERED_TRIGGER_COUNTER_ADDRESS_0 | R | 32-bit value of trigger-counter |
| REGISTERED_TRIGGER_COUNTER_ADDRESS_1 | | |
| REGISTERED_TRIGGER_COUNTER_ADDRESS_2 | | |
| REGISTERED_TRIGGER_COUNTER_ADDRESS_3 | | |

| *Location* | *Read/ Write* | *Function* |
|---|---|---|
| BEAM_TRIGGER_AMASK_ADDRESS[3] | R/W | AND mask for input triggers. Bottom 4 LSB significant |
| BEAM_TRIGGER_OMASK_ADDRESS[4] | R/W | OR mask for input triggers |
| BEAM_TRIGGER_VMASK_ADDRESS[3] | R/W | VETO mask for input triggers |
| DUT_RESET_DEBUG_ADDRESS | R/W | Write static level to RESET outputs. |
| DUT_TRIG_DEBUG_ADDRESS | R/W | Write static level to TRIGGER outputs. Does not activate TRIGGER/BUSY handshake |
| DUT_CLOCK_DEBUG_ADDRESS | R | Read values of DUT_CLOCK lines |
| DUT_LED_ADDRESS | R/W | Control the LEDs. '1'=illuminated |
| INTERNAL_TRIGGER_INTERVAL | R/W | Interval (in milliseconds) between internal triggers. Writing zero disables internal triggers |

# 18 Readout sequence

When the TLU receives a trigger it writes the current value of the 64-bit time-stamp into a buffer and the BUFFER_POINTER is incremented. The trigger counter is also incremented. To order to perform an "atomic" read on the value of BUFFER_POINTER, TRIGGER_COUNTER and TIMESTAMP, write (any value) to STATE_CAPTURE_ADDRESS. The values are then captured and stored in REGISTERED_BUFFER_POINTER, REGISTERED_TRIGGER_COUNTER and REGISTERED_TIMESTAMP.

To read out the buffer of timestamps, the following sequence should be followed:

1) Write '1' to LSB of TRIG_INHIBIT_ADDRESS, this stops further triggers
2) Write any value to INITIATE_READOUT_ADDRESS
3) Use TLUReadData function on host to transfer content of time-stamp buffer to the host.
4) Write to bit '2' of RESET_REGISTER_ADDRESS to reset the buffer pointer (so that further timestamps are written at the start of the buffer)
5) Write '0' to bit-1 of TRIG_INHIBIT_ADDRESS to enable triggers.

# 19 Grounding and Shielding

The RJ45 connectors for the DUT interface allow shielded cable to be used. **It is recommended that shielded cable is used**. Unlike 10/100/1000-BaseT Ethernet where the signals are DC-balanced and can be AC-coupled, the interface between the TLU and the DUT is not DC-balanced and is DC-coupled. This limits the common-mode voltage between the DUT and TLU to between 0.3V and 2.1V[5]. Excessive current flow through any ground loops formed should be reduced using ferrite cores round the cables.

[3]Not implemented in version 14 of the firmware
[4]Writing 0x0F enables all beam triggers. Writing 0x00 disables all beam triggers ( internal triggers are not affected). Triggers are "OR"ed together.
[5]Set by the sn65lvdm1676 transceivers used in the TLU. This common mode range will be even lower if the DUT has a lower common mode range.

## Acknowledgements

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## References

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