



## JRA1 – Status of the Demonstrator Telescope

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### Abstract

In this memo the overall status of the EUDET JRA1 Demonstrator Telescope will be described. This is a summary of a report given at the EUDET Annual Meeting.

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# 1 Introduction

Within EUDET JRA1 a test beam telescope will be developed. It will provide a high precision of better than  $3 \mu\text{m}$ , even at the lower energies available at the DESY test beam facility. In addition to high precision, a high readout speed and easy handling is of importance.

The project is divided into two phases. During the first phase a first test facility with analogue readout and a much lower readout speed will be built. This gives the opportunity to check the design and to have a first telescope quickly available for the groups working on detector R&D. The use of an established pixel technology with analogue readout and no data reduction gives the possibility to have such a telescope ready on a very short time scale.

This memo describes the status of the Demonstrator Telescope at the time of the EUDET annual meeting October 2007. The Demonstrator was ready for test beam early summer 2007.

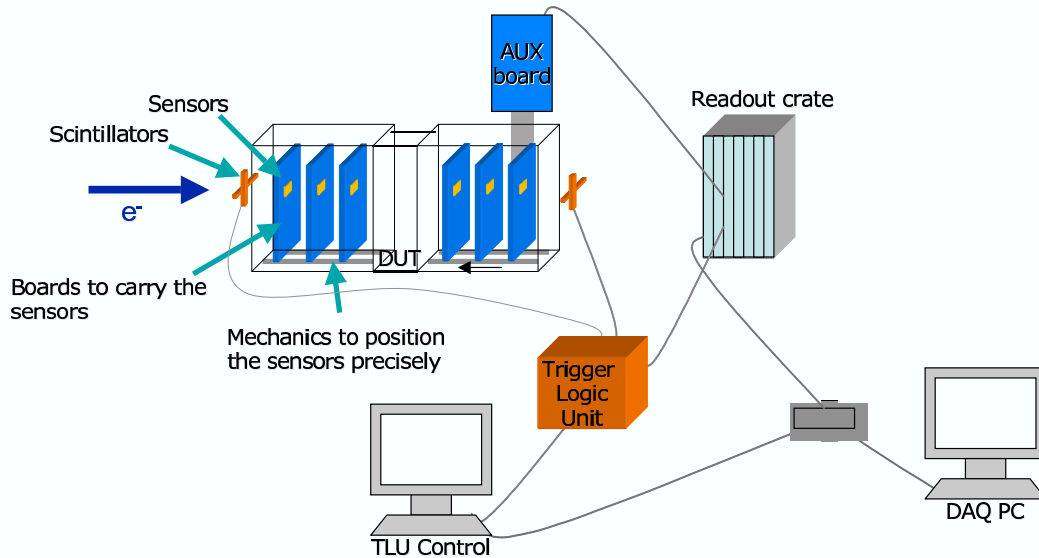


Figure 1: Overview of the ingredients needed for an analogue telescope.

In Figure 1 all "ingredients" for such an analogue telescope are shown. In the following sections the availability and status of all these components will be described.

Following hardware elements are the main parts of the telescope:

- MimoTel Sensors with  $256 \times 256$  pixels and a pitch of  $30 \mu\text{m}$ . These chips were developed at IPHC Strasbourg.
- Precisely worked mechanics to position the sensor boards in the particle beam.
- The EUDRB readout boards developed at INFN Ferrara.

- A MVME 6100 VME CPU.
- The Trigger Logic Unit developed at Bristol University.
- As DAQ Computer a MAC Pro with 4×1 TB raid array for data taking.

## 2 Reference Plane Sensors: MimoTel

As sensors for the reference planes the MimoTel prototype is used. This is a chip processed in the AMS 0.35 OPTO process with 14 and 20 $\mu\text{m}$  epitaxial layer. It is subdivided into four sub-arrays of  $64 \times 256$  pixels. The pixel pitch is  $30 \times 30 \mu\text{m}^2$  resulting in an active area of  $7.7 \times 7.7 \text{ mm}^2$ . The layout of the reticle is shown in figure 2. The engineering run was in summer 2006 and the chips were received October 2006. From November to end of 2006, two test setups were prepared in parallel in Strasbourg: a probe station setup preparation for wafers with 14  $\mu\text{m}$  EPI, and a laboratory test setup for circuit tests with 20  $\mu\text{m}$  EPI. End of 2006 to January 2007 the 14  $\mu\text{m}$  EPI wafers were diced and the laboratory tests started.

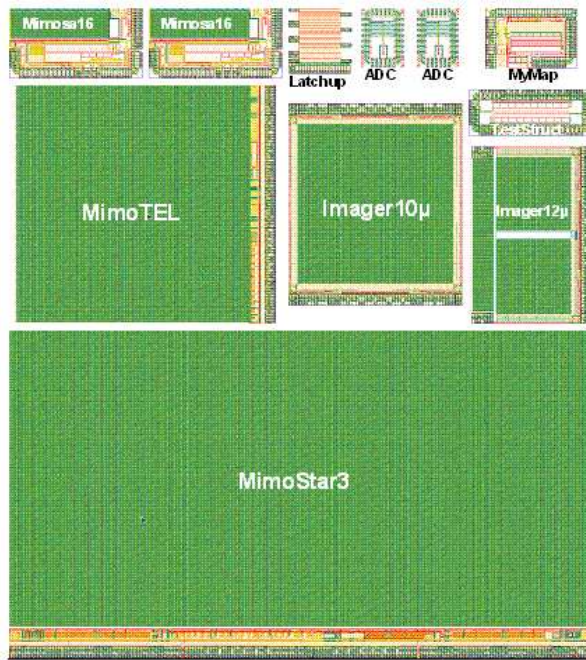


Figure 2: Layout of the reticle of the engineering run AMS-035 OPTO 07/2006 on 14  $\mu\text{m}$  (standard) and 20  $\mu\text{m}$  epi substrate

It was soon evident that AMS did not respect one of the specifications given by Strasbourg: the high-resistivity poly was thinner than desired. This resulted in the DACs biasing being out of range, therefore it was difficult to make the circuit work at nominal conditions. But by rearranging a number of passive components on the sensor boards

this problem could be solved. This problem did not affect Mimosa18, the high resolution sensor for the telescope.

The necessary PCBs to hold the sensors and to refresh the signals traveling from and to the sensor chips were produced in Strasbourg, and populated in Strasbourg and at DESY. By early summer 2007 the PCBs were produced and enough chips were tested to equip the Demonstrator.

### 3 EUDRB (EUDET Data Reduction Board)

The DAQ Card (EUDRB) developed by INFN consists of:

- One mother board, hosting an ALTERA Cyclone II FPGA and the core resources (SRAMs, FIFOs, VME64x interface, trigger port, diagnostic UART). A 32 bit embedded microcontroller (NIOS II) handles tasks like on-board diagnostics, on-line calculation of pixel pedestal and noise (without interfering with data taking operations), and remote configuration of the FPGA via RS-232, VME, and USB2.0. The clock rate of the FPGA is 80 MHz (40 MHz for the NIOS II processor), and the clock rate of the A/D converter is up to 20 MHz.

Functionality of the motherboard includes on-line calculation of pixel pedestal and noise, cluster finding, ADC, remote configuration of the FPGA, and on-board diagnostics.

- One analog daughter card with 4 independent signal processing and digitizing stages
- One digital daughter card, featuring a standard PCI Mezzanine Card interface to the mother board. It drives/receives control/status signals for the detectors and it features a USB 2.0 link.

The EUDRB also implements the interface to the EUDET trigger bus and a VME64X slave interface capable 64-bit MBLT transfers up to 80 MB/s. It is planned to implement 2e-VME transfers for a peak bandwidth of up to 160 MB/s.

The whole system can run in two readout modes:

- Zero Suppressed readout to minimise the readout dead-time while in normal data taking.
- Non Zero Suppressed readout of multiple frames for debugging or off-line pedestal and noise calculations.

#### 3.0.1 Full Frame readout mode:

The card responds to a trigger by sending out a formatted block which includes a header and a trailer identifying the event number, and all raw pixel data for three consecutive frames: the frame being acquired at trigger time, the preceding one and the following one, for a total of 400 kB per board per event. The TRIGGER BUSY is set as soon as the trigger is received and released when data has been transferred to the host PC.

### 3.0.2 Zero Suppressed readout mode:

The card responds to a trigger by sending out a formatted block which includes a header and a trailer identifying the event number and the number of hits. Processing of triggers in this mode does not stop the scan of the detector and therefore no data are lost due to trigger processing. The trigger processing time is at least one frame time. The TRIGGER BUSY is set as soon as the trigger is received and released when data has been transferred to the host PC.

During the test beam operation at DESY and CERN in summer 2007 the functionality of the EUDRBs were fully tested. In the CERN test beam five sensor planes were running simultaneously. The sixth available EUDRB could not be implemented due to problems with the VME crate. Problems with the FPGA programming were solved during these detailed functionality tests.

## 4 Data Acquisition

The main challenge of this telescope is the integration of the different DAQs. The typical telescope users will bring their own DAQ and should not need to invest time in rewriting code or reconfiguring the hardware. A “plug-and-play” system would be desirable. Therefore it was decided to use different hardware and DAQ for the DUT and the reference planes, and to integrate the two systems at the trigger level. Synchronisation will be done with the Trigger, Busy and Reset signals. The readout software, DAQ and data storage for the DUT is provided by the DUT user. The events are then combined offline.

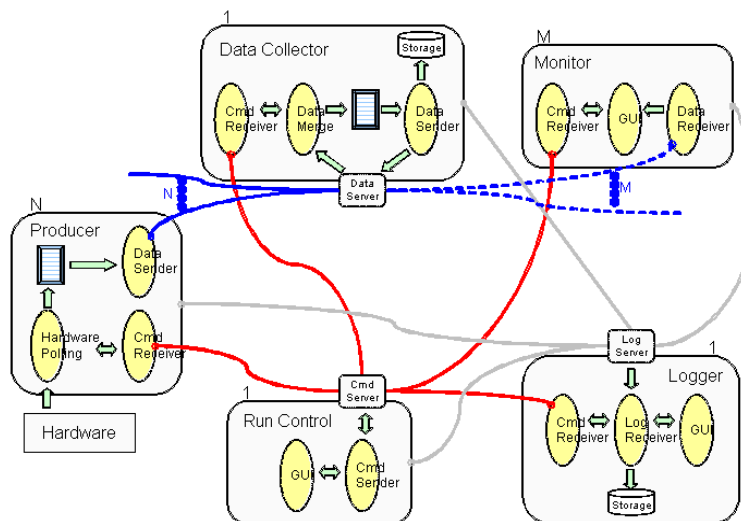


Figure 3: Organigram of the DAQ software.

The basic idea for the DAQ software was to create a simple and easy to use DAQ system for the beam telescope and distributed across multiple computers. The software framework was inspired by the DAQ software written by the DEPFET group in Mannheim and Bonn.

Custom DAQ software was written in C++, using POSIX for threads and sockets. The main Run Control GUI was implemented using Qt, and the Online Monitor uses Root. The whole DAQ software runs on Mac OS X and Linux, but can also be used on Windows (using cygwin).

The organisation of the DAQ software is shown in figure 3. It is highly modular, allowing DUTs to be easily integrated into the framework. This was tested with the first user DEPFET.

One main Run Control controls the DAQ:

- Controls all the other applications

Producers:

- Communicate with hardware and send data to Data Collector

Data Collector:

- Collects and merges data from all Producers

Monitor:

- Receives data from Data Collector for display/statistics

Logger:

- Collects logging messages from all other applications

It was decided to use LCIO/Marlin for data storage and processing. Currently data is transferred internally and stored on a local RAID array in a custom binary format. It is then manually copied to the GRID for conversion to LCIO, and then clustering and tracking is performed.

Now that the conversion has been validated, we can think about writing directly in LCIO, then automating the copying to the GRID and initiation of processing.

In figure 4 screen shots of the DAQ software are shown. A first version was available for the use in the DESY test beam June 2007.

## 5 Mechanics

Based on detailed analytical calculations [1], and also for redundancy and flexibility, it was decided to provide six telescope planes. The telescope will be subdivided into two arms of 3 sensors each, to allow more flexibility without limiting the size of the DUT, which will be located between the two arms. For large DUTs mechanical actuation is

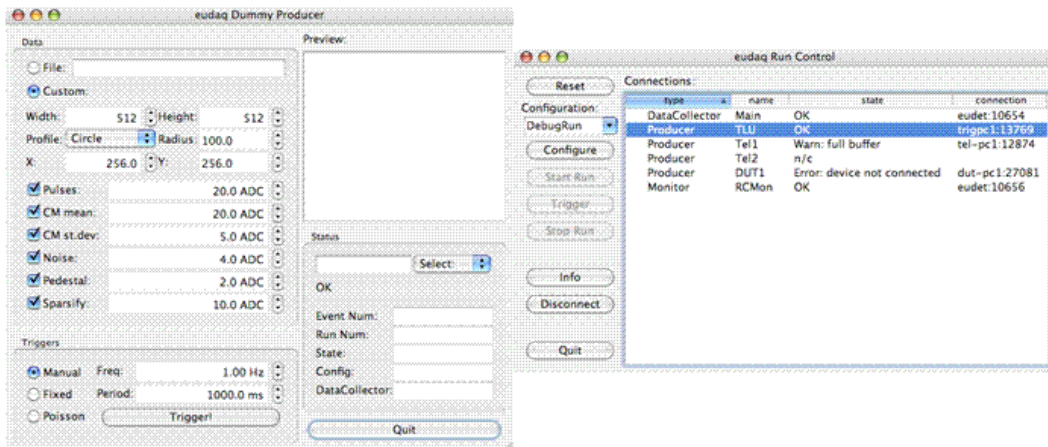


Figure 4: Screen shot of the DAQ software for the DESY test beam.

foreseen in order to move the device through the active area of the telescope. The volumens containing the reference planes will be cooled, DUT cooling needs to be provided by the DUT user. During the CERN testbeam a close to final version of the mechanics was used for the first time. The main problem was the cooling of the sensors, as the thermal resistivity between the cooling and the sensor is too high. An improved version of the mechanics is under way. Apart from this problem, the mechanics were close to final.

## 6 Conclusion and Outlook

This memo summarises the status of the JRA1 Demonstrator at the time of the annual meeting 2007 in Paris. This analog telescope was ready for data taking in summer 2007 and extensively tested at test beams at DESY and CERN. All ingredients necessary for successful data taking are tested and available. Remaining issues to be solved are the optimisation of sensor board supports (L-pieces). Also the readout speed needs improving, mainly in the VME library. And last but not least the software needs improved documentation.

## Acknowledgement

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