



JRA2/SITRA status report 2007

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Abstract

This memo briefly describes the progress made by JRA2/SITRA groups during 2007. First sensors were designed by SiLC collaboration and manufactured by HPK. These sensors were used to construct first module prototypes, populated with special SiLC 130 nm readout chips. The final modules were tested in the lab test bench as well as in the beam test at CERN.

1 Introduction

SITRA is one of the tasks of the Joint Research Activity JRA2 of EUDET. There are 4 participating institutes in the project: HIP, University of Helsinki (Finland), LPNHE, UPMC and IN2P3/CNRS (France), Charles University in Prague (Czech Republic), IFCA-CSIC and University of Cantabria (Spain). Moreover there are five associated institutions: IMB-CNM/CSIC in Barcelona (Spain), Moscow State University and Obninsk State University (Russia), IFIC/CSIC and University of Valencia (Spain) and HEPHY Vienna, Austria.

These institutes, together with many others form the SiLC (Silicon for the Linear Collider) collaboration [1], which is a generic R&D collaboration to develop the next generation of large area Silicon Detectors for the ILC. It applies to all detector concepts and gathers teams from all proto-collaborations. The main goal of SITRA within the EUDET project is to develop and install a test beam infrastructure based on silicon tracking detectors.

2 Sensors

A baseline sensor design has been established to get comparable results from different sensor producers. Since future silicon strip sensors for the ILC will need a very high resolution, a readout strip pitch of $50\mu\text{m}$ is foreseen, possibly with intermediate strips in between, resulting in $25\mu\text{m}$ pitch. Smaller pitch becomes very complicated in terms of wire bonding, contacting the strips with needles for testing but also because of the fact that the charge generated by particles traversing the detector is shared by too many strips reducing the effective S/N ratio.

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This baseline was presented to HPK and it was agreed to order detectors based on this design. 30 sensors have already been delivered by HPK in October, which have successfully passed the QA measurements done in Vienna. Two of them have already been used in a test beam which took place in October this year at SPS at CERN. One can see the masks for the sensors at Fig. 1.

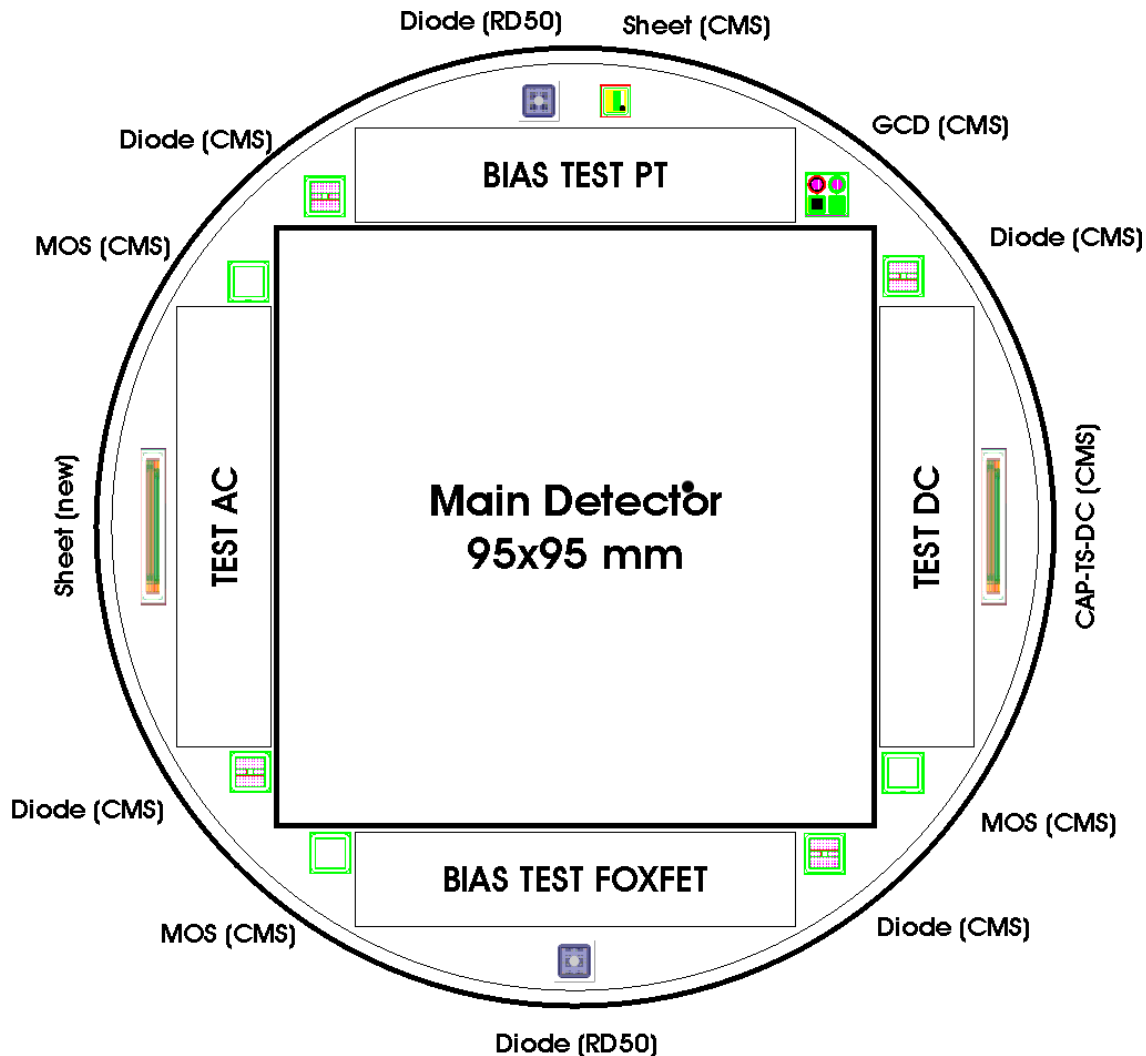


Figure 1: The layout of the Detector designed by the SiLC collaboration together with HPK

One of the goals of the SiLC collaboration is to establish contacts with companies to deliver silicon detectors for future HEP experiments. With this in mind, new fruitful collaborations started with VTT, ON Semi and IET with very promising results, which allows us to go to the next step with these vendors very soon. This helps to establish the procedures, processes and contacts with the producers very early to have a good basis for future steps. Other vendors willing to cooperate in the future have to fulfill the same requirements which these vendors already passed.

Sensor	pitch [μm]	total length [mm]	FE electronics
HPK	50	181	130 nm
CMS	183	283.5	130 nm
CMS	183	283.5	VA1 (reference)

Table 1: Characteristics of the module prototypes and their associated F.E. electronics

The next goals are the development of sensors with dual metal layer structure for in-sensor routing. Together with this, a cheap, industrial bump-bonding technology must be established to take full advantage of this technique. In parallel, sensor producers will be encouraged to build doubled sided detectors, together with evaluation of companies capable of 8" inch or even larger wafers. More details are available at the dedicated EUDET memo [2]

3 Large size prototypes

The sensors obtained were used in the construction of large size silicon strip detector prototypes. This required to set up module construction systems in several laboratories. The first system, used to build modules already in 2006 was set up in IEKP Karlsruhe. Second system was designed and built in LPNHE Paris this year. Wirebonding was performed in a CERN bonding lab.

The large prototypes of silicon structures are designed in an evolutive way. Modules built in the 2008 will be added to the existing ones and tested in the framework of LP TPC project.

Three module prototypes were constructed using various sensor and ASIC combination. They are summarized in the Table 1. Two modules can be seen at Fig. 2.

4 Alignment prototype

Based on the successful experience of AMS-1 and CMS tracker systems, the SiLC has proposed a low-material highly integrated alignment system where the same silicon tracker detectors will monitor the position of a network of IR laser lines, allowing the accurate determination of the relative position of the tracker's sensors [3].

Five sensors out of the batch ordered to HPK have a circular optical window - made by removing the backplane metallization- making them semitransparent to the IR light. These sensors will be part of the "large SiLC tracker prototype" to be built on 2008. They are the baseline for the SiLC alignment prototype. The optical testing of these sensors will be executed in a dedicated test bench at IFCA which is currently being commissioned.

The test stand is placed inside the clean room of IFCA's metrology laboratory. Laser, cosmics and β -source testing of the sensor prototypes will be accomplished; it is equipped with 3 axes motorized linear stages for characterization of large modules, the moving

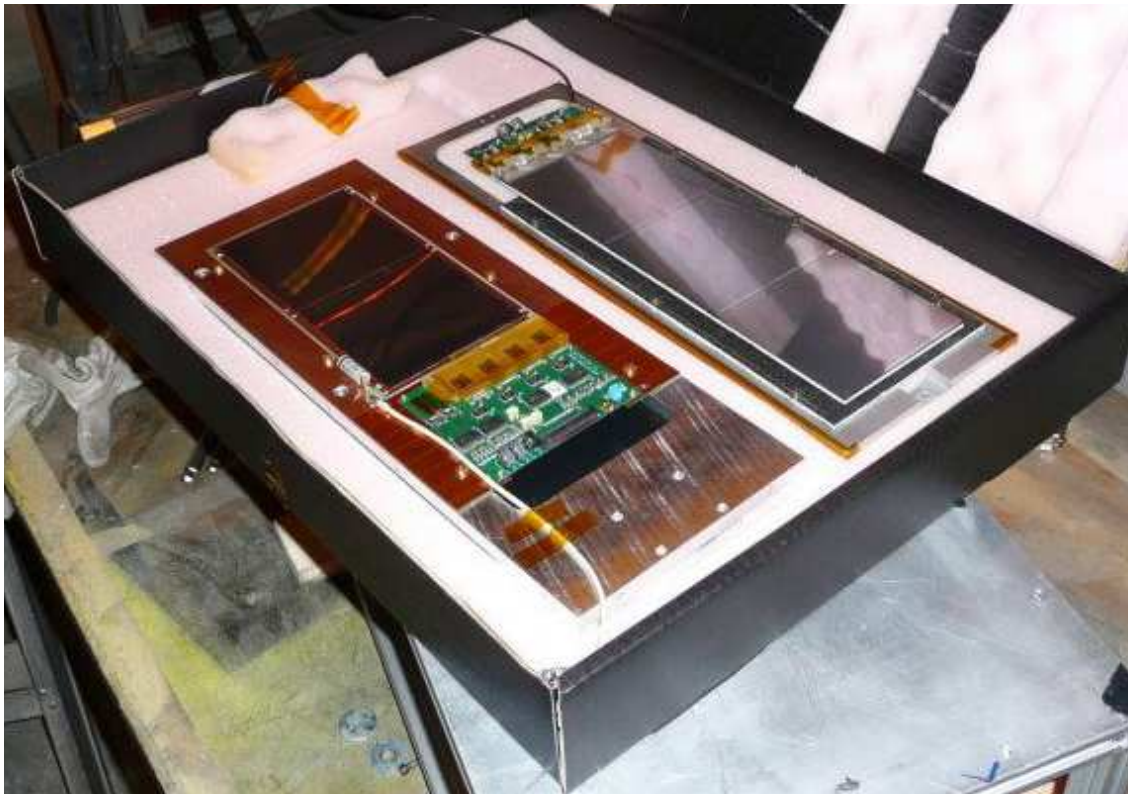


Figure 2: Modules tested at the October CERN test beam

head can scan a volume of 500 mm x 300 mm x 200 mm with a nominal precision of 10 μm . By interferometric techniques we expect to achieve a sub-micrometric accuracy on the moving head.

A second R&D line is currently pursued in parallel to the prototype building. This is a joint project with the Centro Nacional de Microtecnologia at Barcelona (CNM-IMB). The aim of this other activity is to maximize the optical transmissivity of the conventional microstrip sensors without compromising their attributes as particle detector. Thickness of the sensor layers, doping concentrations, strip width vs. pitch ratio, use of semitransparent electrodes are some of the parameters that are to be optimized to increase the optical transmissivity. A very detailed description of this second effort is to be found in [4]. Our goal for 2008 is to probe the accuracy of our optical spectra simulations comparing them to real spectra from especially prepared silicon wafer with different stack structure. Once this is achieved we will produce full "optical friendly" microstrip sensors that could also include the ILC sensor baseline from the point of view of particle detection.

5 Front end electronics

To process the signals from the silicon strips special ASIC is developed by LPNHE Paris and LAPP Annecy. Up to now two 130 nm chips have been designed, the first one being a full digitizing 4-channel version, the second one implementing some blocks required in the final chip, such as calibration, an improved version of the analogue pipeline, a 10-bit digital to analog converter for the generation of internal reference. The architecture of the 4-channel chip is depicted on Figure 3. The motivations for going

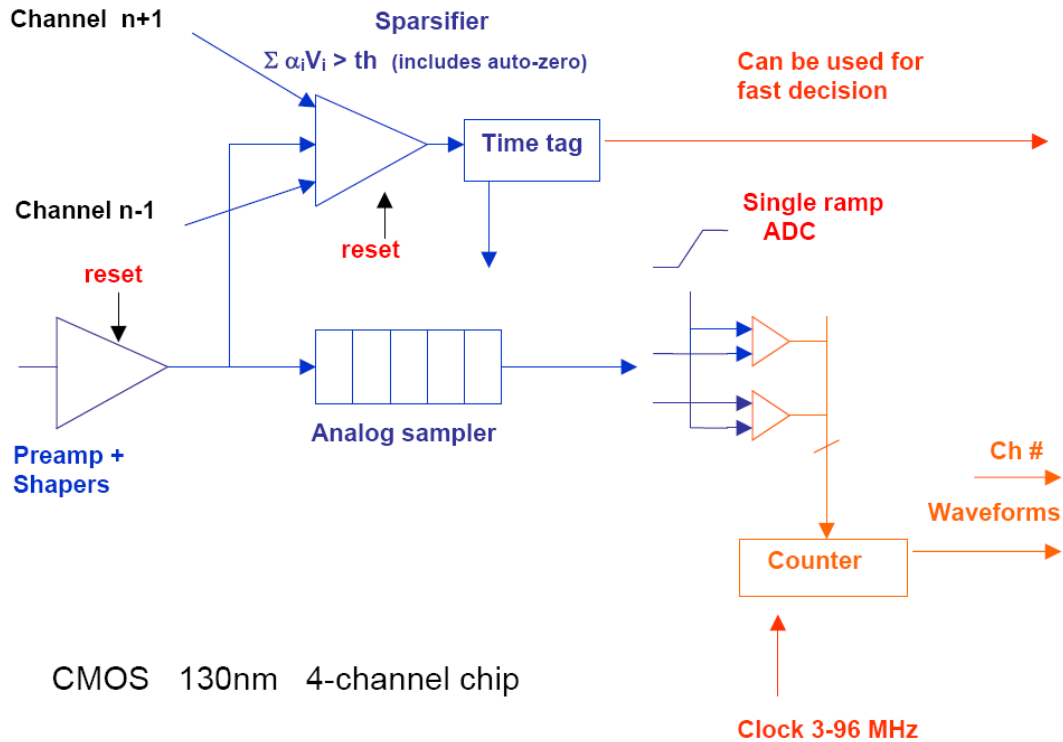


Figure 3: Front-end chip architecture

to 130 nm CMOS technology were to achieve a lower material readout, faster at less power, and better radiation hardness performance (though this is not required at the ILC, but certainly for LHC). Moreover, this technology is presently dominant in the industry. Drawbacks are a reduced dynamic range due to smaller voltage supply range, gate/subthreshold leaks, a longer design time due to more constraining design rules, and more complex models, sometimes not up to date, regarding the noise, in particular.

Although some issues had to be faced with the 130 nm technology, such as unaccurate noise modeling, transistors leakage stray currents, more constraining designn rules, it was possible to implement the two test chips.

Measured performance mainly agree with the simulations, and most of the analog blocks have been validated for the next design. These two 130 nm CMOS designs and first test

results demonstrate the feasibility of a highly integrated front-end for Silicon strips (or even large pixels) readout with DC power under $500 \mu\text{W}$ and Silicon area under $100 \times 500 \mu\text{m}^2$ per channel.

After the two present chips will be fully understood and debugged after radio-active source and beam tests, be compared to the LSB value of $250 \mu\text{V}$. Power is 30 mW per channel, for the chosen biasing point. Some unexpected features such as gain differences between channel, that may be due either to channel to channel differences in the input calibration capacitance values (traces on PCB), or damages to the chip due to the FIB process remain to be understood. All blocks will be merged to build a 128 channel version in 130 nm CMOS. This design is expected to be submitted to the foundry in the beginning of 2008. More details can be found at a dedicated memo [5].

6 Lab test bench

In order to test the functionality of the sensor and chip prototype lab test bench system was designed and built on LPNHE Paris and LAPP Annecy, with the helps of Barcelona University. The system consists of specially designed FPGA cards programmed in the VHDL, power supplies, USB interface to the PC, etc. The card can be seen at the Fig. 4.

7 Beam tests

Further performance evaluation has been done at the two SiLC/SITRA beam tests. One was held in June in DESY. The second beam test took place in October 2007 at the SPS accelerator at CERN (H6). Here modules were placed in the specially designed Faraday cage and tested in the beam of 120 GeV pion beam. The beam position was monitored by the set of EUDET telescopes [6] (see Fig. 5).

The detailed analysis of the beam data has only started. First results show a clear response of new module to the beam particles (see Fig. 6).

The SiLC/SITRA collaboration has made a great progress towards the fulfilment of all commitments of the EUDET project during 2007. The detailed discussion of individual deliverables is beyond the scope of this memo, but it can be found in the EUDET annual report.

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Figure 4: DAQ readout card for the 130 nm chip

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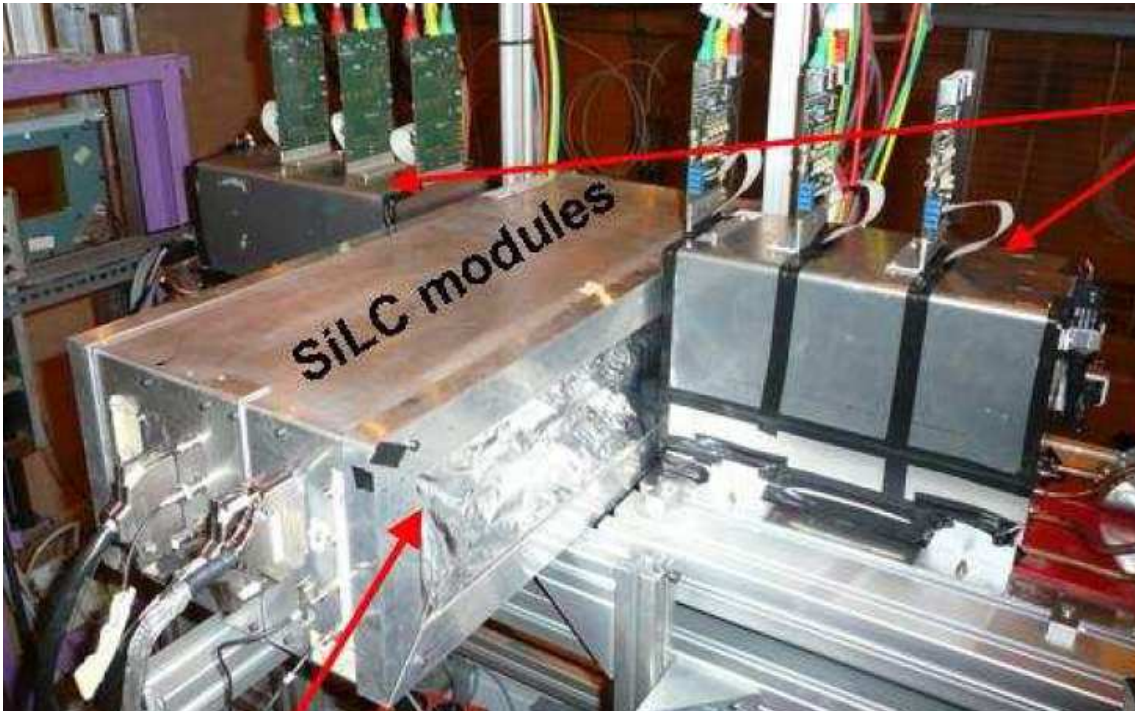


Figure 5: SiLC modules in the insulating frame positioned between the EUDET telescopes during the 2007 CERN test beam

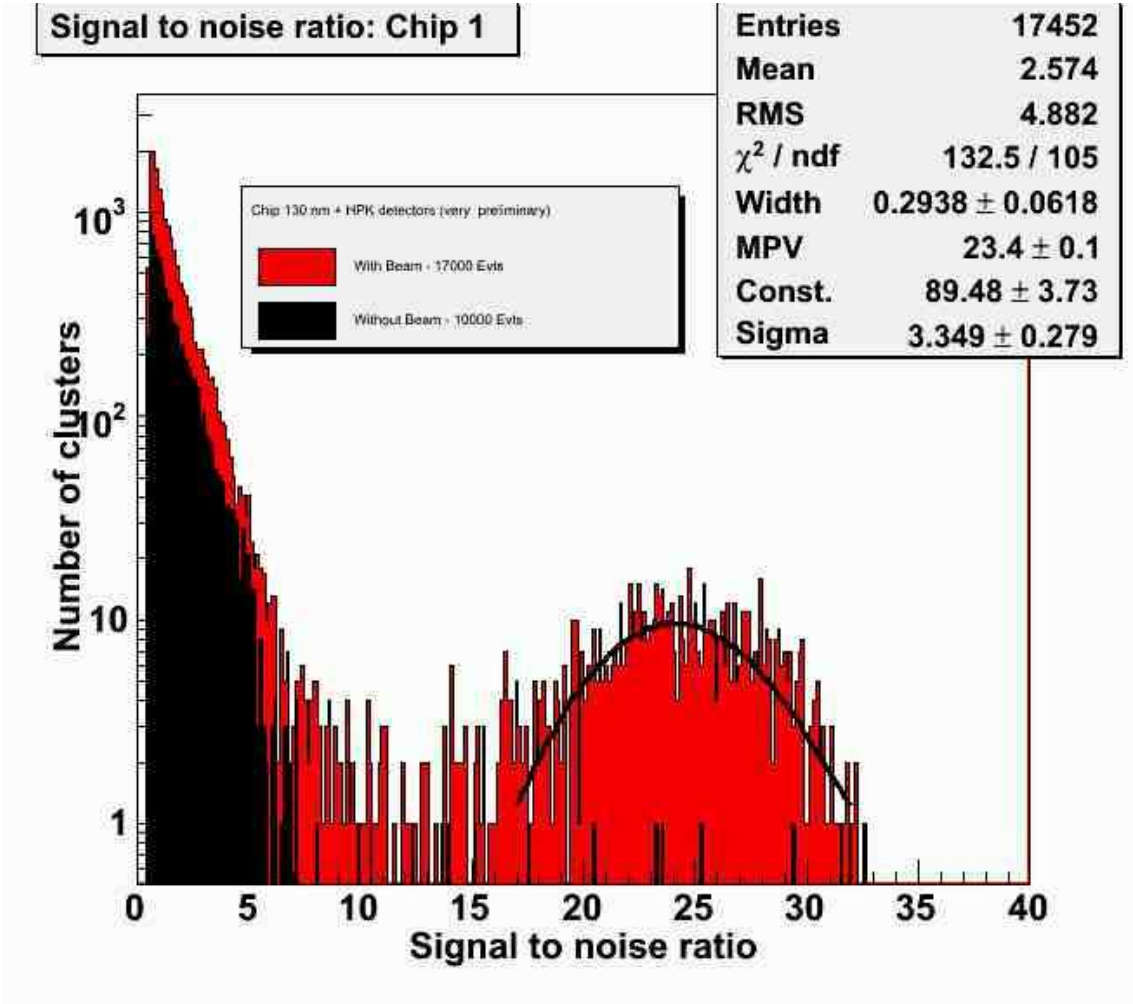


Figure 6: Amplitude spectrum of the HPK-130 module at the CERN beam test