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Status of the TLU v0.2

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Abstract

Experience gained by using the TLU during the 2009 beam-test season is summarized. Firmware has been enhanced, including the addition of synchronization pulses, reset pulses and the eight-fold increase in the timestamp resolution. The hardware has been enhanced by the addition of a clock generator board and the upgrade of the photo-multipler power supply boards to include a I^2C DAC.

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1 Beam Test Experience

The TLU was used in the JRA1 beam-test infrastructure at CERN. Many new firmware features introduced to support (s)LHC users. Unfortunately this lead to number of significant "regression" in firmware, which inconvenienced a number of users. The most serious of these bugs resulted in incorrect trigger numbers being resported to the device under test. Testing and bug fixing underway. Users are asked to report problems using the Hepforge issue tracker at `http://projects.hepforge.org/eudaq/trac/report`

2 Hardware Enhancements

2.1 Clock Generator

The latest TLUs have incorporated a clock generation board based around a Texas Instruments cdce949 device[1]. The board produces two TTL and two LVDS clock outputs. The frequency is controllable by I2C (settings are stored in EEPROM). Clock either produced from crystal or input from front-panel. The board can be retrofitted to existing TLUs, but this necessitates replacement of the front panel.The new front panel also has mounting for LVTTL general purpose I/O connector. A circuit schematic of the board can be found online at `https://svn.phy.bris.ac.uk/svn/uob-hep-pc017a/trunk/www/Schematics/pc017c_clock_board.pdf`

2.2 Photomultiplier Power Supply

In the latest TLUs, the 15V supply for photo-multiplers has been upgraded The new board includes an adjustable 0-1V control voltage controllable via an I^2C interface). The updated board can be retrofitted to existing TLU v0.2 (no new front panel required). The 2-pole Lemo connectors have been replaced with 4-pole Lemo wired to "DESY standard". More details can be found in the updated TLU manual[2].

3 Firmware Enhancements

3.1 Synchronization

One user (TimePix) requested a periodic synchronization pulse to act as a "shutter". The pulse period is in the region of 10Hz - 1kHz. This has been implemented as a LVTTL signal on a single pole 00 lemo connector on the front panel. Pulse width and repetition frequency set terms of clock cycles. The synchronization pulse is "armed" by writing to width/frequency registers and starts running when timestamp reset.
Resetting the internal time-stamp results in a pulse on the reset line of active DUTs. This allows the DUT to set "time-zero" and match the TLU timestamps with its own internal timestamps.

3.2 Reliability and Debugging Enhancements

The timestamp block transfer firmware has been completely rewritten. Instead of initiating a separate transfer for each block of timestamps the TLU continuously reads out the timestamp buffer. This, together with improved error detection software results in considerably more reliable timestamp transfer. The new firmware must be used with new DAQ software (TLUProducer.exe , TLUControl.exe).
In order to ease debugging, more information is avaialable about the finite state machine behind each DUT connection.

3.3 Trigger-only handshake-mode

In this mode the TLU issues fixed length trigger pulse to DUT, ignoring the state of the BUSY line. Mode selectable on DUT-by-DUT basis (i.e. it can be mixed with normal TRIGGER/BUSY handshake).

3.4 DUT Initiated Busy

There is an option for DUT to initiate "busy" state by raising DUT_CLK line outside a trigger/ busy handshake sequence. This option can be selected on a DUT-by-DUT basis (by default it is disabled). With previous firmware the DUT could indicate busy by rasing its busy line outside of a trigger/handshake sequence. However, this gave a race condition where DUT raising BUSY and then thinks it has suspended triggers and simultaneously TLU sends trigger and thinks that BUSY is raised in response.

3.5 Timestamps

Time-stamp precision has been increased from a single clock cycle (20.8ns by default) to 1/8 clock cycle (2.6ns) Accuracy isn't as good as this - bins not equal size due to timing skew between different derived clocks.

3.6 Trigger Masks

Existing AND-Mask and Or-Mask work as before. Howeverm it is now possible to write a 16-bit number that defined what combination of inputs will result in trigger. For example if it is required that the trigger fires if inputs 0 and 1 have a signal, but inputs 2 and 3 do not, then bit "0011" = 3 of the trigger word should be set. There is also a second, independent, trigger connected to scaler. This can be used for e.g. estimating the efficiencies of the trigger scintillators.

4 Firmware Plans

The firmware needs a substantial tidy up. For example, the code for interface hardware (EZ-USB chip) completely mixed with TLU specific code. It should be factorized to

make it easier to add new modules. Factorization will also allow the EUDET specific parts to be released under the GPL. Tidying up the code should make it easier to run simulations and hence result in fewer bugs in released code. Regardless of code reorganization existing bugs need to be identified and removed.

5 Conclusion

A significant number of new features were introduced for the 2009 beam-test season. This took effort away from debugging existing code and lead to a number of serious regressions. Available effort is now concentrated on bugfixing. Once TLU firmware/software is stable again, will move towards prototyping a "tagging mode" with existing hardware.

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References

[1] Texas Instruments, "Programmable 4-PLL VCXO Clock Synthesizer with 1.8V, 2.5V and 3.3V LVCMOS Output (Rev. C)", October 2009

[2] D. Cussans, "Description of the JRA1 Trigger Logic Unit (TLU), v0.2", EUDET-Memo-2009-04