JRA2-SiTRA: NEW VERSION OF THE MIXED MODE SILICON STRIP FRONT END AND READOUT ASIC

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Abstract

A new prototyped version of the SiTR_130 chip has been achieved end of 2008 to process the signal from 88 strips and was tested in 2009. The goal of this work is to pursue developing this Front-End and Readout chip for the Silicon strips at the ILC able to equip larger size Silicon prototype than those currently built for the EUDET project. The goal is to achieve the handling of at least 128 channels and improve further the digital treatment of the information with implementing full programmability, flexibility, fault-tolerance for use in a large scale beam test infrastructure. A new version is being designed for 2010, able to treat 128 channels.
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1. Introduction

A new 130nm CMOS version with 88 readout channels including sampling and analog-to-digital conversion (ADC) has been developed and is currently under testing. In order to reduce material budget, integrate more channels and improve radiation hardness, we decided to use the Deep Sub Micron (DSM) integrated technology selected for the previous prototype and proven by it. The technology used in both cases is the 130nm CMOS technology provided by the United Microelectronics Corporation (UMC) in Taiwan .

Each channel comprises *i)* a low-noise charge preamplifier with a 30mV/Minimum Ionizing Particles (MIP) gain, *ii)* a pulse shaper operating between 0.5 and 2 microseconds peaking time (shaping time) in order to match various detectors lengths and readout conditions, and *iii)* a two dimensional structure of 8x8 analog sampler which allows storing up to eight successive events with eight samples per event. The latter is triggered by a sparsifying analog section, summing three adjacent channels from the output of the shaper. Finally, all the samples are converted by a 12-bit parallel ADC. All the bias conditions of the circuit are controlled by a set of digital-to-analog converters (DAC) where the typical analog values are found in the middle of the digital range. Finally, the digitized sample is serially read out in 40-bit data words containing charge, time, channel and event information. The static consumption of the chip is simulated at 1.1mW per channel in the active mode and 145µW per channel in the power down mode.

The chip is designed to match the timing at the International Linear Collider (ILC) machine where collisions and data taking occurs every 337 nanoseconds during a train of one millisecond, followed by a 200 millisecond idle time. Digitization and readout are performed just after the end of the collision train. Once the data is read out, all the bias currents are lowered in order to reduce power consumption.

1. Architecture

During data taking, the analog signal is sampled continuously. Up to the decision, the pulse is stored in the 8-deep analog-pipeline. The second dimension allows storing up to eight events per channel.

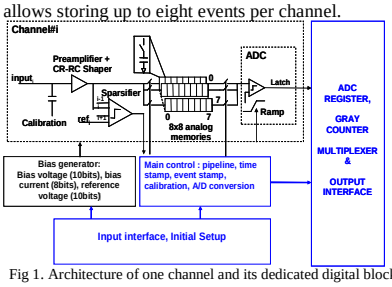

Fig 1. Architecture of one channel and its dedicated digital block.

The digital implementation allows initializing all the bias conditions of the circuit. This part controls the functionality of the analog-pipeline, the recording of time, channel and event information, and the analog-to-digital (A/D) conversion. The architecture of one channel and its dedicated digital setup is depicted in Figure 1.

2. Building blocks

2.1. Analog part

The analog part benefits from the successful results of the previous version [1], [2], [3], [4] and therefore it presents no major changes in the preamplifier, shaper, sparsifier, and ramp ADC architectures.

An 8-deep analog memory is run continuously as a circular buffer during data taking with a programmable write clock with a frequency that can be set to 1.5, 3.0, 6.0, or 12.0 MHz. Based on the decision received from the sparsifier, the clock frequency can switch to 3.0, 1.5, 0.75, or 0.325 MHz (after several clock cycles). These slow frequencies are chosen in order to match the slow falling edge of the signal [Fig. 2]. The analog signal is subsequently redirected to another analog-pipeline, and this

process is repeated itself until the eight buffers are filled.

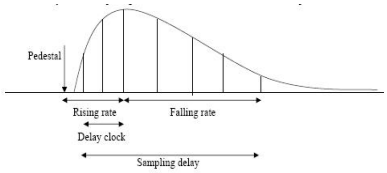

Fig 2. Sketch of the four parameters which control the sampling of the analog-pipeline for the pulse height reconstruction.

At the end of the collision train, each analog sample is converted by a 12-bit ADC in 85 microseconds. To convert all the analog samples, this operation is repeated 64 times. Once finished, the chip is set to minimum consumption (idle phase) and stands by until the next acquisition cycle begins.

A bias generator block controls all the bias currents and voltages of the circuit. There are two programmable values assigned to each bias current, one for active mode and the other one for the power down mode. The latter value corresponds to a small, non-zero current, such that the switching time between the two modes is optimal. Moreover, as the sparsifier is sensitive to the variation of the input offset of its comparator, the sparsifier threshold for each of the 88 channels is adjusted individually between two common high and low references via a 4-bit DAC.

2.2. Digital part

The digital part could be divided into three main blocks: Control Interface, Main Control and Output Interface.

The Control Interface block receives the initializing data serially, and stores all the information on bias conditions and other chip-operation options in 98 10-bit registers. The minimum time required for filling all the registers is about 40 microseconds (using a 48MHz clock).

The Main Control block controls all the circuit logic needed for the acquisition and conversion of the signal. It switches among four states: *Idle*, *start_pipe*, *write* and *read*. In the *Idle* state, the chip is inactive and waits for the acquisition signal indicating the beginning of the bunch train. In the *start_pipe* state, the analog-pipeline is activated and reset. Next, in the *write* state, the analog signal at the output of the analog shaper is sampled and stored in the analog-pipeline once a trigger from the sparsifier is received. The *write* state is maintained until all the event buffers are filled, or until the circuit receives the signal announcing the end of the bunch train, whichever comes sooner. In the *read* state, all the samples are converted and sent to the output. The circuit then goes into *Idle* state and waits for a new collision cycle.

Finally, in the output interface block, during each 85 microsecond conversion interval, the 40-bit word is performed, serialized and sent to the output. Beside the 12 bits of charge information and the 16 bits of time information, 7 bits of channel number and 3 bits of event number are also associated

Finally, in the Output Interface block, during each 85 microsecond conversion interval, the 12 bits of charge information and the 16 bits of time information are associated with 7 bits of channel number, 3 bits of event number, and 2 parity bits to form a 40-bit word which is serialized and sent to the output.

3. Implementation

The silicon area of the chip is 10x5mm^2, with the analog part occupying a surface of 10x3.5mm^2, and the bias generators (DACs) occupying an area of 1mmx300μm. The remaining space is filled by the digital part.

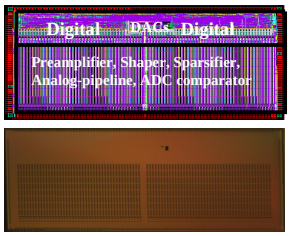

Fig. 4. The layout and photograph of the chip

4. Preliminary results and conclusion :

The first tests of the chip indicate that the static consumption is about 1.35mW/channel. With a gain of 43mV/MIP and 2.6% of nonlinearity, the output of the shaper of the 88th channel (test channel) is linear up to 24 MIPs at the input.

This chip presents a highly performing digitized FEE, fully programmable, with a high processing capability, and a high degree of fault tolerance and flexibility. Comprehensive testing of this device is underway.

Acknowledgments:

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