JRA3 Hadronic Calorimeter

Technical Design Report

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Abstract

A first comprehensive proposal for the Analogue Hadronic Calorimeter (AHCAL) for the ILC has been presented and discussed during the EUDET annual meeting 2007 in Paris. In this short memo, the technical design of the AHCAL is presented, with emphasis on electronics integration, as well as future milestones and component prototypes that are foreseen within the EUDET infrastructure initiative for ILC detector R&D.

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1 Introduction

The basic structure of the Analogue Hadronic Calorimeter (AHCAL) is shown in Fig. 1a. The *AHCAL Half Sector* consists of 38 detector layers (current status). Each layer is subdivided into subunits, called HBUs (*HCAL Base Unit*), of which always 6 in a row form an *AHCAL slab*. Two Half Sectors form the AHCAL Sector (=Octant), of which 8 pieces are combined to a circular structure. Two of these structures next to each other containing in total 16 sectors are combined to the AHCAL barrel, shown in green colour in Fig. 1b. The AHCAL barrel is located between the electromagnetic calorimeter (ECAL, blue colour in Fig. 1b) and the magnet coil (purple colour in Fig. 1b).

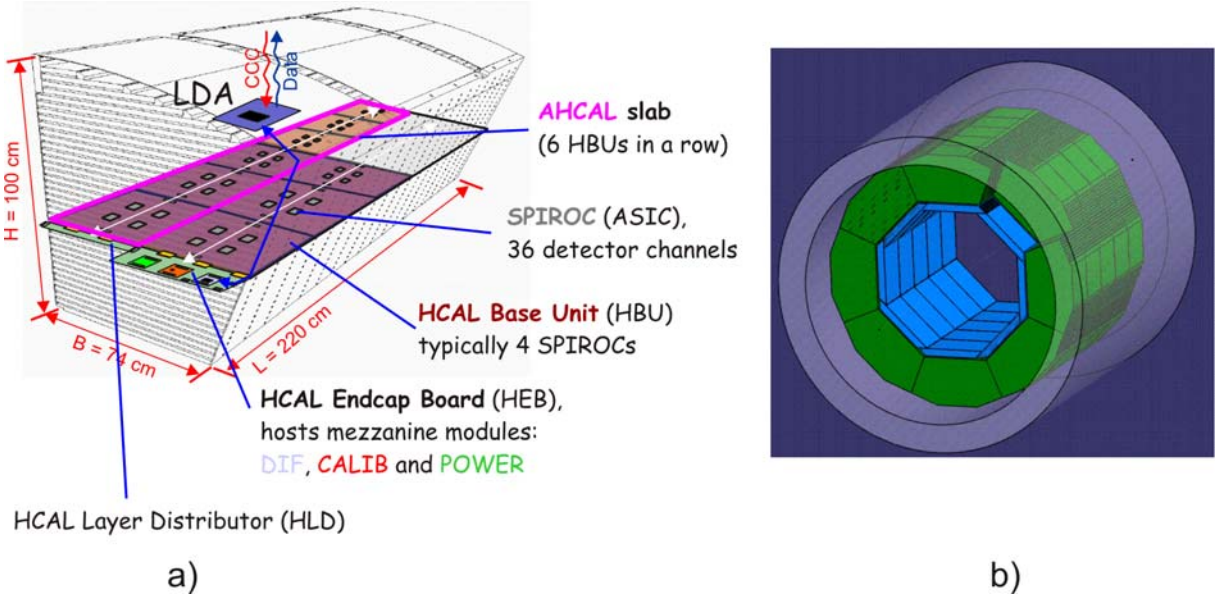


Fig. 1 : Structure of the AHCAL detector and its interface to the DAQ via the boards HEB and LDA (a). A detector layer of an AHCAL half sector can be filled by 2 or 3 AHCAL slabs, depending on its mechanical dimensions. Two Half Sectors form a Sector, of which 2x8 are combined to a full AHCAL barrel (b, green colour). The AHCAL is surrounded by the magnet coil (purple colour) and has the electromagnetic calorimeter (ECAL, blue colour) inside.

At the AHCAL end face (the end of the absorber structure), the boards HEB (*HCAL End Board*) and HLD (*HCAL Layer Distributor*) enable the electrical interconnection to the inner detector electronics. The HEB, that also hosts the DIF, the *detector interface* to the DAQ, is supposed to have the same size for all layers, while the HLD changes in size from layer to layer.
Additionally to the DIF, the HEB also hosts the AHCAL specific subgroups CALIB (control of the calibration system) and the POWER-and-Monitoring subgroup that provides power to the AHCAL and operates the voltage- and temperature-monitors (Fig. 1 bottom side).

2 Mechanical Design and Analysis

The design of the absorber structure minimizes the amount of dead material which would compromise energy resolution and pattern recognition capabilities. There are no spacers in the active detector area, the absorber plates are supported only by a 3mm steel sheet at the boundary to the neighbouring sector. This guarantees that a maximum area in the gap can be instrumented with active elements, and a modular structure with easy insertion and removal of the layers can be realized, which facilitates assembly and maintenance.
Using finite element methods first analyses of the mechanical stability of this ambitious design have been started within the I3. Depending on the fixing points of the AHCAL Half Sectors and their

position within the barrel, the bending of the absorber plates can be calculated as shown exemplarily in Fig. 2.

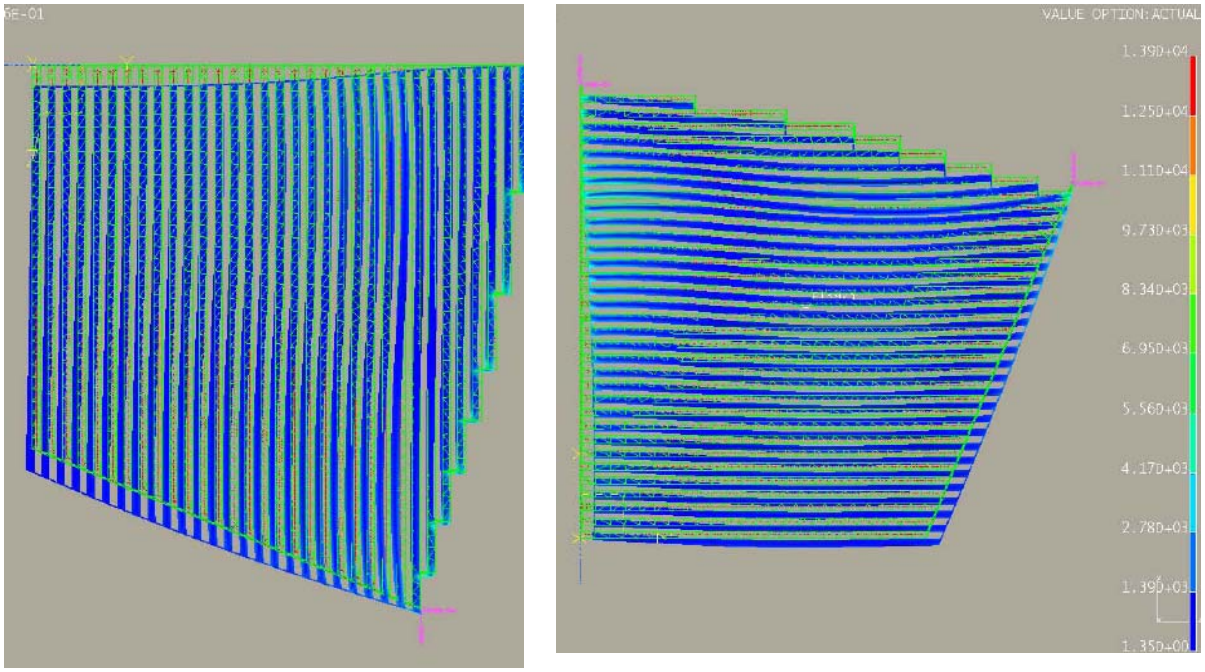


Fig. 2: Bending of the absorber plates of a AHCAL Half Sector for one of the proposed fixing schemes.

The results confirm the intrinsic stability of the module if suspended in different orientations. Next, the fixations of the structure components to each other need to be optimized, and the support of the overall ring structure in the complete detector must be defined in cooperation with detector concept groups in the ILC community.

3 Front-End ASIC SPIROC

The front-end ASIC SPIROC has also been developed within this JRA and is documented in detail in [1],[2]. It collects the analogue signals of the MGPDs (**M**ulti-pixel **G**eiger mode **P**hoto **D**iode [3]), digitizes the amplified and shaped signals and transfers the digital results together with a timing information per channel with respect to the ILC bunch structure to the DAQ. Main features of the SPIROC are:

- 36 input channels with 5V-DACs for channel-wise adjustment of the MGPD bias voltage.
- shaping time between 50ns and 100ns.
- two gains enabling a dynamic range for charges between 1 and 2000 photo-electrons equivalent.
- all channels with a threshold adjustable self triggering logic.
- time measurement with respect to bunch structure by 12-bit TDCs (100ps per bin).
- 12-bit ADCs on chip.
- low power: 25µW per channel in ILC power pulsing mode.

4 AHCAL Detector Layer, -Modules

The AHCAL barrel with the 38 layers in the 2 x 8 sectors will contain more than 2,400,000 detector channels (scintillator tiles). A typical layer of a sector covers an area of 0.9x2.2m² and with a tile size of 3x3cm² more than 2200 tiles. The detector electronics of each layer will be subdivided into subunits (HCAL Base Unit, HBU), while several constraints from the barrel's mechanical boundaries, as well as restrictions from electronics production and assembly define the HBU size and the number of channels (tiles) per HBU.

The widths of the AHCAL detector layers are not constant but increase from layer to layer by about 1cm (c.f. Fig. 1). Therefore, also the widths of the layer detector modules (HBUs) and the number of channels per slab are not constant. Table 1 shows the different types of HBUs that are necessary to fill an *AHCAL Half Sector*.

Layer Width [tiles]	**HBU width [tiles]**	**HBU depth [tiles]**	**Channels (tiles) per HBU**	**No. of SPIROCs per HBU**	**Unused SPIROC inputs**	**No. SPIROCs per slab** (in readout chain)
24	12+12	12	144 / 144	4 / 4	0/0	24 / 24
25	8+8+9		96 / 96 / 108	3 / 3 / 3	12/12/0	18 / 18 / 18
26	8+9+9		96 / 108 / 108	3 / 3 / 3	12/0/0	18 / 18 / 18
27	9+9+9		108 / 108 / 108	3 / 3 / 3	0/0/0	18 / 18 / 18
28	8+8+12		96 / 96 / 144	3 / 3 / 4	0/0/0	18 / 18 / 24
29	8+9+12		96 / 108 / 144	3 / 3 / 4	12/0/0	18 / 18 / 24
30	9+9+12		108 / 108 / 144	3 / 3 / 4	0/0/0	18 / 18 / 24
31	9+10+12		108 / 120 / 144	3 / 4 / 4	0/24/0	18 / 24 / 24
32	8+12+12		96 / 144 / 144	3 / 4 / 4	12/0/0	18 / 24 / 24
33	9+12+12		108 / 144 / 144	3 / 4 / 4	0/0/0	18 / 24 / 24

Table 1: Definition of the different types of HBUs that are necessary to fill the layers of an AHCAL Half Sector. The unit 'tiles' refers to the width of 3cm of the foreseen 3x3cm² scintillator tiles. While the HBU depth is constantly 12 tiles (=36cm) in order to fill the 220cm barrel depth by 6 HBUs in a row, the HBU width (8, 9, 10 or 12) and the number of slabs per (half-) layer (2 or 3) vary.

The left column of Table 1 depicts the Half Sector layer width. The smallest layer closest to the beam is 74cm wide (cf. Fig. 1), which is in unit 'tiles' (1 scintillator tile is 3x3cm²) about 24. The second column shows the width of the HBUs (=width of slab), by which the layer could be filled, again in the unit 'tiles'. The HBU depth is always 12 tiles (3rd column), in order to fill the 220cm barrel depth by 6 HBUs in a row. The fourth, fifth and sixth column show the number of resulting detector channels, SPIROCs per HBU, and number of unused input channels per SPIROC, respectively (the SPIROC has 36 input channels). The last column shows that the readout chain (number of SPIROCs per slab) varies from layer to layer, which has to be taken into account in the DIF design.
Intermediate layer sizes (e.g. 76 cm width) that do not fit into the 3-cm tile-size grid are proposed to be filled with modules of the next larger layer (78cm width corresponds to 26 tiles) that are especially shortened. The last row of tiles will have 2cm or even more precisely adapted width, and the HBU printed-circuit board must have a lay-out which allows to trim its transverse size..

4.1 HCAL Base Unit (HBU)

Due to the large area of the AHCAL detector layers, a subdivision of the electronics into subunits, the so called HCAL base units (HBUs) is proposed. Main task of the HBUs is the integration of scintillating tiles with MGPDs together with front-end electronics (SPIROC ASIC) and the light calibration system. Additionally, the HBU enables the operation from (interface to) the DAQ.

The size of the HBUs reflects a compromise between the numbers of modules that have to be handled during the AHCAL installation and the feasibility of the module's production concerning PCB-size, the stability during the HBU assembly and transport and requirements from the barrel's mechanical boundaries:

- The HBUs should be as large as possible in order to keep the AHCAL assembly time small.
- The HBUs should be as thin as possible in order to enable the smallest possible magnet diameter.
- The HBU should enable easy de-/installation of single units if a replacement is needed.
- The HBUs must enable the AHCAL assembly for all sector orientations (see Fig. 1b). Up to now it is not clear if a rail system is needed, or if the assembly can take place with the support of the sector walls.
- The HBU design must consider an optimization of the dead area by minimizing the gaps between the scintillating tiles.

In order to reduce the AHCAL assembly time, several HBUs can be combined to 'layer-modules' – cassettes with electronics interfaces - before assembly into the absorber stack. The possible layer module's size depends on the available space in front of the calorimeter structure and the cabling of other detector components. Quality control and initial calibration using test beams can be performed with modules or even with HBUs stacked in a light aluminium structure.

4.1.1 Detector Layer (HBU) Cross Section

The proposed setup of an AHCAL detector layer, that is defined by the HBUs and the absorber plates, is shown in the cross sectional view of Fig 3a. The HBU cassette is formed by top- and bottom steel plates that are produced from the same material as the absorber plates.

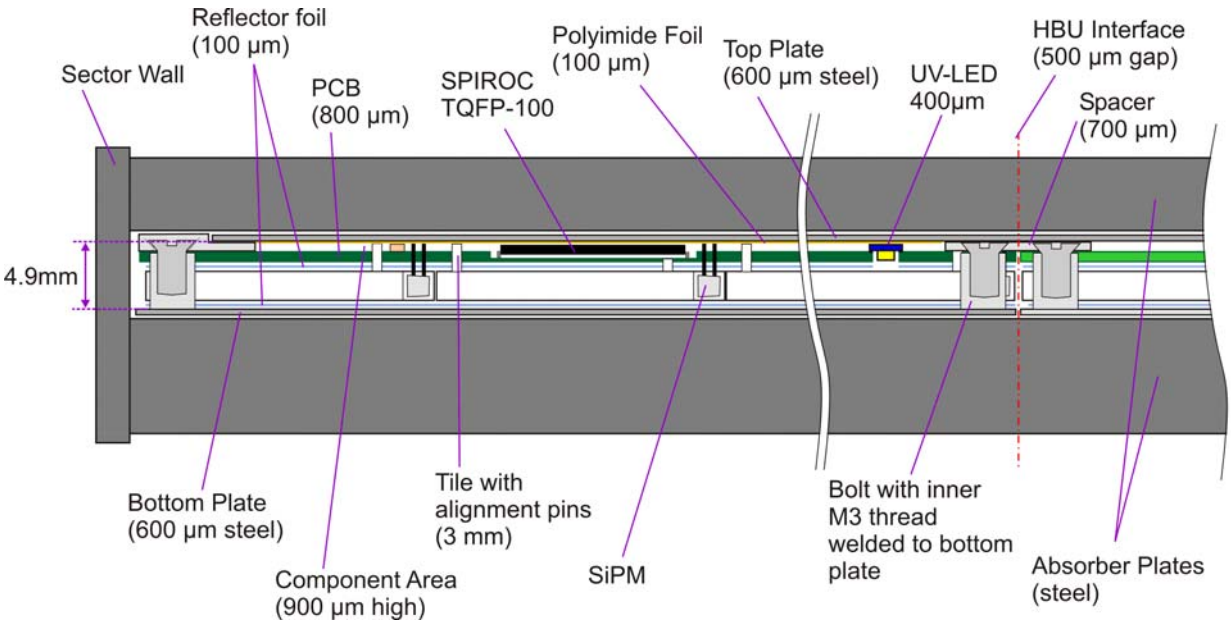


Fig. 3a: Cross sectional view of a AHCAL detector layer (HBU and absorber plates). The distance between the edge-tiles of two adjacent HBUs is supposed to be between 500µm and 1mm. The component area on top of the PCBs is 700µm, additionally there are 100µm for the polyimide foil and 100µm safety margin. The total height of the HBU results in 4.9mm excluding the top- and bottom plate (absorber material).

The scintillating tiles are positioned below the PCB by their alignment pins, which are plugged in respective holes of the PCB during HBU assembly. The alignment pins ensure proper placement of the photo-sensor contacts on the PCB while maintaining their position relative to the wavelength shifting

fibre, even if realistic tolerances of the tile sizes are taken into account. The production of such tiles (see Fig 3) using low-cost injection moulding technology has been developed at the associate institute ITEP, Moscow. The group plans to test the performance of their tile MGPD systems in the JRA3 infrastructure. Other schemes of scintillator positioning and photo-sensor contacting are also being disused in the community and can be integrated with minor modifications to the HBU design.

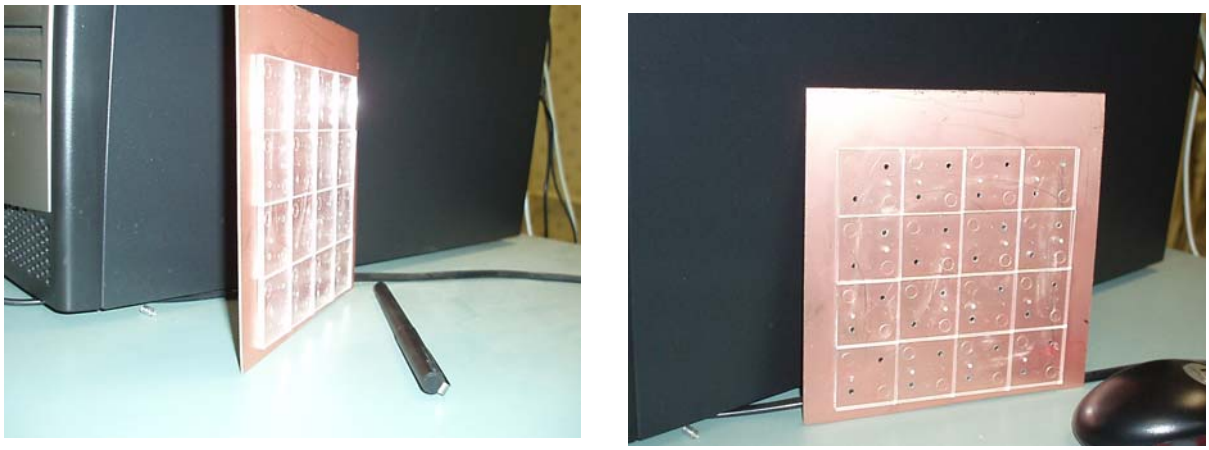


Figure 3b: Scintillator tiles with alignment pins fixed to a PCB (courtesy V.Rusinov, ITEP).

The contact pins of the MGPDs (SiPMs) are plugged in the same way into the PCB and are soldered from the PCB's top side. The scintillation light is kept inside the tiles by layers of reflection foils below and above the tiles. All electronic components are assembled automatically (reflow) on the PCB's top side. For a height optimization, the ASICs and connectors (not shown) are placed into cut-outs of the PCB. Below the top plate of the cassette, a polyimide foil prevents shorts between the electronics and the steel cover. One possible concept of the light calibration system is to have one UV-LED per tile that is placed up-side-down onto the PCB. The LED radiates its light through a hole in the PCB and reflection foil into the tile. In the four corners of the HBUs, a bolt with an inner M3 thread is welded to the bottom plate. The top plate can be fixed together with the PCB and an adapter by screws to the bolts. Gluing techniques are also being considered. The detailed design has to take the testing and commissioning procedure into account.

4.1.2 Printed Circuit Board (PCB) of the HBU

The HBU PCB has six metallization layers in a thickness of 800µm. Two layers enable impedance controlled routing (50Ω), a third layer can be used for short, digital signals. Three power layers form a EMC-suitable power ground system. For standard sized HBUs with 144 channels, the PCB has outer dimensions of 36x36 cm², while for larger HBUs the length of 40cm should not be exceeded. The PCB thickness is for all HBUs 800µm.
In order to minimize the HBU height, ASICs (SPIROCs) and connectors are assembled into cut-outs of the PCB. Two companies already agreed on the proposed setup at reasonable costs. The resulting cross section of the PCB is shown in Fig. 4 (current proposal).

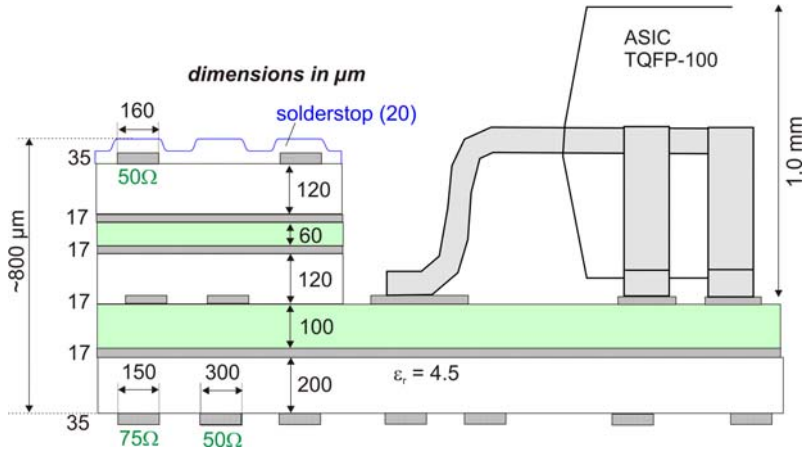


Fig. 4: Cross section of the proposed HBU PCB. The six-layer design has three routing layers, of which two can be impedance controlled. ASICs and connector are assembled into cut-outs for a HBU height optimization.

4.1.3 Future Integration Plans

In 2008 two test board setups will show the feasibility of the proposed concept.

1. A HBU prototype with presumably 144 channels and four SPIROC prototype ASICs will be used to test the integration of scintillating tiles with MGPDs, PCB, ASICs and light calibration system, the assembly of the cassette (mechanical construction) and the performance of the electronics in the dense HBU setup. The HBU prototype is operated with the future DAQ.
2. A layer-module setup will be used to analyse the performance of the setup in slabs of 2.20m length. Besides signal impairment on the long traces, the switching of the power supplies for an ILC-mode operation shall be tested.

5 Calibration and Gain Monitoring

The MGPDs of the current AHCAL physics prototype show strong gain dependence on the operating temperature (~ -1.7%/K) and the bias voltage (2.5%/0.1V). Basic calculations [4] show that the electronics inside the AHCAL gaps do not require an active cooling system. Without cooling system a suitable calibration and gain monitoring system is necessary for long-term temperature effects. The current physics prototype uses a light calibration system, which is also the baseline for the proposed AHCAL design. Alternatively, radioactive sources can be considered.

5.1 Light Calibration System (LCS)

Two concepts of light calibration systems (LCS) are under investigation:

a.) Electrical signal distribution
In this concept, one ultra-violet (UV) LED per scintillating tile (detector channel) or per a few tiles produces the necessary light for calibration. The driving signals for the LEDs are transferred electrically (differential signal, LVDS) from the HEB board at the end of the absorber structure (see Fig. 1a) to the HBUs. This concept avoids optical fibres with the associated problems of optical coupling between the HBUs and between the fibres and tiles. Since many LEDs are foreseen to be driven by a single pulser and a single analogue bias voltage for the optical level adjustment, the concept depends on a good uniformity concerning the LED component to component light intensity variance.

b) Optical signal distribution
In this concept, strong LEDs on the HEB boards (see Fig. 1a) produce the calibration light. The light is transported into the detector gap by optical fibres. Impurities in the fibre couple the light through holes in the PCBs of the HBUs to the tiles. Since inside the detector gap this LCS concept only distributes optical signals, there is no crosstalk to the MGPDs and ASICs. The light level can be monitored by PIN diodes on the HEB. At least 72 detector channels will be connected to one fibre of 2,20m length; where the uniformity of light distribution will be critcial. Additionally, a fibre connection concept between the HBUs has to be evaluated (one fibre or several pieces with connectors).

5.1.1 Electrical Signal Distribution

The concept of electrical signal distribution makes use of the MGPD property to form a so called single-photon-peak structure in the spectrum. At low light intensities, only one or very few single pixels of the MGPD contribute to the output signal, which results in a spectrum (histogram) as shown in Fig. 5.

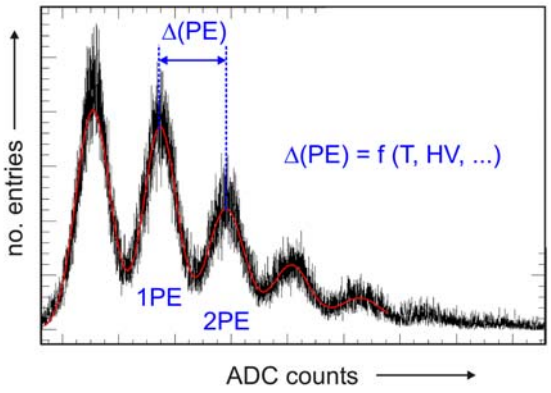
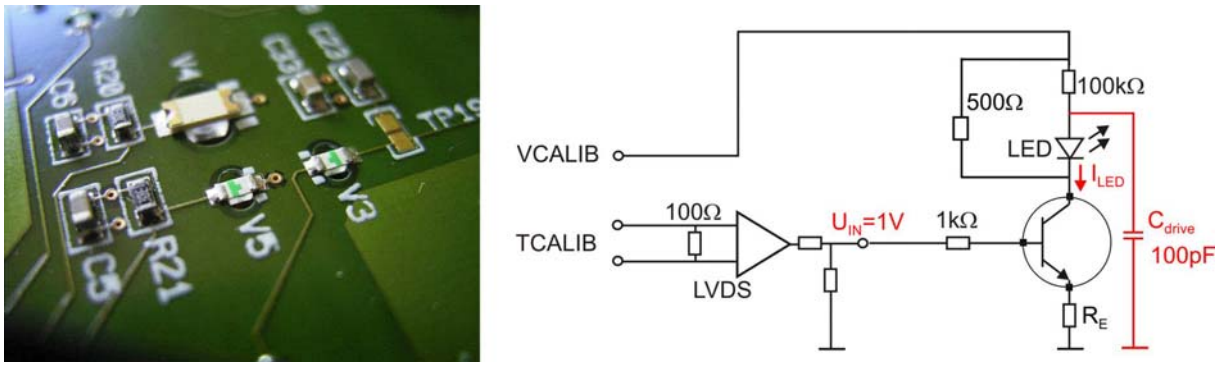


Fig. 5: Single-photon peak spectrum of a MGPD for a low-light intensity run. The first peak is the pedestal, the second peak corresponds to a single generated photoelectron (PE). The distance of the peaks (DPE) is a measure of the MGPD gain that depends on temperature and MGPD bias.

The distance of the single-photon peaks (∆PE) can be used to calibrate the detector and to monitor the MGPD gains over the time.
A first test board has been realized in order to verify a possible integration of the UV LEDs (wavelength of 395nm) to the HBUs and to do first performance analysis of the concept. The integration is shown in Fig. 6a. The UV LEDs (V3 and V5 in Fig. 6a), are automatically assembled up-side-down in a reflow process, without damaging one of the tested LEDs. This is an important step towards a concept for a detector with more than 2.4 million channels in the barrel. The driving circuit of the LEDs (Fig. 6b) is based on a fast npn bipolar transistor that is used as a switch (R_E small) and a capacitor C_{drive} that stores the necessary charge for the LED driving pulse current.



a) b)

Fig. 6: Assembled UV LEDs (V3 and V5) on a test board (left). The assembly was done automatically in a reflow process together with the remaining SMD components without damaging the LEDs. The proposed circuit for LED operation (right) foresees a fast trigger (TCALIB) that is transferred differentially to the HBUs, and a constant analogue bias voltage (VCALIB).

First performance measurements of the LEDs have been done by connecting the LED directly to a pulse generator. The LEDs show a sufficiently fast response time (pulse width) below 4ns (FWHM, Fig. 7a). In a second test, the component-to-component variations of the LEDs have been tested. In this test, the LEDs have been operated with the final driving circuit concept (Fig. 6b). The LED light was detected by a scintillating tile with MGPD (SiPM) that was coupled directly to an oscilloscope. The amplitude was monitored with respect to the analogue bias voltage VCALIB. 11 different LEDs have been tested (Fig. 7b). Although LEDs from the same reel (tape) have been used, the LED output sensitivities at a specific VCALIB show large deviations and a clustering into three sensitivity groups can be observed. Future investigations and discussions with the manufacturer have to show if a LED pre-selection or the use of another LED type (e.g. 430nm wavelength instead of 395nm) can lead to a more uniform output distribution. A spread below 25% at a specific VCALIB would enable the operation of all LEDs from one VCALIB.

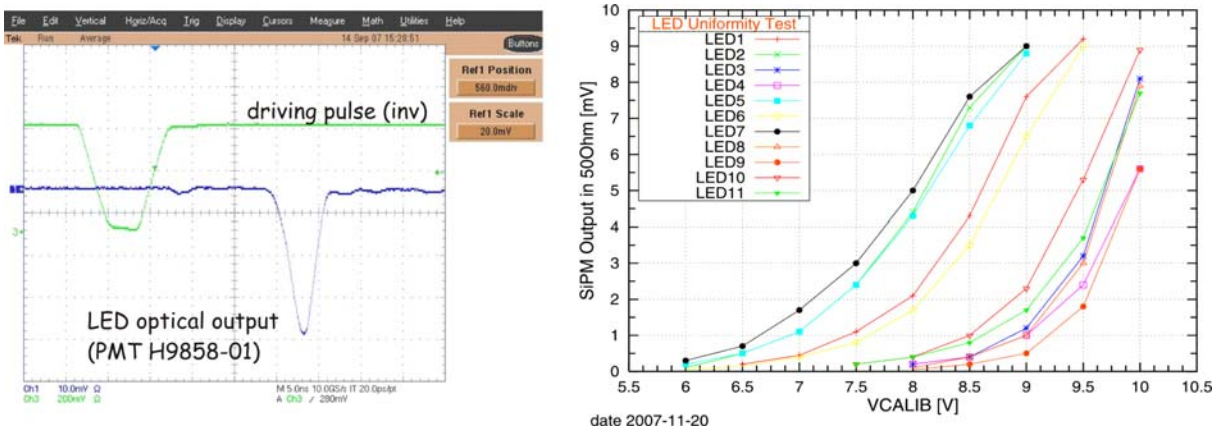


Fig. 7: Test of the LED response time by connecting the LED to a pulse generator and measuring the LED optical output by a PMT (left) and test of the LED component-to-component uniformity (right). For the uniformity test, the proposed LED driver was used and the output signal was measured with a scintillating tile and a MGPD (SiPM).

Future tests will cover measurements of the crosstalk of the driving circuit to the MGPDs, the achievable dynamic range and a linearity analysis by connecting the LED test board to a front-end ASIC and the existing CALICE data acquisition.

5.1.2 Optical Signal Distribution

The concept of optical signal distribution is currently under test with a first focus on the LED driver which must provide larger signals whilst minimizing electrical interference. A first prototype (Figure 7a) has been developed and tested in Prague (IPASCR). Detailed documentation can be found in [5]. The signal distribution by fibres will be tested in the future.

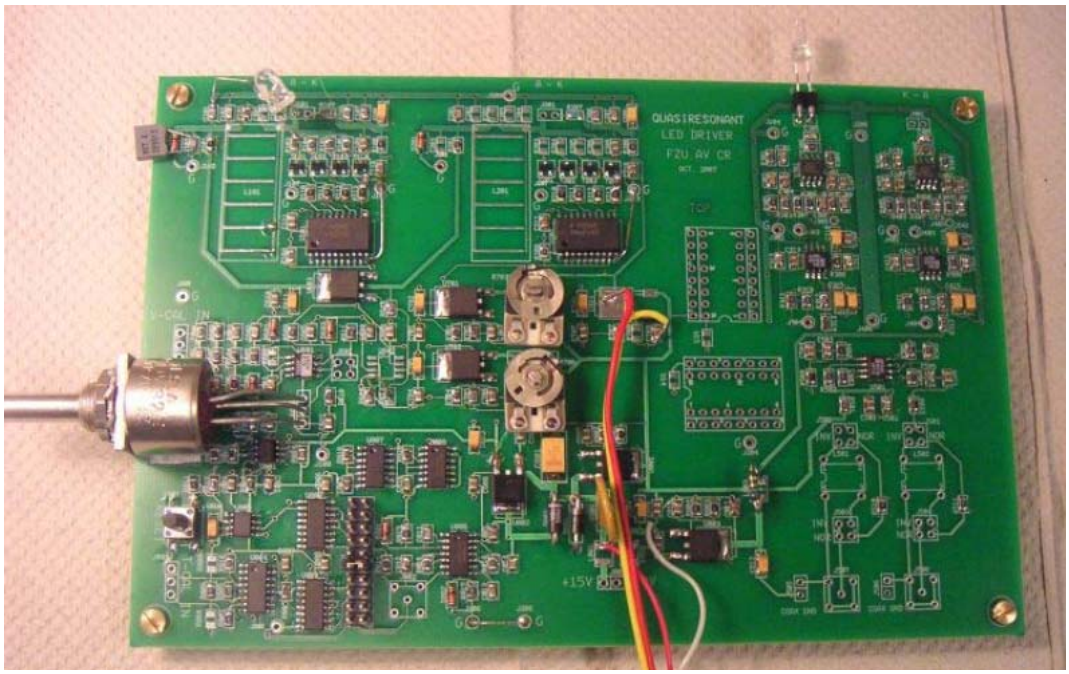


Figure 7a) 2-channel prototype of a quasi-resonant LED driver.

6 AHCAL Data Acquisition

For CALICE, a general data acquisition (DAQ) architecture is proposed for all detector parts (ECAL, DHCAL and AHCAL) [6][7] in order to enable detector interfaces that are as common as possible and to allow the designers to utilize the synergies of the common design structures. The DAQ scheme is divided into the backend module ODR (off-detector receiver), the intermediate module LDA (link/data aggregator) and the detector-specific front-end module DIF (detector interface, one per AHCAL layer) as shown in Fig. 8.

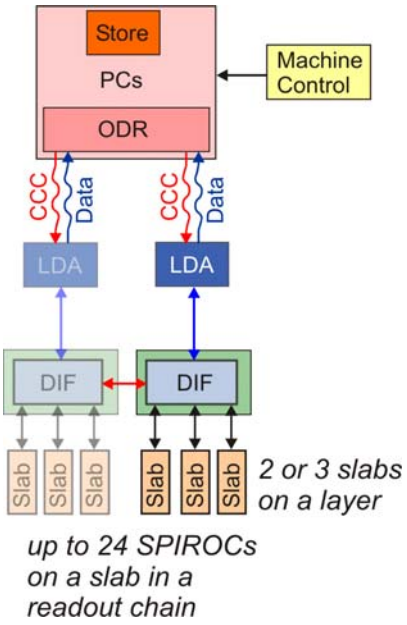


Fig. 8: DAQ structure with the general blocks ODR, LDA and DIF for the AHCAL setup. CCC (clock, control and configuration) as well as the Data (readout) path are realized as optical connections.

Although the amount of data (configuration and event data) that is transferred between the detector slabs of the three CALICE detectors and the DIFs is different, many parts of hardware and operating software of the controlling devices (e.g. VHDL code of the FPGAs) can be developed in a common approach in order to reduce the design effort. A working group with a member of each detector-design team and one of the CALICE DAQ team coordinates these design efforts.

In the AHCAL case, the DIF module is placed on the HEB board (Fig. 9), along with the AHCAL specific blocks CALIB (calibration block, including the light calibration system) and the POWER+Monitoring block (power regulators, power cycling control for the ILC-mode operation, readout of the temperature- and voltage-monitors). The three subgroups DIF, CALIB and POWER+Monitoring are supposed to be realized as independent blocks in separate mezzanine boards on the HEB. Ultimately, tight space constraints will favour direct integration into the HB, however for task-sharing in the prototyping phase the advantages of the modular structure are obvious. The signalling between the DIF and the two AHCAL-specific subgroups, including signals for debugging purposes is shown in a preliminary state in Appendix B.

6.1 DIF

The DIF has in all CALICE detector concepts the following main tasks [6]:

- Receive and regenerate the clock signal from the LDA and distribute it in parallel to the Front-End ASICs.
- Receive and decode configuration data from the LDA and distribute the data to the Front-End ASICs. In the AHCAL setup, the SPIROCs of a slab are set up in a slow control serial chain for the write operation of configuration data. The foreseen data rate is 1MBit/s or higher, e.g. 5 MHz.
- Receive and decode fast commands from the LDA and send it to the Front-End, as e.g. a test-trigger.
- Receive and buffer result data from the front-end ASICs, reformatting and transmission of the data to the LDAs. For the readout of the result data, the ASICs of a slab are organized in a readout token setup. The ASICs send their data on a common data-bus between the DIF and

the all ASICs of a slab and upon finishing the transmission, the readout token is passed to the next ASIC in the chain. Readout speeds between one and five MBit/s are possible.
- Main control of the power pulsing sequence for the front-end ASICs for the ILC-mode operation.
- Watchdog of the operation.

Fig. 9 shows the top-view of a 3-slab AHCAL (half-)layer. Two of the slabs contain 24 SPIROCs on 6 HBUs, one slab only has 18 SPIROCs in a readout chain. The interconnection between HBUs and between DIF and HBU is realized by two 80-pin connectors, the first one mainly for signals from DIF and CALIB block (red bus on HEB), the second one for power (+3.5V, +5V, GND and MGPD bias voltage) and (temperature-)monitoring signals (blue bus on HEB). The signals on the HBUs are connected in parallel to all SPIROCs (red bus) or run in a token-chain architecture from one SPIROC to the next (blue bus, purple return signal).
To a HEB with the proposed DIF board, two or, as shown in Fig. 9, three AHCAL slabs are connected, depending on the layer width. For redundancy reasons, a 'DIF-DIF-connector' between the HLD boards of two half-layers connects the two layer parts together (cf. Fig. 11).

6.1.1 Data Rate Slab => DIF

The SPIROC has 36 input channels with an analogue pipeline of 16 time-slices (stages), a TDC for each channel and a 12-bit ADC. The amount of data per SPIROC and readout cycle is 18.696 bits (8-bit Chip ID, 256-bits time stamp, 9216 bits TDC information, 9216 bits data). For the longest readout chain of 24 SPIROCs, the amount of data is 449kbits. Since the readout with 1MHz clock is not possible in 200ms, two options can be considered:
- increase the readout clock speed to 3MHz (readout in 150ms).
- subdivide each AHCAL slab into 3 parallel readout chains, each running with 1MHz. In this case, the DIF would have to operate 9 data input channels (3 slabs per DIF, each with 3 data lines)

Assuming **worst case conditions** for the AHCAL half-sector data (3 slabs per DIF, each 500kbits of data which is only true for the largest layer), the DIF receives 1.5MBit per bunch train (7.5MBit/s at 5Hz bunch-train rate). With 38 AHCAL layers, the LDA receives 57 MBit per bunch train (285 MBit/s).

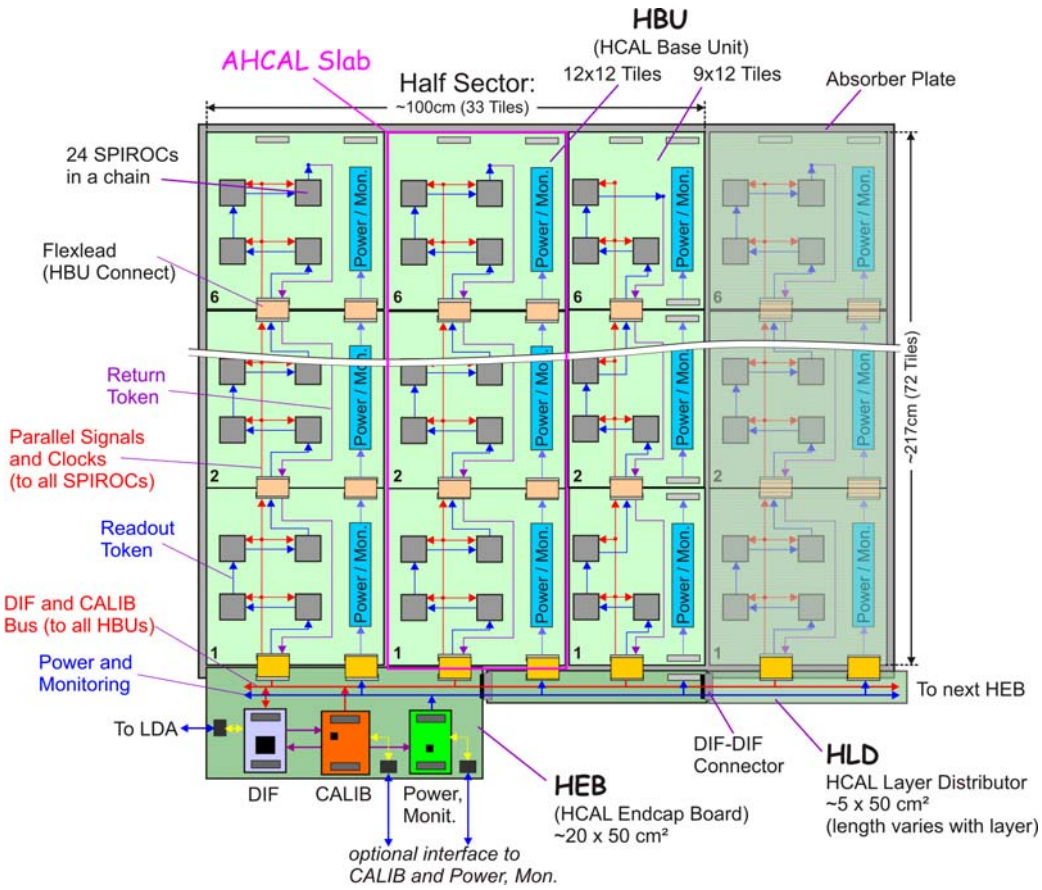


Fig. 9: Top view of an AHCAL detector layer with 3 slabs and the interface board HEB, carrying the DIF module and the AHCAL specific modules CALIB and POWER+Monitoring. The AHCAL slabs contain HBUs of different sizes.

6.1.2 DIF to Slab Signals

During the EUDET meeting in Paris, the DIF working group completed a list of all signals between the DIF and the slabs of the three CALICE detectors (see Appendix A) for the current FE-ASIC prototype version.

6.2 CALIB

In order to offer the possibility for gain calibration and monitoring for the MGPDs, the AHCAL will include a light calibration system based on UV-LEDs. Two different concepts are under consideration (see section 6.1). In case of the electrical signal distribution, the respective driving pulse will be sent in LVDS logic to the HBUs and coupled to an RF transistor that operates the LEDs. The LVDS receiver that is necessary on each HBU will be operated from a separate power line that can be switched off when no calibration is needed (power saving). The LED power level can be adjusted by an analogue control voltage (VCALIB) that is provided by the CALIB module (12-bit DAC on CALIB module). The LED setup is currently under test. Additionally, the SPIROC's analogue charge injection inputs are accessible in parallel in a similar manner as the LEDs. Since the external trigger of the detector is a very fast signal and must be combined in some cases with the calibration system, it is also controlled by the CALIB block and sent in LVDS logic to the HBUs.

The CALIB module is logically a slave to the DIF and is fully operated through the AHCAL-specific part of the DIF.

6.3 POWER

The POWER module provides the AHCAL slab with the supply voltages +3.5V, +5V and GND as well as the SiPM bias voltages. The number of different SiPM voltages that have to be provided to each slab is not known yet. It depends on the quality (bias voltage spread) of the final SiPM production. It is aimed that not all SPIROCs of a slab are connected in parallel to the power bus, so that a broken SPIROC that shorts a power line to GND does not disable the whole slab. The necessary number of lines per voltage is under investigation.
On the POWER module there will be the voltage regulators for the supply voltages and a large capacitor bank that can cope with the power-cycling of the detector. Special care has to be taken that the power cycling does not lead to oscillations in the power planes.

Due to the temperature dependence of the SiPM response, it is necessary to monitor the temperature on the HBUs. It is assumed that three HBUs of a slab should be equipped with a temperature sensor (e.g. PT1000) that is read out via two extra lines each. Additionally to the temperatures, the supply voltages of the slab are monitored. On the POWER module, an ADC digitizes the response of the sensors, and transfers the results to the DIF if requested by the user.
An additional radiation monitor for the gamma dose could be considered on the DIF.

The POWER and Monitoring module is logically a slave to the DIF and is fully operated through the AHCAL-specific part of the DIF.

6.4 Redundancy, Failsafe setup

For the write-process of configuration data from the DIF to the SPIROCs, the ASICs are organized as slow-control chains. With 703 bits of slow-control data per ASIC, 24 SPIROCs in the longest chain and 1MHz slow-control clock, the write cycle takes about 17ms.
In order to cope with the failure of a single chip in the chain, the failsafe setup as shown in Fig. 10 should be taken into account for the slow control data chain as well as for the readout of the ASIC's result data. A respective failsafe configuration procedure has to be developed in the future.
In order to be able to cope with a failing DIF or LDA module, the endcap modules of a AHCAL layer will be connected via a 'DIF-DIF-connector'. By this each AHCAL slab is connected to two LDA modules (Fig. 11).

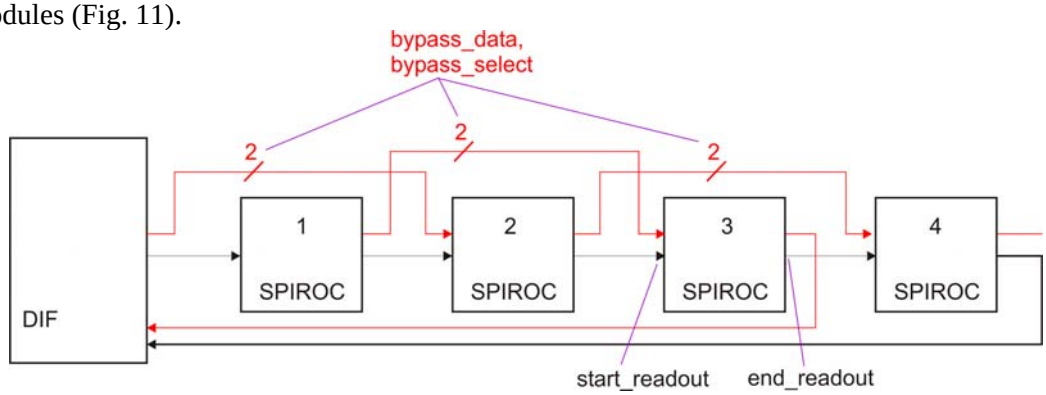


Fig. 10: Failsafe setup of the SPIROC ASICs. If e.g. SPIROC 2 in the chain fails, SPIROC 1 is programmed to use the bypass output, and SPIROC3 is programmed to use the bypass input, instead of the usually foreseen pins 'start_readout and end_readout'.

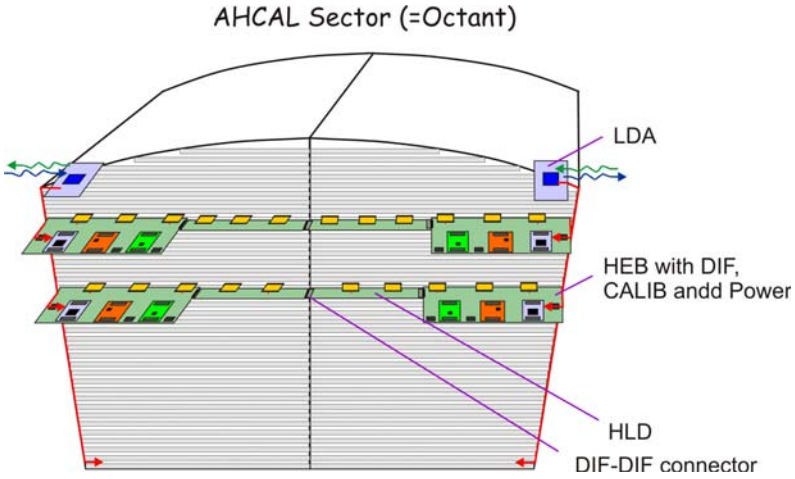


Fig. 11: Failsafe setup of an AHCAL sector. The HEB and HLD modules of a layer are connected by the DIF-DIF connector so that each AHCAL slab is connected to two LDA modules.

Summary

A technical design of the HCAL sector electronics integration has been prepared. The most critical components have been verified by prototypes. The next steps will address system integration issues like layer to layer interconnection. A structure is emerging which will allow testing the novel MGPD technologies under the conditions of a hadron calorimeter which are characterized by both large extension and high compactness.

Acknowledgement

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Appendix A : Signals between DIF and AHCAL slabs

	Signal	Function	AHCAL (SPIROC)
Power			
	Vdda	Analog supply +3.5V	power
	Vddd	Digital Supply +3.5 V	power
	GND	Common ground 0V (GND)	power
	HV	High Voltage (SiPM)+/-xxxV	power
		DAC/Analog +5.0V	power
	Vref	Reference voltage +x.xV	power
slow control			
	clk_sc	slow-control shift-reg. clock	LVCMOS
	srin_sc	slow-control shift-reg. input	LVCMOS
	srout_sc	slow-control shift-reg. output	LVCMOS
	load_sc	latch slow control data	LVCMOS
	resetb_sc	reset slow-control register	LVCMOS
readout			
	start_readout	token input of data readout	LVCMOS
	end_readout	token output of data readout	LVCMOS
	CK_5M	5MHz/1MHz clock readout	LVDS
	CK_40M	40MHz clock	LVDS
	TransmitOn	Dout is active	open collector
	Dout	serial data output	open collector
	SCASat	analogue pipeline full	open collector
	RamFull	digital RAM full	
controls			
	start_acqt	start data acquisition	LVCMOS
	start_conv_DAQb	start ADC conversion	LVCMOS
	no_trig/RazChn	Suppr. Int. trig. / rearm trig.	LVDS
	Val_Evt	event valid	LVDS
	trig_ext	external trigger	LVCMOS
	resetb_BID	reset event counter	LVCMOS
	resetb	global reset	LVCMOS
Power Controls			
	pwr_analog	analog power on	LVCMOS
	pwr_adc	ADC power on	LVCMOS
	pwr_dac	DAC power on	LVCMOS
	pwr_ss	Slow shaper power on	____
	pwr_sca	SCA power on	LVCMOS
	pwr_digital	digital power on	LVCMOS
Calibration			
	CTest	*charge injection (pulse)*	analogue

Signal list for the ASICs prototype versions.

Appendix B: Preliminary Signal Map for the DIF-AHCAL SLAB interface