EUDET-Memo-2008-06

A prototype readout system for the LCTPC

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10.03.2008

Abstract

The EUDET milestone of delivering a prototype readout system for the Linear Collider TPC (LCTPC) has been met. The readout system will be used to study the performance of the 'large' prototype TPC, built in preparation for the International Linear Collider (ILC). The front end electronics is based on a system used in the ALICE experiment at the LHC, but with modifications needed to be compatible with new gas amplification systems and small pad sizes foreseen for the final TPC at the ILC. The data acquisition system uses the hardware and the drivers of the ALICE experiment, but the software necessary for the new readout system has been developed.

1 Introduction

The detector at the future linear electron-positron collider ILC (International Linear Collider) will include a tracking device, which is able to provide a momentum resolution sufficient to observe a possible Higgs signal from the missing mass spectrum of the Higgs strahlung processes. One option for such a tracking devise is a large TPC using new gas amplification techniques, like GEM's or Micromegas, together with smaller pads compared to previously used. In order to study the performance of such a TPC, a 'large' prototype is being built, offering a certain modularity with respect to investigating various gas amplification systems, pad sizes and geometries as well as different read-out systems.
The main read-out system which has been developed is based on the read-out electronics used in the ALICE experiment [1]. Some modifications have been necessary in order to adapt it to the expected output signals from the new gas amplification systems, including a new programmable charge amplifier. The schematic layout of the system is shown in Fig. 1 and a short description of its components follows below. One complication is given by the fact that the effective area occupied by the front-end card (FEC) per channel is significantly larger than the smallest pad size to be investigated, which is 1x4 mm^2. Thus the FEC's can not be attached directly to the pad plane, but have to be connected via kapton cables as indicated in the figure.
The read-out electronics for the large prototype should offer a performance that is better than that of the final TPC, so that the compromises that may become necessary for the multimillion channel final system can be studied and optimized. In order to meet these requirements the front end electronics will not only contain a programmable charge amplifier ASIC, called PCA16, but also digitisation up to 40 MHz sampling rate by a modified ALTRO chip [2] , as developed for the ALICE experiment.
The FEC's are placed on a backplane together with a Readout Control Unit (RCU) [3], which is used to control the readout. Data is sent through a Detector Data optical Link (DDL) to a Detector Read Out Receiver Card (DRORC), which is a PCI card situated in a PC. The low level software consists of drivers and libraries for communicating with the DRORC and the front end through the DDL. The TLU is the central trigger unit for all subdetectors in a common test beam setup. The distribution box (DBOX) can receive triggers from either the TLU or from local triggers when the TPC is operated in a stand-alone mode.

1.1 The charge sensitive preamlifier

The specifications of the newly developed PCA16 programmable charge preamplifier are:

- 1.5 V supply; low power consumption <8mW/ channel.
- 16 channel charge amplifier + anti-aliasing filter.
- single ended preamplifier.
- fully differential output amplifier.
- operated with both signal polarities.

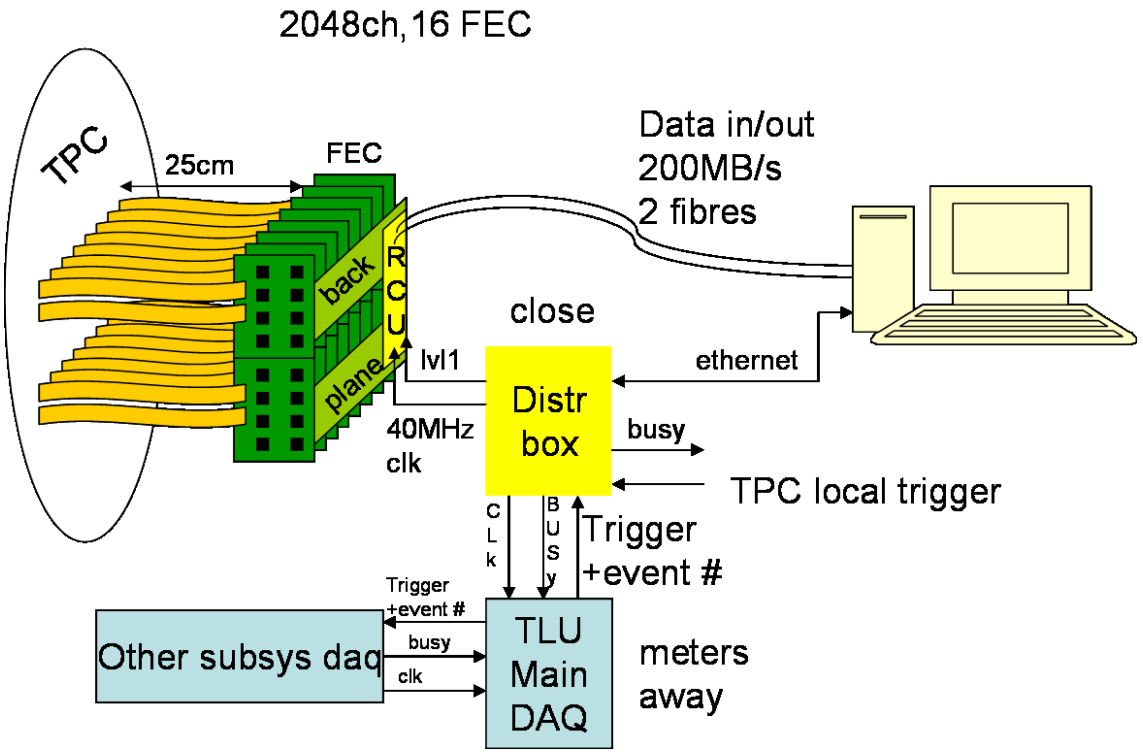

Figure 1: *A schematic view of the front-end electronics and the data aquisition system.*

- power down mode with a wake-up time of 1 ms.
- programmable peaking time between 30 and 120 ns.
- programmable gain in four steps between 12 to 27 mV/fC.
- preamp-out mode.
- tunable decay time constant of the preamplifier.

A first step towards the development of the PCA16 was to produce a non-programmable preamplifier with 12 channels in order to confirm that the desired performance could be met. The 12 channel prototype preamplifier chip, with a fixed rise time of 100 ns, was produced in 130 nm CMOS technology. The test results of the preamplifier are summarized in Table 1.
As can be seen from the table, the performance of the chip is up to the specifications or better. Especially one may notice that the noise is much below the specifications and the dynamic range is significantly wider.
The final PCA16 chip was delivered at the end of 2007. It has a silicon area of 6 mm^2 with 94 pins in total. Out of these there are 16 input pins and 32 output pins for the differential pulses. The remaining pins are for grounding and voltage supply, and 9 pins

Parameter	Specification	Simulation	MPR Samples
Noise	< 500e	300e (10 pF)	270e (10 pF)
Conversion gain	10 mV/fC	10 mV/fC	9.5 mV/fC
Peaking time (default)	100 ns	100 ns	100 ns
Non linearity	$< 1\%$	< 0.35 %	< 0.3 %
Cross talk	< 0.3 %	0.4 %	< 0.3 %
Dynamic range	> 2000	3300	4600
Power consumtion / channel	< 20 mW	10 mW	10 mW

Table 1: *Comparison between specifications and results from simulations and tests of the preamplifier-shaper prototype.*

are used to set the programmable parameters of the chip. The baseline option for control of the PCA16 is to use the the Board Controller (FPGA) on the FEC to set an octal DAC (Digital to Analogue Converter), which defines the decay time of the preamplifier output. An 8-bit shift register provides the digital input to the PCA16 in order to set the rise time, the gain, the polarity and to bypass the shaping function. In Fig. 2 a schematic diagram of the control system is shown.

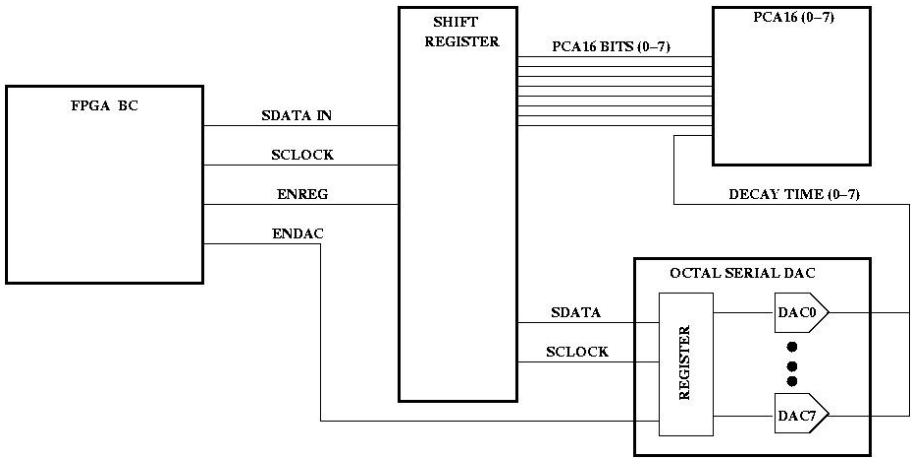

Figure 2: *Schematic diagram of the system to control the parameters of the PCA16*

A reprogramming of the FPGA, via an EPROM, was needed to include the additional functions for changing the parameters of the PCA16 on-line. The signal transfer between the PCA16 and the ALTRO is differential but is internally converted to single-ended analogue signals. A separation between the digital and analogue grounds is provided via the different grounding pins of the ALTRO. The programming of the PCA16 from the FPGA introduces the need for digital grounds. However, the signals from the shift register and the DAC's, used to set the PCA16 parameters, can be considered as D.C. signals and therefore the noise on the PCA16 input pins is expected to be negligible.

A fall-back solution was foreseen in case of noise problems, which allows to set the parameters manually by jumpers/dip-switches. However, tests performed with the PCA16 parameters set on-line via the FPGA have proven its functionality and also that the noise level is acceptable.
In total 1000 PCA16 chips have been produced, of which 200 have been purchased, which is significantly beyond the request of the EUDET project. The remaining ones are reserved for the extended study. The first tests of the PCA16 chips have proven its functionality qualitatively. In order to save time the number of chips needed for the prototype FEC were mounted before they had been fully tested. However, before the production phase of the FEC's is starting, the PCA16 chips will go through individual tests, using a chip testing robot in Lund. One example of such tests is the measurement of the response to input pulses of increasing amplitudes. Fig. 3 shows the linearily increasing pulses on an expanded scale such that the individual pulses can be identified, whereas Fig. 3 shows the complete spectrum to illustrate the linear behaviour over the full range. The kink is at a point where the step size in the amplitude is increased.

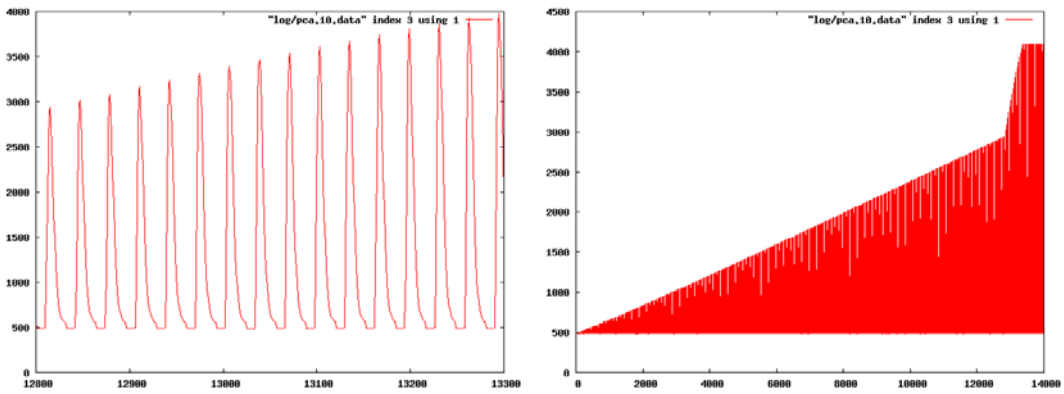

Figure 3: *Spectrum of pulses with increasing amplitudes measured at the output of the FEC.*

1.2 The digitization

The sampling frequency needed for the digitization depends on the characteristics of the pulse from the gas amplification system. In order to accurately reconstruct the pulse shape to extract the charge deposited on the pad, a few points on the rising edge of the pulse are needed. With a sampling frequency of 40 MHz one would measure rise times down to around 50 ns. The ALTRO chip has been developed for the ALICE TPC to be operated at 10 MHz with 10 bit resolution. It offers a large flexibility and can be used as a general purpose AD-converter for a multi-channel system. If the sampling frequency is increased to 25 MHz the effective number of bits decreases to 9 which would still be

sufficient for the expected input pulses. Enough ALTRO chips are available to match the number of PCA16 chips. A modified version with 40 MHz sampling rate has been developed, which provides a resolution corresponding to an effective number of bits equal to 9.5. Presently 125 chips of 40 MHz sampling rate are available, which corresponds to 2000 channels in total. These are intended to be used for the EUDET project.
The data transfer between the PCA16 and the ALTRO is differential, which allows separation of the analogue and digital grounds. The ALTRO chip contains a memory of 1024 10-bit words for event storage for each of the 16 channels. This corresponds to a depth of 25 μsec drift time at 40 MHz sampling rate. The maximum drift time in the 60 cm long prototype TPC is 15 μsec if we assume a drift velocity of 4 cm/μsec. Thus, the 25 μsec event length foreseen for the ALTRO storage, provides sufficient margin for different gas choices. The ALTRO has a flexible subtraction of pedestals accompanied by a powerful suppression of zero data. Thus, it is expected that only valid data will have to be read out from the ALTRO. This will reduce the number of events on the data aquisition (DAQ) system. The ALTRO chip is read out in 40 bit wide words on a customized 40 MHz bus.

2 The data aquisition system

A schematic view of the components of the prototype TPC readout system, as described here, is shown in Fig. 4. A small modification of the RCU has been necessary in order to adapt to the way the trigger signal are delivered by the LCTPC. The ALICE drivers and libraries for communicating with the readout hardware are used unmodified. The software which has been developed for this DAQ system consists of the code that provides the configuration of the hardware, the readout, and the local data storage. A standalone monitoring and histogram presenter system has been implemented. The run control is done from a graphical user interface. Eventually, it will all be connected to a common beam test data acquisition system.

2.1 Configuration

For the data acquisition to become active a START DAQ command must be received from the run control. This will initialize the handling of the DRORC, memory buffers in the computer, and the configuration of the front end electronics. There are several settings to be made in the front end electronics, e.g. the run operating conditions of the PCA16, ALTRO, and RCU must be downloaded. These values are stored in configuration files, which are read and downloaded when the START DAQ command is received from the run control. After the initialization the readout is waiting for a START RUN command.

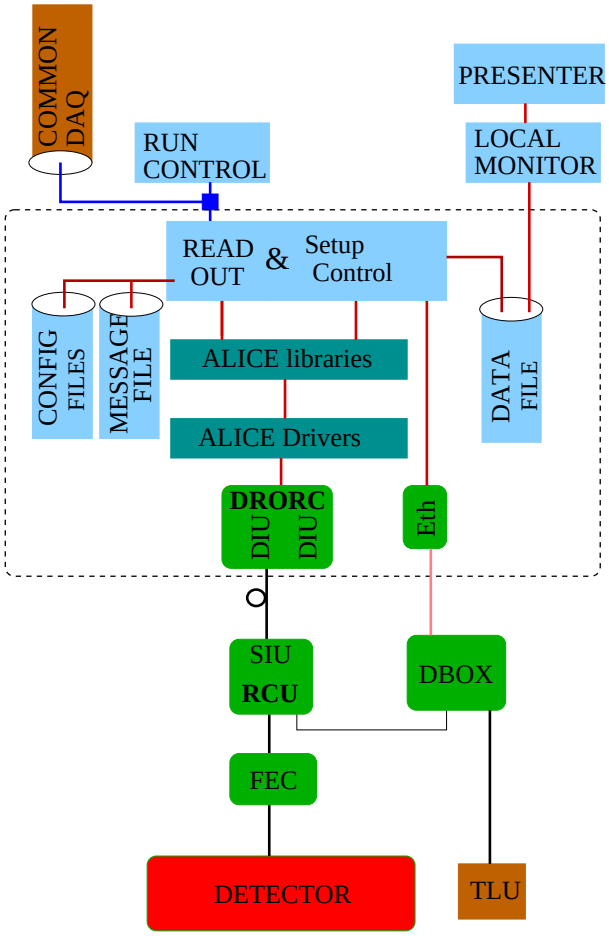

Figure 4: *Overview of the prototype DAQ TPC readout.*

2.2 Trigger and readout

When a START RUN command has been acknowledged, the readout system is ready to receive triggers. On the reception of a trigger from the DBOX the RCU distributes it via the backplane to the FEC's. The TLU is common to all subdetectors involved in building events from the observation of particles in the test beam. The trigger starts the digitization of the analogue information from the PCA16 in the ALTRO chips, and a configurable number of time samples is stored in a memory in the ALTRO. The data is automatically read by the RCU and pushed into the DRORC, which stores the data directly into the physical memory of the readout computer. The readout program is polling the DRORC for new data, and stores the data in a file on a local disk. During the whole readout of an event the trigger system must be blocked from accepting new triggers. The communication between the DBOX and readout program is done

through the network. The readout program is subdivided into two parts, one part that handles the communication with the hardware, and one that acts as an interface to the run control through the network. These parts communicate with each other through TCP/IP sockets and Unix signals.
The synchronization of events between RCUs and other detectors will be done with a time stamp given by the time of the trigger from the DBOX together with the event counters in the DBOX and in each RCU. In a common environment the DBOX gets the event number from the central trigger unit (TLU).

2.3 Run control

The run control is written in Java. It can be run on any computer, and communicates with the readout program through the network. The control has a few commands as described in table 2.

START DAQ	The readout will open devices, setup and configure the readout, and download the configuration to the electronics.
STOP DAQ	Stop data acquisition. The readout will close all devices, and wait for a START DAQ command.
START RUN	Start a run. The readout enables the trigger system, and start polling for data.
STOP RUN	Stop a run. The readout disable the trigger system, and wait for a START RUN or a STOP DAQ command.
STATUS	Get status. Request the status of the system.

Table 2: Run control states

2.4 Monitoring

The readout stores the events either in a shared memory or in a data file. A MONITOR SERVER sends events from the shared memory or the data file to the MONITOR program when it requests an event. This can be done over the network, i.e. the MONITOR can be run on any computer. The MONITOR program decodes the event format and fills histograms. It creates and updates histograms in a shared memory or in a histogram file, being accessible from the PRESENTER, which is a ROOT based program. The monitor server is also able to playback a data file.

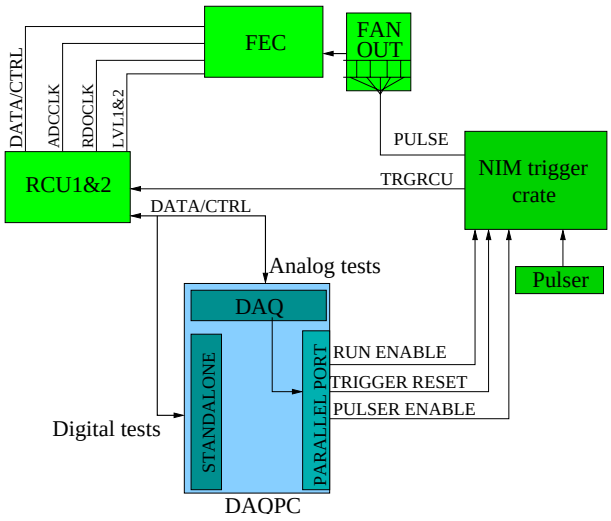

Figure 5: *Schematic diagram showing the test set up.*

3 The test set-up

The test set-up is shown schematically in Fig. 5 and in reality in Fig. 6. The pulses are generated by a pulse generator and sent via a NIM trigger crate to the FEC. A fan-out card makes it possible to test individual channels or arbitrary combination of channels via the setting of manual dip switches. This enables detailed investigations of noise and cross talk. The signals are fed either directly into the FEC or via a kapton cable, to investigate the influence of the cables on the electronics noise. The FEC is readout by the RCU at the receipt of a trigger signal from the NIM crate and the data are sent to the DAQ PC. A parallell port of the DAQ PC provides the enable/reset signals to the trigger pulser system. After an enable has been given a trigger is generated by the pulser. The performance of the complete FEC is observed via the branch 'Analogue test' in Fig. 5, but also the content of specific registers can be tested via the branch 'Digital test'. Special software has been written for this.

4 Tests of the FEC

The upper four plots of Fig. 7 shows a sampling spectrum obtained without kapton cable on the input from 4 of the 16 channels (channels 10 - 13) contained in a single chip readout chain. A shaping time of 120 ns and a gain of 12 mV/fC was used for the PCA16. Channel 12 was pulsed and the other channels give information about cross talk and pedestal noise. A close inspection shows that the channels closest to channel 12 (channel 11 and 13) exhibit tiny signals, which from a quantitative analysis comes out to be less than 1% cross talk. The most important parameter to be measured is the noise

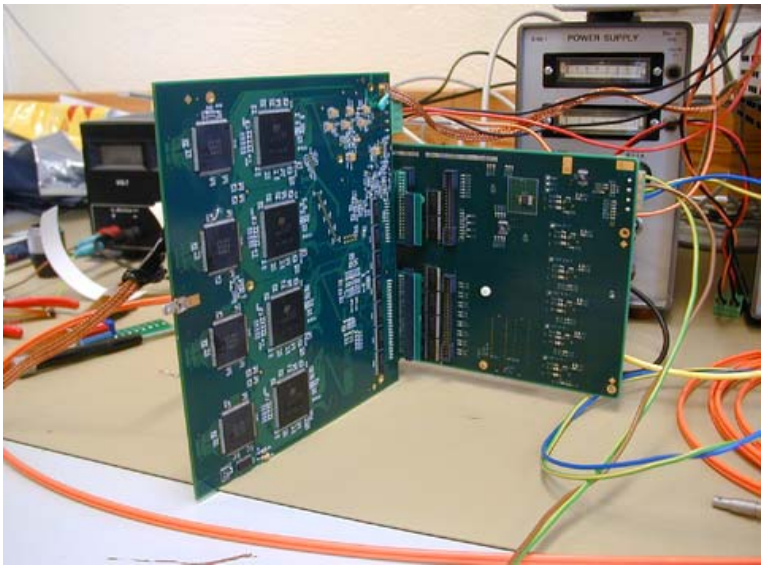

Figure 6: *Photograph showing the test set up.*

level. This is obtained from the widths of the pedestals (zero levels) of the channels. The pedestals are shown in the four lower plots of Fig. 7 for the same channels as above, where the level and the width of the pedestal are presented in a mV scale on the horizontal axis. The width of the peak provides information about the noise. The RMS-values of the peaks in the non-pulsed channels are typically 0.6 mV. The bin width is 1 mV and the gain, as mentioned above, was 12 mV/fC. From the fact that 1 fC corresponds to about 6250 electrons, the noise level of 0.6 mV is slighly more than 300 electrons which is close to the level of the internal amplifier noise. The pulsed channel has a pedestal distribution with a small tail, which is caused by a small undershoot of the pulse at the side of the falling edge. The peak of the pulse itself is far outside the scale shown.
Fig. 8 shows another pedestal spectrum, for channels 11 to 14, but now with signals read out via a 25 cm long kapton cable. Again the shaping time was 120 ns and the gain 12 mV/fC, but none of the channels were pulsed. The noise levels have RMS-values between 1.5 and 2 mV. The observation is that the introduction of the kapton cable increases the noise about a factor three from slightly above 300 to a level of around 1000 electrons.
Running at the shortest shaping time of 30 ns makes a regular frequency behaviour in the noise to appear in the sampling spectrum at a point corresponding to the time at which the ALTRO chip starts composing 40 bit words, out of the 10 bit word AD information, and putting it into an internal memory. Before the full choice of parameter settings of the PCA16 can be used the system noise should be reduced.

5 Conclusion

A complete front end board with 128 readout channels has been built and a data aquisition system has been developed. Initial tests have proven that the system works. The programability of the PCA16 preamplifier chip allows the system to be operated under various conditions. Some problems have been observed when running at the shortest shaping times. These problems are under study and will be solved before the production of the FEC's starts. Especially the coherent noise has to be reduced and it has to be shown that the cross talk is below 1% on all channels generated by signals transmitted without kapton cable. The effects of the cable will be subject of a special study with different modifications of the cable design.

Acknowledgement

This work is supported by the Commission of the European Communities under the 6^{th} Framework Programme "Structuring the European Research Area", contract number RII3-026126, by the Swedish Research Council (VR) and by the Scientific Research Fund FRNS (Belgium).

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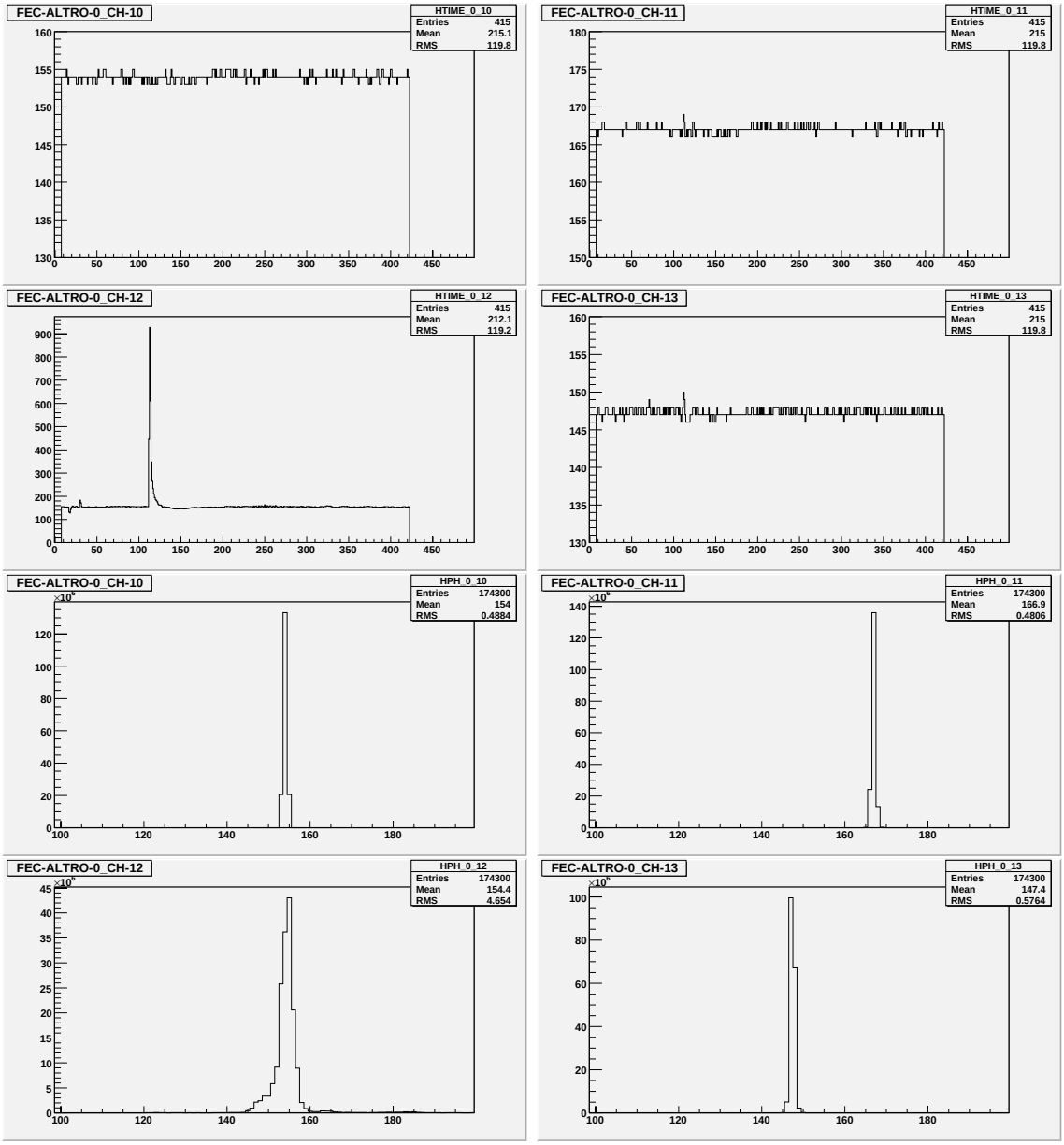

Figure 7: *Sampling spectra and pedestal spectra for the channels 10 to 13. Channel 12 has been pulsed.*

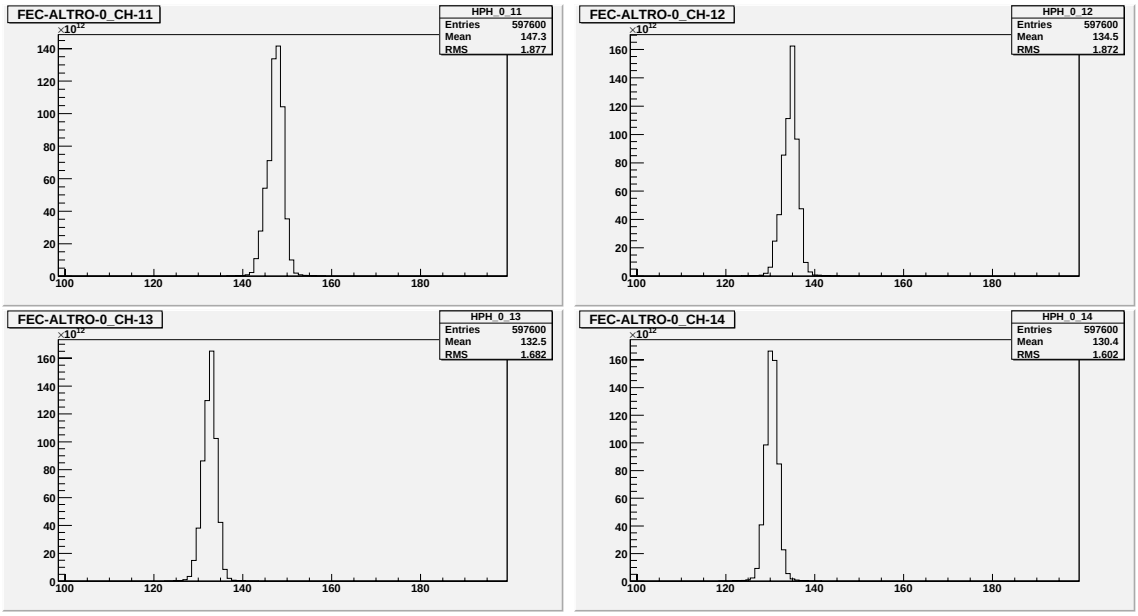

Figure 8: *Pedestal spectra for the channels 11 to 14.*