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JRA1 Progress Report: The data acquisition framework

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Abstract

The JRA1 data acquisition (DAQ) framework has been used successfully in the 2007 and 2008 testbeam campaigns. This memo presents an overview of the framework and current improvements as well as remaining issues of the DAQ. Finally an outlook of the needed changes to adapt to the readout of the final telescope sensor in 2009 is given.

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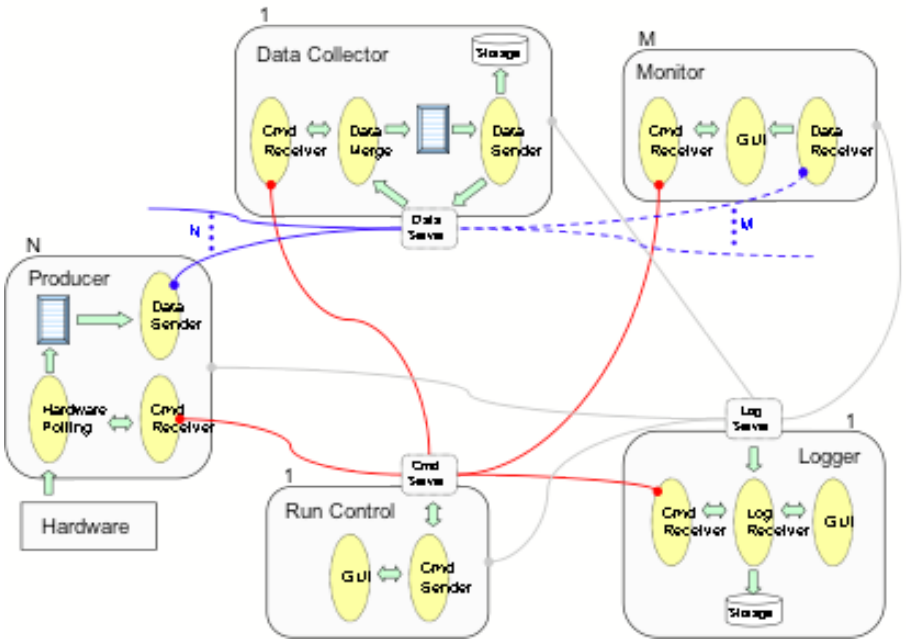

Figure 1: The EUDAQ software scheme.

1 Introduction

The JRA1 data acquisition framework has been described in [1] and [2] in detail. The dedicated hardware for the DAQ system has also been described elsewhere ([3], [4]). In this framework, several producer tasks communicate with a global run control using sockets (see Figure 1). These producer tasks connect to the hardware of the beam telescope, to the TLU and eventually to the DUT. Data from all producers is sent to the central data collector and can be monitored by several processes. An online monitor based on the ROOT framework showing online data quality monitoring histograms as well as a process to collect log messages are available. EUDAQ is written platform independent and runs on MacOS, Linux and Windows using cygwin.
In addition, integration of different user applications is possible at DAQ software level: The user provides own DAQ hardware by implementing dedicated producer tasks. This approach allows maximum flexibility and has been followed successfully by a few users already.
This memo will concentrate on two topics, that have been addressed recently or are still open:

- The VME readout speed
- Adaption of the software framework to the final chip

2 The VME readout speed

2.1 Situation in 2007 and 2008

The years 2007 and 2008 have been used to establish a stable system and get first experience with the demands of different users (only in 2008, we had seventeen weeks of tests at CERN). Useability and robustness of the system were the main goals of these 2 years.
While these goals have been achieved quite successfully, some issues still remained to be solved. After two years of running, a few smaller bugs concerning stability need to be solved. In addition, the readout of the system was in the order of a few tens of Hertz only, while we want to establish a readout speed in the order of 1 kHz.
It has been discovered quickly, that the problem was in the usage of the VME driver: The driver works by mapping windows of VME addresses into the memory space. The software was remapping this window each time that a new card was addressed and this process took 2-3 milliseconds per card. With 6 cards in the system, this effectively reduced the speed of the DAQ to below 50 Hz.
On the other hand, this readout speed was sufficient for all the users in the extensive test campaign in 2008. Thus we decided to address this issue only after end of the campaign, to avoid stability issues during the data taking.

2.2 Improved driver and readout

An improved driver for the VME system has been developed end of 2008. This driver uses different memory windows for each different readout board, thus avoiding the remapping of the memory space during the change of the boards.
The solution has for now been tested only in the lab, using two readout boards. The boards have been run in zero-suppression mode. With the new driver, the readout speed of two cards improved by a factor 4 from 150 Hz (with two boards, only 2 remappings are necessary) to 600 Hz.
Detailed measurements of the VME readout have been performed and the obtained results are shown in Figure 2. A readout process works as follows:

- The VME CPU clears the BUSY flag via a VME command
- The data reduction boards (EUDRBs) wait for the next trigger
- and read out one frame. This takes 1126 μs for a MimoTEL sensor at 15 MHz.
- The EUDRBs process the event ($\sim$ 125 μs)
- The data is transferred by a block transfer (MBLT) to the VME CPU and added to the event buffer (190 μs per board)
- The BUSY is cleared (20 μs) and the system is ready for the next event.
- Then the data is sent to the main DAQ PC (40 μs).

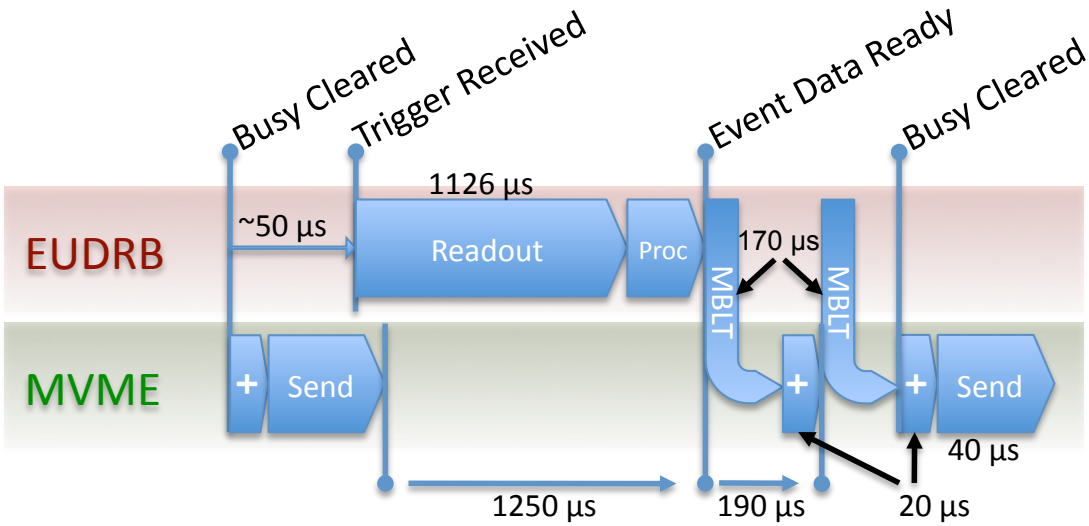

Figure 2: VME readout by the VME cpu (MVME 6100) of a data acquisition board (EUDRB).

With this timing, it should be possible to readout 6 boards at around 400 Hz (1250 μs for the readout of the EUDRBs and 6*190= 1140 μs for the transfer to the VME CPU. This still needs to be verified with the setup at DESY in early 2009.

2.3 Possible further improvements

Further speed improvements are still possible: In the current firmware of the EUDRBs, the BUSY has to be cleared externally via a VME command. It is easily possible to clear the BUSY, as soon as the data has been processed from the input buffer to the output buffer. Then, the block transfer of the data could take place in parallel with the incoming of a next event, thus increasing the overall speed by another factor 2. This scenario will probably be addressed in 2009.
In addition, the MimoTEL could be run at a higher clock frequency (20 MHz instead of 15 MHz). This would reduce the readout and processing to about 970 μs and the block transfer would then be the dominant factor. Block transfers could then still be further improved by using the full speed VME 2e SST protocol with a bandwidth of about 160 MB per second, while currently we are only using the basic MBLT protocol running at about 80 MB/s and could thus win another factor 2.
These improvements are possible upgrades for the future and will be evaluated in 2009.

3 Towards the readout of the final chip

3.1 Description of TC/Mi26

The final sensor TC/Mi26 will have a total of 1152x576 pixels on an active surface of 21.2x10.6 mm^2. A single point resolution of about 3.5 μm is expected, resulting in an effective pointing resolution of about 2 μm on the surface of the DUT. The frame rate will be of the order of 10^4 frames per second, resulting in data throughput of up to 80 MBit per second for one sensor. The sensor has on chip zero suppression.

3.2 Needed changes to the DAQ framework

The higher frame rate of the final chip needs an adaption of the EUDRBs which is currently ongoing. To be able to cope with readout speeds above 1 kHz, additional changes to the DAQ software framework will be needed as well.
At this throughput, the block transfer of the data over the VMEbus starts to become the dominant factor. To achieve this, we need to:

- Decouple input and output buffers on the EUDRBs,
- add an output buffer for multiple events on the EUDRBs and
- implement the fastest possible transfer mode via VME (2eSST)

To further increase the speed, the telescope could be split on two VME crates to win another factor two.
As in the years before, the first priority is the integration of the final chip into the existing readout in a stable and reliable manner. Extensive tests in the laboratory and at the DESY testbeam are foreseen in early 2009. Speed and performance will be addressed as 2nd priority. Users in summer 2009 will be able to use the final chip at an increased speed.

4 Conclusion

In 2008, the JRA1 DAQ software framework has been used extensively by lots of different users. After the test beam campaigns, the readout speed has been significantly improved, going from about 50 Hz up to 400 Hz in the current design. A further factor two improvement is possible with a small firmware change.
The priority in 2009 is the implementation of the final sensor into the data acquisition system. Changes on the EUDRBs are currently ongoing and the first tests with the full chain will take place in early 2009.

Acknowledgement

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References

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