Integrated pixel readout for a TPC at NIKHEF

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Abstract

We report on present R&D activities at NIKHEF for the fabrication of a pixel readout TPC for the future International Linear Collider.
Latest NIKHEF activities involve the fabrication and testing of integrated Micromegas structures (InGrid) on top of Timepix chips. A beam test at the PS/T9 at CERN has been performed succesfuly. Other new structures as well (GEMgrid and Twingrid) are under study.
The protection of the Timepix chips against discharges by means of high resistive materials has been successfully applied using silicon rich nitride (SiRN) in Ar and He based gas mixtures.

1 Timepix chamber

Research activities at NIKHEF for a pixel readout TPC follow the direction of combining a pixel readout chip like Timepix, covered with a discharge protection layer, with a an integrated Micromegas structure (Ingrid) on top [1].It has been shown that this combination is able to survive discharges that could otherwise destroy the naked chips. Tracks from minimum ionizing particles have been recorded in helium and argon based mixtures.

With these detectors we have performed beam tests at the PS/T9 line at CERN. Two Timepix chips, one covered with 15µm a-Si and the second one covered with 20 µm a-Si were tested with pions and electrons. Five different gas mixtures were used, namely Helium/Isobutane (77/23), Argon/CO_2 (70/30), Argon/CF_4/Isobutane (95/3/2) and Xenon/CO_2 (70/30). Tracks are shown in figure 1. The first detector with 15µm a-Si was damaged by a discharge when operating the grid at -490V in the Xenon/CO_2 mixture. The rest of the measurements were performed with the chip with 20µm a-Si protection layer. The device was operated with a radiator in front and transition radiation could be observed.

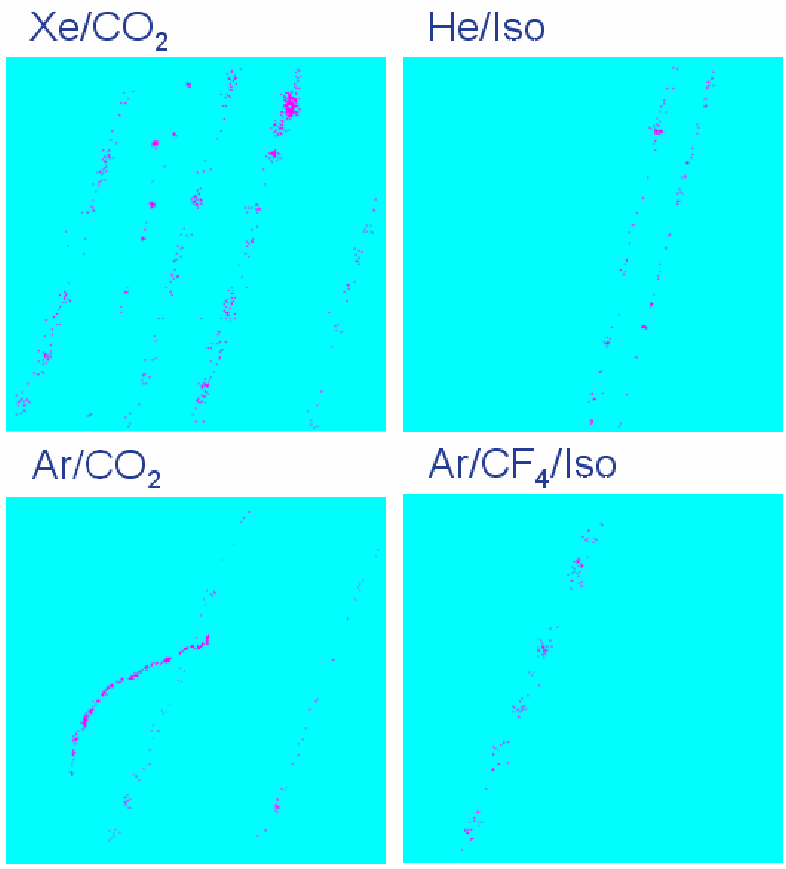

Figure 1. Tracks in several gases recorded with a Timepix chip equipped with Ingrid during the beam test at CERN.

Timepix chips equipped with Ingrid are currently produced by post-processing single chips, which limits the number of chips that can be delivered. A collaboration effort is currently ongoing between MESA+ University of Twente, NIKHEF, SMC (Scottish Microelectronics Center, Edimburgh) and IZM Berlin to post-process full size 8 inche Timepix wafers. As an intermediate step, chip squares containing 9 chips will be processed, producing 9 Ingrids in the same time that it takes to post-process a single chip.

2 Silicon rich nitride protection layer

From previous experience it is known that a layer of about 15 µm a-Si on top of the Timepix chip is needed to protect the chip against the discharges. At NIKHEF we have also tested the properties of silicon rich nitride as anti spark layer.
Silicon nitride (Si_3N_4) is an insulator material commonly used in microelectronics to passivate the top layer of microchips and it is used as anti-scratch layer. By adding a certain amount of silicon to the material, the stechiometric ratio is changed and the material is converted into silicon rich nitride (SiRN), which is highly resistive and the resistivity can be tuned depending on the added silicon.
This material is deposited by plasma enhanced chemical vapor deposition (using a mixture of silane and ammonia) at 300 °C on top of the Timepix, well safe for the CMOS chip. Several chips have been covered with different thicknesses of SiRN from 7.2 µm (see figure 1) to 2.4 µm and the resistivity is controlled with the silane to ammonia ratio. This anti-spark protection can be easily incorporated in future Timepix designs as the final CMOS silicon nitride anti-scratch layer could be converted by the foundry into silicon rich nitride and not perform the last etching step to open windows to reach the pixels to later on bump bond the silicon sensor. This way the foundry could procure chips ready to be post-processed for gaseous detectors applications.

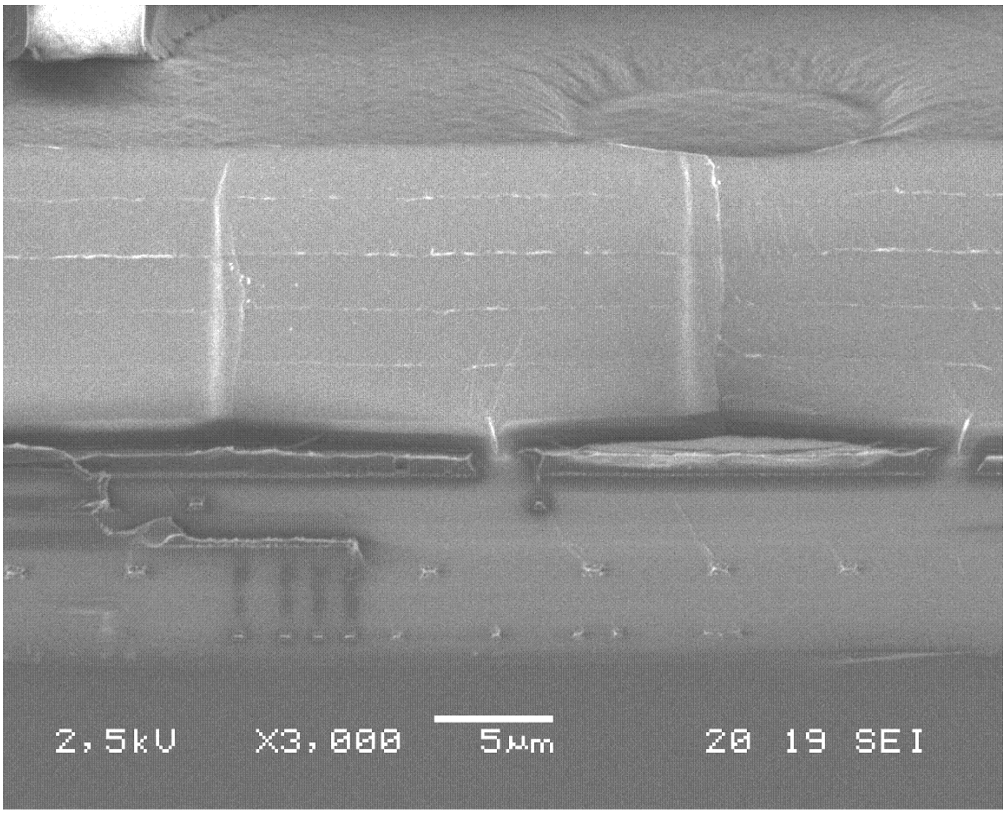

Figure 2. Cross section SEM picture of a pixel of a Timepix chip covered with a layer of silicon rich nitride.

To asses the anti spark performance of these anti-spark layers a Micromegas foil was mounted on top of a Timepix chip covered with 7.2 µm SiRN. The grid voltage was raised to -520V in a a Ar/Isobutane (80/20) mixture and the chip was not destroyed, although discharges were observed as well (figure 3), certifying the protection provided by the layer. More studies will be done with thinner layers to determine the minimum thickness needed.

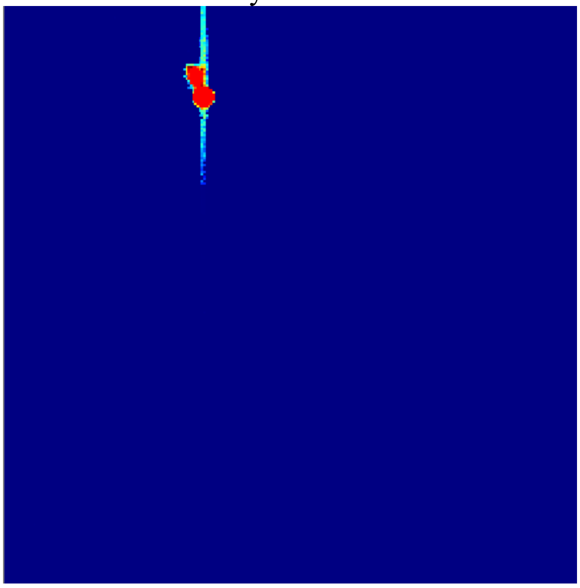

Figure 3. Image of a spark recorded with a Timepix chip protected with 7 μm thick SiRN layer and operated with a Micromegas foil on top.

3 New devices

New detector structures have been developed following the same fabrication scheme as for the integrated Micromegas. A GEMgrid structure (figure 4), similar to the Microbulk Micromegas [2], consists of a punctured metal foil supported by insulating walls. This kind of structure provides higher mechanical robustness than an Ingrid and allows to align the holes of the grid to the pixels of the chip. Single electron efficiency in this device seems to be slightly lower than for Ingrid structures. Tracks from cosmic rays have been recorded in Helium/isobutane (77/23) mixture.

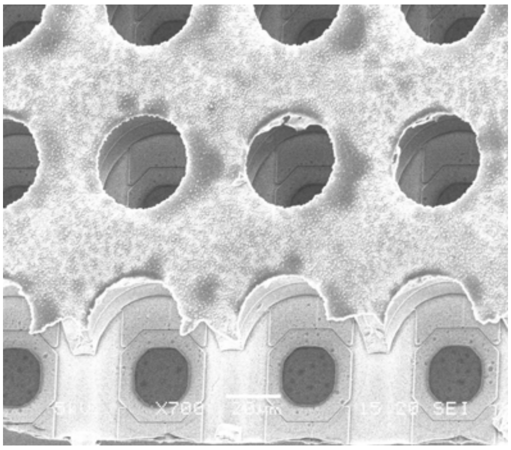

Figure 4. SEM picture of a GEMgrid device on top of a Timepix chip: a punctured metal foil is supported over the chip by means of insulating walls.

Another concept under investigation is the use of multilayer structures, similar to a double or triple GEM [3]. Figure 5 shows a design of a double layer structure on top of Timepix chip, ^{55}Fe has been recorded using this device and the gain can be divided between the two stages. A Timepix chip with this structure was destroyed after 5 hours of operation; more studies should be done about the spark behavior of these structures to determine the needed thickness of the induction gap in order to eliminate sparks over the chip.

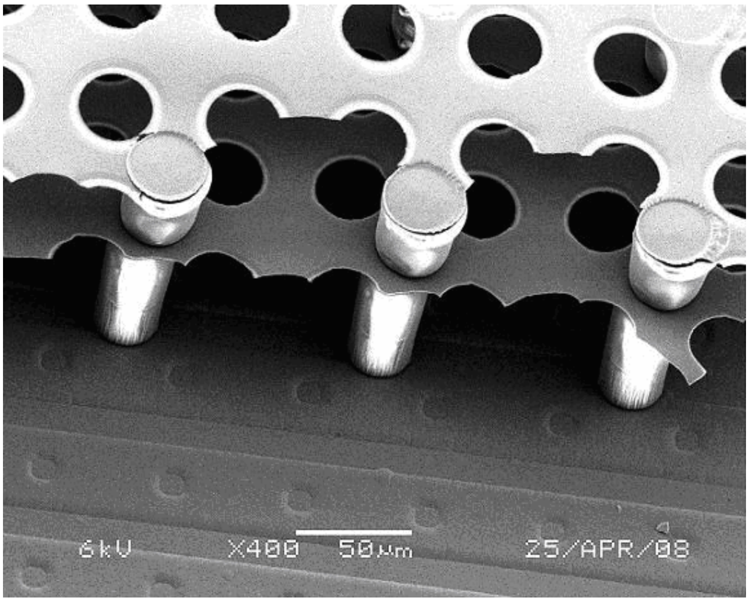

Figure 5. SEM picture of a double layer structure over a Timepix chip, gain can be divided along both stages.

Acknowledgement

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References

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