Description of the JRA1 Trigger Logic Unit (TLU), v0.2

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Abstract

This document describes the interfaces and operation of the EUDET JRA1 Trigger Logic Prototype (TLU v0.2a) with firmware version 241. The TLU is intended for test-beam use and provides a simple interface between the beam-trigger, the DAQ and the device-under-test[2].

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[2]Any good ideas are due to the collaborative efforts of members of the JRA1 working group. Any errors in documenting or implementing them are due to the author.

1 Introduction

The TLU is based around an “off-the-shelf” FPGA board[1]. It has LVDS and/or TTL interfaces to the beam-telescope readout and any devices under test, PMT signal and/or NIM level signal interfaces to the beam-trigger and a USB interface to the DAQ. The most up-to-date version of this document can be found at https://svn.phy.bris.ac.uk/svn/uob-hep-pc017a/trunk/www/Docs/tlu_v0_2_manual_eudet_note.pdf (username/password = anonymous/anonymous). The TLU v0.2 is a development of TLU v0.1. Firmware and software written for TLU v0.1 can be used with the TLU v0.2 without damage, however the Busy input multiplexing can not be controlled (it defaults to the RJ45 inputs) and the LEDs can not be controlled with v0.1 firmware/software. Circuit schematics for the mother-board and LEMO-IO daughter-board are available online[2],[3].

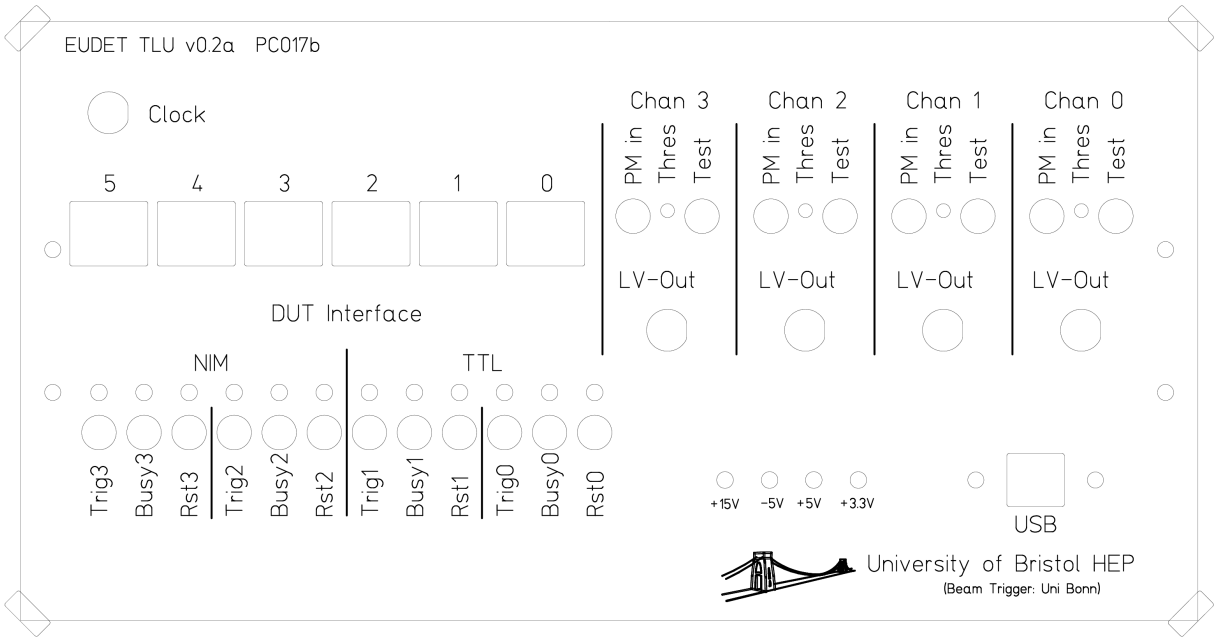
2 Power Requirements

5V @ 1A supplied on a 2.5mm connector on rear panel. Centre conductor positive.

3 Interface

4 Front Panel

The front panel for the TLU v0.2 is shown below:



5 Control

USB2.0 , “B” type connector on front panel.

6 Clock

There is a 2-pole LEMO-OB connector on the front panel for input or output of the internal clock. (the internal clock sets the “tick” for the trigger time-stamp). When used as an output the 100-ohm termination resistor R23 should be removed. Input can be either LVDS or LVPECL (3.3V referenced). Pin-1 (red dot) is the non-inverting signal. Not used by the current version of the firmware.

7 Beam Trigger

Four LEMO-00 single pole connectors on front panel, terminated into 50-ohms. Negative going pulses. The discriminator produces fixed length output pulses. If the pulses are too short and/or too close to the threshold narrow “glitches” rather than full length output pulses are produced. Pulse of greater than 3ns at -500mV are sufficient to produce correctly recognized pulses. The signal from the “Test” outputs can be used to monitor the output of the discriminators (terminate test outputs into 50-ohms at oscilloscope for a 21:1 probe of the discriminator output). Details of the discriminator unit can be found elsewhere[4].

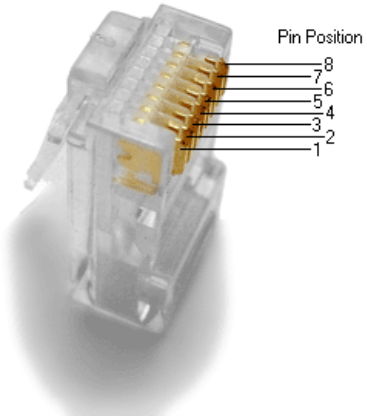
Four 2-pole LEMO-OB connectors, marked LV-out, provide power for internally powered PMT bases. By default a 15V DC-DC 300mA regulator is fitted, but this can be changed on request. Pin-1 (red dot) is positive.

8 LVDS DUT Interface[3]

Six RJ45 connectors on front panel, terminated into 100-Ohms. LVDS levels. Pin out at TLU:

1. DATA_CLOCK- (input to TLU)
2. DATA_CLOCK+ (input to TLU)
3. BUSY- (input to TLU)
4. RESET- (output from TLU)
5. RESET+ (output from TLU)
6. BUSY+ (input to TLU)
7. TRIGGER- (output from TLU)
8. TRIGGER+ (output from TLU)

Connector pins numbering illustrated the figure below:



1 LEMO DUT Interfaces

Four of the six DUT interfaces (0 to 3) can be connected to LEMO-00 connectors. Trigger, Busy and Reset but not Data-Clock signals are connected. Outputs (Trigger, Reset) can be active at the same time as the corresponding LVDS outputs, but only one Busy input (either the LVDS or the Lemo) can be active for each DUT. The source of the Busy input (LVDS / Lemo) is selected using the I2C bus (see section 17).

[3]There is an error in the note describing the TLU v0.1 dated 30th August 2007 and earlier. The pinout direction is reversed (ie. 1 is swapped with 8, 2 with 7 etc)

1.1 NIM LEMO DUT Interfaces

Lemo interfaces 2 and 3 use (pseudo) NIM levels.

The Busy inputs are terminated into 50-ohms to ground. The threshold is -0.5V. The busy inputs can tolerate indefinitely in input voltage of +/-5V. The reset and trigger outputs produce a 0V, -1V level when terminated into 50-ohms to ground.

1.2 TTL LEMO DUT Interfaces

Lemo interfaces 0 and 1 use 5V TTL levels.

The Busy inputs are terminated into 50-ohms in series with 100pF to ground. They are protected against negative voltages by a Schottky diode clamp and can tolerate indefinitely being driven with a NIM "1" level. They can be connected to 5V TTL signal levels or 3.3V TTL signal levels (with lower noise immunity).

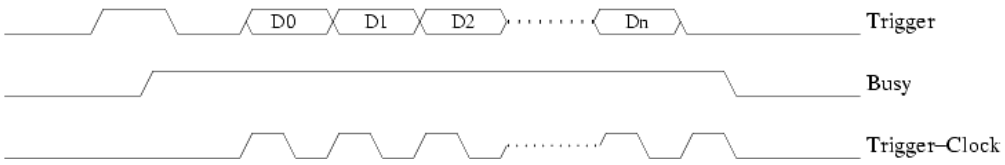
The Reset and Trigger outputs supply 3.3V LVTTL signals. They are series terminated by 50-Ohms and can tolerate indefinitely being shorted to ground. They can drive 50-Ohms to ground without damage, though in this case the high level output voltage is reduced due to the series termination by a factor of two.

2 Handshake between TLU and DUT

There are two modes of hand-shake between the TLU and the DUT. A "simple handshake" and a "trigger data handshake" where data is transferred from the TLU to the DUT on each trigger.

2.1 Trigger Data Handshake

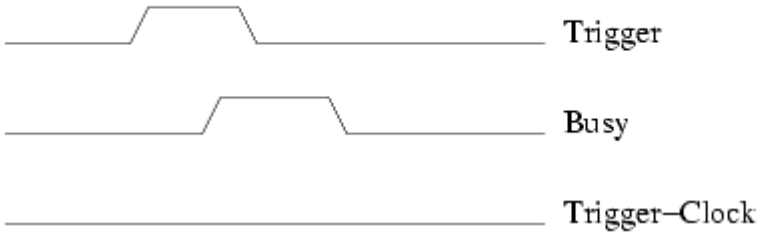
1) TLU receives trigger from beam scintillators
2) TLU asserts TRIGGER
3) On receipt of TRIGGER going high, the detector asserts BUSY
4) On receipt of BUSY going high, TLU de-asserts TRIGGER and switches the TRIGGER line to the output of a shift register holding the trigger number/data.
5) The DUT clocks data out of the shift register by toggling TRIGGER_CLOCK. Data changes on the rising edge of TRIGGER_CLOCK[4]. The least significant bit of the trigger data is shifted out first.
6) After clocking out the trigger number (and the detector being ready to take more data, the DUT de-asserts BUSY)
7) System is ready for triggers again.



[4]The Trigger-Clock line is sampled by the 48MHz internal clock and the rising edge used as a clock enable for a shift register clocked by the 48MHz internal clock. Hence the Trigger-Clock should be less than 24MHz. The practical maximum frequency of Trigger-Clock is in the region of 10MHz.

2.1 Simple Handshake

1) TLU receives trigger from beam scintillators
2) TLU asserts TRIGGER
3) On receipt of TRIGGER going high, the detector asserts BUSY
4) On receipt of BUSY from DUT, the TLU de-asserts TRIGGER
5) On receipt of TRIGGER going low and the detector being ready to take more data, the DUT de-asserts BUSY
6) System is ready for triggers again.



(state of Trigger-Clock is irrelevant in this mode)

1 Trigger Latency

The time interval between the beam-trigger arriving at the TLU and trigger(s) being issued to the DUT(s) is 27.3 +/- 3 ns. The uncertainty is an indication of the difference in the delay time between different DUT outputs (different logic routing inside the FPGA) and shifts due to fluctuation in temperature and supply voltage.

The discriminators used are housed on a daughter-board and are of a fixed-threshold design. There will be “timing-walk” (variation in latency) with varying pulse heights. With negative going pulses of 1ns fall-time the latency varies by about 1ns for pulse heights between -100mV and -600mV

For a given DUT output at a fixed pulse-height, temperature and supply voltage the fluctuation in trigger latency between successive triggers is much lower than this. This trigger latency jitter is 31ps RMS, measured the lab. Electrically noisy environments may result in a larger jitter than this.

2 Using BUSY line to veto triggers

The DUT can raise the BUSY line outside a Trigger/Busy handshake sequence. If this is done no further triggers are issued by the TLU until the BUSY line is brought low again. However, the DUT should monitor the TRIGGER line, since due to the latency in the cable between DUT and TLU there is a “race” condition where the TLU issues a trigger simultaneously with the DUT raising the BUSY line. It is not possible to eliminate this race condition, but it is possible to detect it and flag the corresponding trigger. In future it may be decided to use the TRIGGER_CLOCK line for the DUT to signal to the DUT that is is busy, this would allow the TLU to detect the race condition and respond appropriately.

3 Control Interface

The ZestSC1 FPGA module uses a Cypress EZ-USB micro-controller to implement a USB 2.0 interface. There are two modes of operation – register and block transfer. The register interface is one byte wide. The block transfer mode transfers blocks of 16-bit words.

4 Address Map

Table 1 gives the address map for register mode transfer (the names refer to constants defined in TLU_address_map.h and TLU_address_map.vhdl)

Location	*Read/ Write*	*Function*
BUSY_REG_ADDRESS	R	Value of the busy lines coming from DUTs
DUT_RESET_ADDRESS	W	Asserts reset line on DUTs for one clock cycle.
DUT_TRIGGER_ADDRESS	W	Asserts trigger line on DUT for one clock cycle. Active even when beam-triggers have been inhibited by writing to TRIG_INHIBIT_ADDRESS. Activates TRIGGER/BUSY handshake
TRIG_INHIBIT_ADDRESS	R/W	Writing '1' to bit 0 (LSB) vetoes triggers. Writing '0' to bit 1 re-enables triggers Reading gives current state of veto in bit-0 and current state of overall veto (including vetoes caused by beam_trigger) in bit-1
RESET_REGISTER_ADDRESS	W	Writing '1' to a bit issues a reset. Bit mapping: TIMESTAMP_RESET_BIT 0 TRIGGER_COUNTER_RESET_BIT 1 BUFFER_POINTER_RESET_BIT 2 TRIGGER_FSM_RESET_BIT 3
INITIATE_READOUT_ADDRESS	W	Puts block transfer state machine into INITIATE_TRANSFER state.
STATE_CAPTURE_ADDRESS	W	Writing causes BUFFER_POINTER, TIMESTAMP, TRIGGER_COUNTER and TRIGGER_IN counters to be copied to registers ready for reading,
TRIGGER_FSM_STATUS_ADDRESS	R	Status of the finite state machines controlling the trigger outputs. 0=idle, 1=busy. One bit per DUT.
REGISTERED_BUFFER_POINTER_ADDRESS_0	R/W	Next location of time-stamp buffer to be written. 0 is LS-Byte, 1 is MS-Byte. Updated when STATE_CAPTURE_ADDRESS is written to
REGISTERED_BUFFER_POINTER_ADDRESS_1	R/W	
REGISTERED_TIMESTAMP_ADDRESS_0	R	64-bit value of the time-stamp captured when STATE_CAPTURE_ADDRESS is written to.
REGISTERED_TIMESTAMP_ADDRESS_1		
REGISTERED_TIMESTAMP_ADDRESS_3		
REGISTERED_TIMESTAMP_ADDRESS_4		
REGISTERED_TIMESTAMP_ADDRESS_5		
REGISTERED_TIMESTAMP_ADDRESS_6		
REGISTERED_TIMESTAMP_ADDRESS_7		
REGISTERED_TRIGGER_COUNTER_ADDRESS_0	R	32-bit value of trigger-counter
REGISTERED_TRIGGER_COUNTER_ADDRESS_1		
REGISTERED_TRIGGER_COUNTER_ADDRESS_2		
REGISTERED_TRIGGER_COUNTER_ADDRESS_3		
BEAM_TRIGGER_AMASK_ADDRESS[5]	R/W	AND mask for input triggers. Bottom 4 LSB significant. Writing 0x00 disables this trigger.
BEAM_TRIGGER_OMASK_ADDRESS[6]	R/W	OR mask for input triggers

[5]Triggers are “AND”ed together and then “OR”ed with the OR trigger.

Location	*Read/ Write*	*Function*
BEAM_TRIGGER_VMASK_ADDRESS[7]	R/W	VETO mask for input triggers
DUT_RESET_DEBUG_ADDRESS	R/W	Write static level to RESET outputs.
DUT_TRIG_DEBUG_ADDRESS	R/W	Write static level to TRIGGER outputs. Does not activate TRIGGER/BUSY handshake
DUT_CLOCK_DEBUG_ADDRESS	R	Read values of DUT_CLOCK lines
DUT_I2C_BUS_SELECT_ADDRESS	R/W	Selects which I2C bus is addressed
DUT_I2C_BUS_DATA_ADDRESS	R/W	Reads/Writes data to I2C clock and data lines.
INTERNAL_TRIGGER_INTERVAL	R/W	Interval (in milliseconds) between internal triggers. Writing zero disables internal triggers
CLOCK_SOURCE_SELECT_ADDRESS[8]	R/W	Selects the clock source used for time-stamp. Writing '0' to LS-Bit selects internal 48MHz clock. Writing '1' to LS-Bit selects front panel clock
TRIGGER_IN0_COUNTER_0	R	Number of pulses on input 0. Updated after each write to STATE_CAPTURE_ADDRESS
TRIGGER_IN0_COUNTER_1		
TRIGGER_IN1_COUNTER_0	R	Number of pulses on input 1
TRIGGER_IN1_COUNTER_1		
TRIGGER_IN2_COUNTER_0	R	Number of pulses on input 2
TRIGGER_IN2_COUNTER_1		
TRIGGER_IN3_COUNTER_0	R	Number of pulses on input 3
TRIGGER_IN3_COUNTER_1		
REGISTERED_PARTICLE_COUNTER_ADDRESS_0	R	Number of pre-veto triggers. (i.e. number of triggers that TLU would have issued if no dead-time)
REGISTERED_PARTICLE_COUNTER_ADDRESS_1		
REGISTERED_PARTICLE_COUNTER_ADDRESS_2		
REGISTERED_PARTICLE_COUNTER_ADDRESS_3		

Table 1: Address map of TLU for register mode transfers.

5 I2C bus

The multiplexing of the Busy inputs and the the indicator LEDs is using I2C. In order to give the possibility of adding extra daughter-boards controlled by the existing motherboard (specifically to give the possibility of adding an interface between the TLU and the Calice Clock and Control module) there are a number of separate I2C buses. With the current version of the firmware a “bit-banging” interface for the I2C SDA and SCK lines is used. Which I2C bus is selected is controlled by writing to the DUT_I2C_BUS_SELECT_ADDRESS register. Data is written to and read from DUT_I2C_BUS_DATA_ADDRESS. Table 2 shows the

[6]Writing 0x0F enables all beam triggers. Writing 0x00 disables all beam triggers (internal triggers are not affected). Triggers are “OR”ed together.
[7]Not implemented in version 241 of the firmware
[8]Not implemented in version 241 of the firmware.

format of the DUT_I2C_BUS_DATA_ADDRESS register. Table 3 enumerates the I2C devices.

5.1 Busy Input Multiplexing

For DUT interfaces 0..3 the source of the Busy input from the DUT can be selected to either be from the RJ45 connectors or the Lemo connectors (there is the possibility of selecting input from a Calice Clock and Control interface board, but the interfaces board has not yet been implemented). For example, to select RJ45 Busy inputs for DUT interfaces 0..3 write 0xFF to PCA9555 with address 3 on the motherboard I2C bus. To select lemo busy inputs write 0xAA. The Busy inputs for DUT interfaces 4 and 5 are always connected to the RJ45 connectors.

Bit	***R/W***	***Function***
0	W	Writing 0 pulls SDA line low.
1	R	State of SDA line.
2	W	Writing 0 pulls SCL line low
3	R	State of SCL line.

Table 2: Bit functions of DUT_I2C_BUS_DATA_ADDRESS register

Function	***I2C bus***	***I2C address***	***Description***	
RJ45 Leds	motherboard	0	LEDs 0..7 connected to IO0, LEDs 8..11 connected to IO1[3..0]	
RJ45 trigger outputs	motherboard	1	rj45_trigger_enable[3..0] connected to IO1[7..4] (DUT interfaces 4,5 are always enabled)	
Lemo trigger outputs	motherboard	1	lemo_trigger_enable[3..0] connected to IO1[3..0]	
RJ45 reset outputs	motherboard	2	rj45_reset_enable[3..0] connected to IO1[7..4] (DUT interfaces 4,5 are always enabled)	
Lemo reset outputs	motherboard	2	lemo_reset_enable[3..0] connected to IO1[3..0]	
Busy LVDS/Lemo select	motherboard	3	**DUT**	**Pins on PCA9555**
			0	IO0[1..0]
			1	IO0[3..2]
			2	IO0[5..4]
			3	IO0[7..6]
			“11” select RJ45, “10” selects lemo.	
LEMO green LEDs	Lemo	1	IO0[7..0]	
LEMO bi-colour LEDs	Lemo	1	IO1[7..0]	

Table 3: List of I2C devices. (All devices are PCA9555)

6 Readout sequence

When the TLU receives a trigger it writes the current value of the 64-bit time-stamp into a buffer and the BUFFER_POINTER is incremented. The trigger counter is also incremented. To order to perform an "atomic" read on the value of BUFFER_POINTER, TRIGGER_COUNTER and TIMESTAMP, write (any value) to STATE_CAPTURE_ADDRESS. The values are then captured and stored in REGISTERED_BUFFER_POINTER, REGISTERED_TRIGGER_COUNTER and REGISTERED_TIMESTAMP.

To read out the buffer of timestamps, the following sequence should be followed:

1) Write '1' to LSB of TRIG_INHIBIT_ADDRESS, this stops further triggers
2) Write any value to INITIATE_READOUT_ADDRESS
3) Use TLUReadData function on host to transfer content of time-stamp buffer to the host.
4) Write to bit '2' of RESET_REGISTER_ADDRESS to reset the buffer pointer (so that further timestamps are written at the start of the buffer)
5) Write '0' to bit-1 of TRIG_INHIBIT_ADDRESS to enable triggers.

1 Grounding and Shielding

The RJ45 connectors for the DUT interface allow shielded cable to be used. **It is recommended that shielded cable is used**. Unlike 10/100/1000-BaseT Ethernet where the signals are DC-balanced and can be AC-coupled, the interface between the TLU and the DUT is not DC-balanced and is DC-coupled. This limits the common-mode voltage between the DUT and TLU to less than +/-0.9V[9]. Excessive current flow through any ground loops formed should be reduced using careful layout of cables and extensive use of ferrite cores round the cables.

Acknowledgements

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4. http://svn.phy.bris.ac.uk/svn/uob-hep-pc017a/trunk/www/Docs/TLU_Discriminator_Board_Documentation.pdf

[9]Set by the sn65lvdm1676 transceivers used in the TLU. This common mode range will be even lower if the DUT has a lower common mode range.