EUDET-Memo-2010-13

The EUDET JRA1 Data Acquisition System – Past, Present and Future

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20th January 2011

Abstract

This memo gives an overview of the JRA1 Data Acquisition System (DAQ), and its evolution in the timeframe of the EUDET project. It gives a short description of the initial prototype that has been developed as 'proof-of-principle'. The 'real' system and its ingredients are then explained in detail as well as the upgrades to this system over the lifetime of EUDET. Some usage statistics of the EUDAQ software framework are presented, and an outlook is given how to migrate the DAQ to the FP7 project AIDA.

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1 Overview

JRA1 has been responsible for the creation of a user-friendly and accessible test beam infrastructure, including a pixel telescope for the qualification of different devices under test (DUTs). Within this joint research activity, the development of a competitive data acquisition system has been a main task. The initial requirements to the DAQ system have been:

- Readout of the pixel telescope;
- Readout of the DUTs
- Handle external data (run/beam-related);
- Easy integration of user-provided DUTs, either via hardware or software;
- Handle a readout rate of about 1 kHz;

The initial requests to the system have been relatively lightweight. Still scalability of the system at a later stage has been an important design driver. Modularity, flexibility, and OS-independence were other key factors in the design phase. The following sections describe the evolution of the JRA1 DAQ, the initial concept, the 'real' implementation and its upgrades over the lifetime of EUDET (and beyond).
Full description of the individual subsystems etc. can be found in the referenced memos and reports.

2 The Initial Concept

2.1 Schematic view

Figure 1a shows the initial concept of the telescope and acquisition system, with the chips being connected to a front-end board providing signal conditioning, sequencing and power. They are read out by a data reduction board that digitises the signals and performs correlated double sampling (CDS) and zero suppression. Data is then sent to a central DAQ PC for event building and storage.

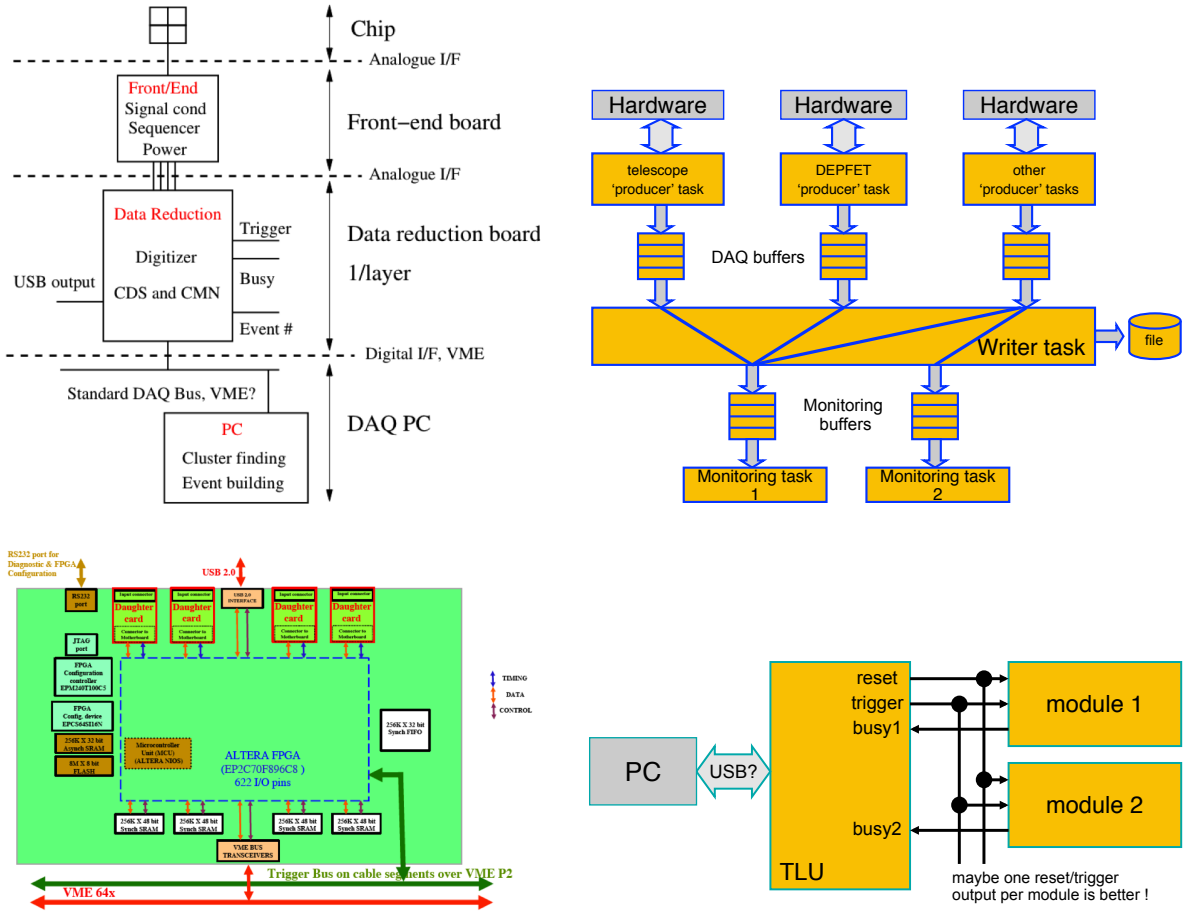

Figure 1: Initial concept:
a) DAQ overview b) Acquisition software
c) Readout electronics d) Trigger logic

The initial concept for the software is shown in figure 1b. Several 'producer' tasks read out the various pieces of hardware, and send data via a buffering system, to the central writer task that saves the data to disk and distributes information to the monitoring tasks. It was based on the DEPFET Mini-DAQ from Bonn/Mannheim, with the addition of an overall control task, communication over TCP/IP, and a method of detector

configuration. It was also designed to be modular, flexible and as far as possible, OS-independant.
It was decided that the readout electronics (figure 1c) would be based around an Altera FPGA on a VME card, with pluggable daughter cards for interfacing with the sensors providing maximum flexibility and adaptability to different sensors. Readout was planned via a choice of either VME or USB.
A trigger logic unit (TLU) was also envisaged (figure 1d), to distribute the trigger signal to the various modules, and handle their busy status. It was decided to base it on the Orange Tree ZestSC1 FPGA development board.

2.2 Proof of principle

Before starting the work on the actual acquisition software, a proof of principle system was built to show that the basic principles were sound. It was constructed by hacking the DEPFET Mini-DAQ to run on multiple machines and by combining it with the Mimosa readout software from Strasbourg. The resulting applications are shown running in figure 2.

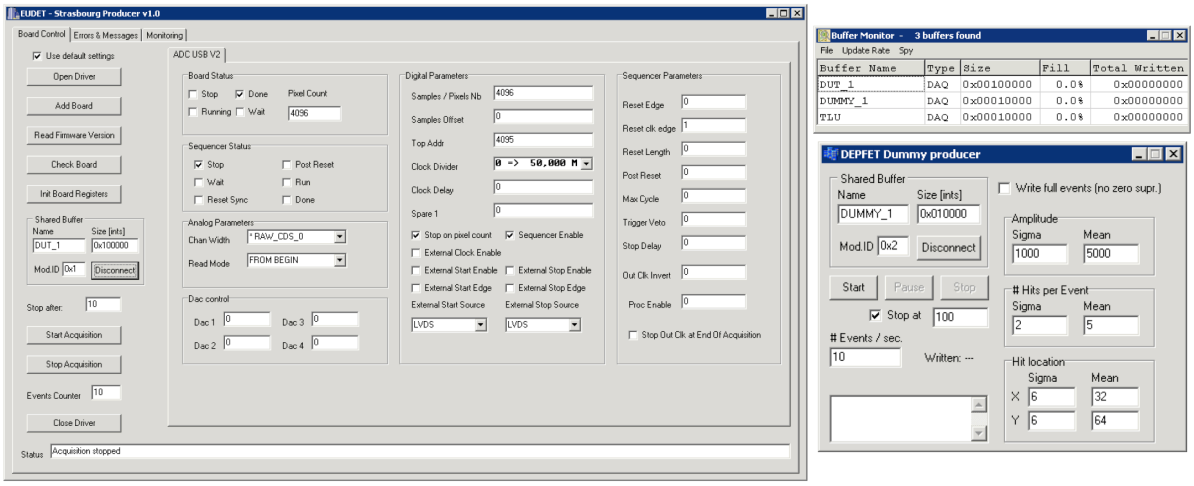

Figure 2: Proof of principle

The agressive initial timeline and Milestones (see figure 3) have been respected and maintained over the full time.

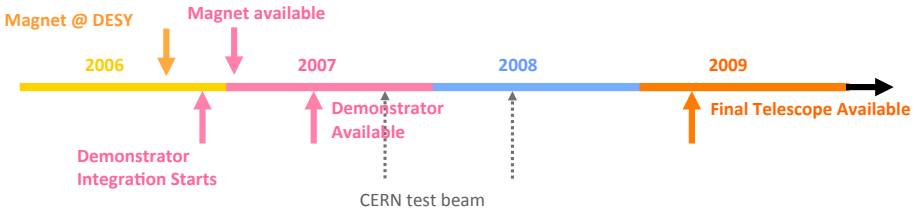

Figure 3: Time line

3 Full implementation of the JRA1 DAQ - The Main Ingredients

3.1 Trigger Logic Unit

The TLU[1] as shown in Figure 4a receives the trigger scintillator signals and combines them to generate a trigger signal that is distributed to the various front-end modules. It has four trigger inputs that are processed by discriminators and can be combined in an arbitrary fashion (ANDed, ORed and VETOed) to generate the resulting trigger signal. Each trigger input also has an independent low voltage power supply for powering PMTs. There is also an internal trigger generator used for testing and pedestal runs, as well as several internal scalers. For each trigger a timestamp is stored, that can be read out over USB by a PC.

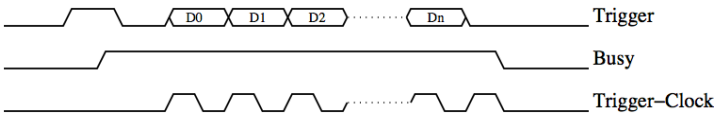

Figure 4: TLU: a) front panel b) protocol

It can communicate with up to 6 DUTs via either LVDS over RJ45, or NIM or TTL

over Lemo connectors, selectable by software. There are two basic handshake modes between the TLU and the DUTs. In the simplest method the TLU sends a trigger, and waits for the DUT to raise its busy signal. Once this happens the TLU drops the trigger and waits for the DUT to drop the busy. The DUT can hold the busy high as long as necessary until it is ready to process more triggers. The TLU will only accept further triggers once all DUTs have dropped their busy lines. The recommended handshake mode is shown in figure 4b. It is very similar to the basic mode, with the exception that during the busy period the DUT may toggle the clock line and for every cycle the TLU will send one bit of the trigger number over the trigger line, up to 15 bits. The DUT must clock out 16 bits to ensure that the trigger line is returned to the inactive state before dropping the busy line.
The TLU has been adapted to different user needs during the course of EUDET with a low jitter mode (for TPCs etc.), and an increased timestamp resolution and central clocking for LHC users.

3.2 EUDET Data Reduction Board

The ***EU***DET ***D***ata ***R***eduction ***B***oard[2][3], or EUDRB (see figure 5) contains the readout electronics for the Mimosa sensors. It consists of a 6U VME64X card with an Altera Cyclone II FPGA clocked at 80 MHz. The FPGA includes a NIOS II 32-bit soft microcontroller running at 40 MHz for diagnostics, pedestal and noise calculation, and for remote configuration. The interface to external electronics is provided by two daughter cards. A digital daughter card drives and receives control signals for the detectors and also provides a USB 2.0 link. An analogue daughter card, based on the successful LEPSI and SUCIMA designs, and clocked at 20 MHz, receives and digitises the data from the analogue sensors.

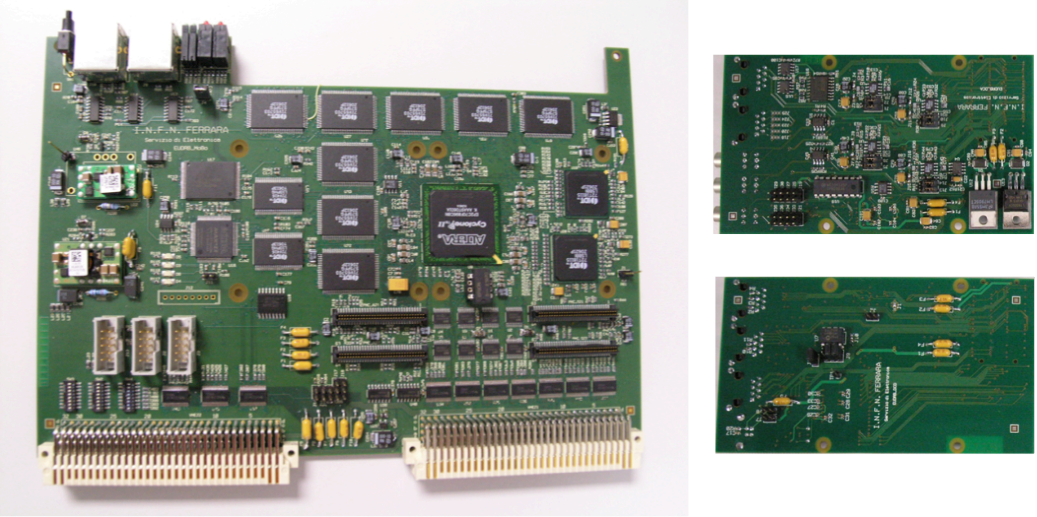

Figure 5: EUDRB: a) main board, b) analogue and c) digital daughter cards

The EUDRB provides two readout modes, zero-suppressed for normal data taking where the data volume is considerable reduced by removing pixels below threshold, and raw readout mode for debugging and offline pedestal and noise calculations.

3.3 EUDET Data Acquisition Software

The EUDAQ acquisition software[4] is a lightweight DAQ system designed to be modular and portable. The general architecture is shown in figure 6. All processes are controlled from the central Run Control process from which they receive commands and respond with their status. A number of Producer tasks communicate with the hardware and send any data to the central Data Collector task. The Data Collector merges the events from all producers and writes the resulting data stream to disk.

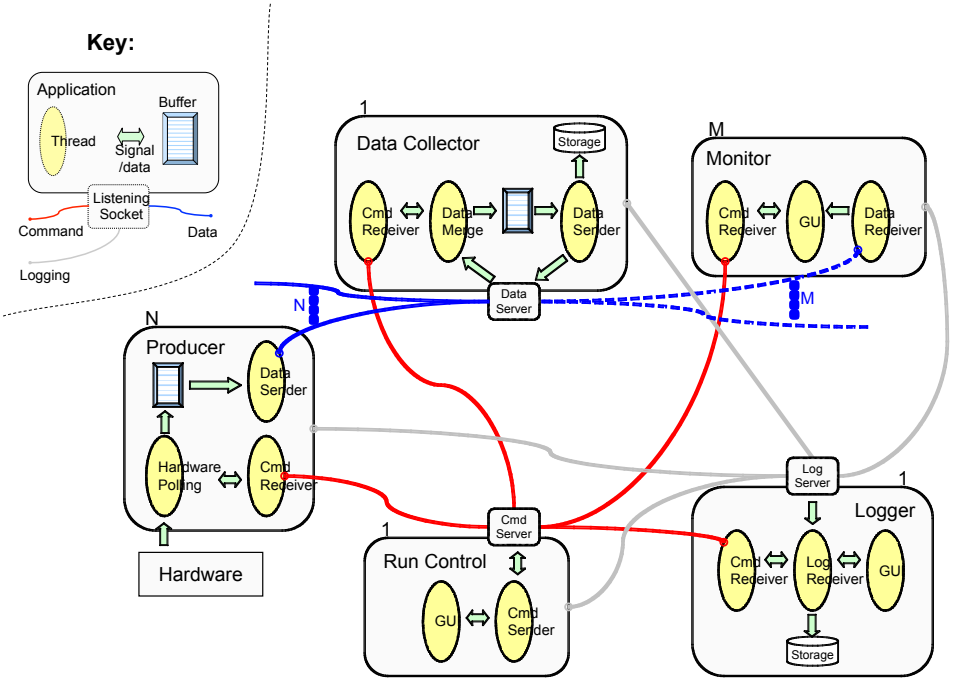

Figure 6: Acquisition software

Monitor tasks receive data from the Data Collector and generate histograms for the monitoring of data taking. This was originally planned to be sent over TCP/IP, but is currently just read from the data file on disk.
In addition, a central Log Collector task receives log messages from all other tasks, providing a central location for all log messages allowing easier debugging.

3.4 DUT Integration

The telescope is designed to be used by many different groups with different detector technologies and different pre-existing DAQ systems. In keeping with the EUDET philo-

sophy, the user is given a choice of options for integrating their DAQ, from a basic trigger-only connection, up to a full integration into the EUDET data stream (see figure 7).

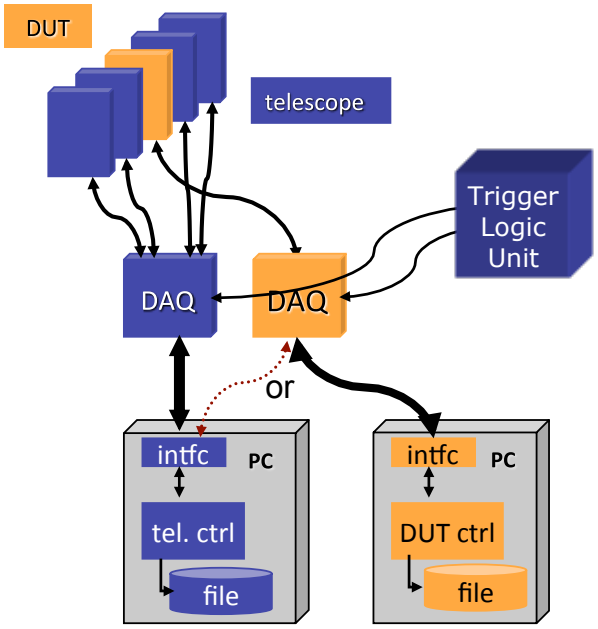

Figure 7: DUT Integration

As the EUDET DAQ has been improved, more users have integrated more fully. Users who have integrated with the EUDET DAQ include:

- Altro – Bonn (Martin Killenberg)
- APIX – Atlas Pixels (Georg Troska)
- DEPFET – Bonn (Julia Fourletova)[5][6][7][8]
- FORTIS/SPIDER – Bristol (David Cussans)[9]
- MimoRoma – INFN (Antonio Bulgheroni)
- MVD – DESY (Silvia Bonfanti)
- PixelMan – Freiburg (Uwe Renz)
- SITRA/SiLC – Santander (Javier Gonzalez Sanchez)[10]
- Taki – Mannheim (Christian Takacs / Ivan Peric)

- Timepix – Bonn (Martin Killenberg)
- Atlas TRT (Ilia Slepnev)
- CALICE, NA62, Alfa, ...

4 Past and Present

The demonstrator telescope[11] is shown (schematically, and a photo) in figure 8.

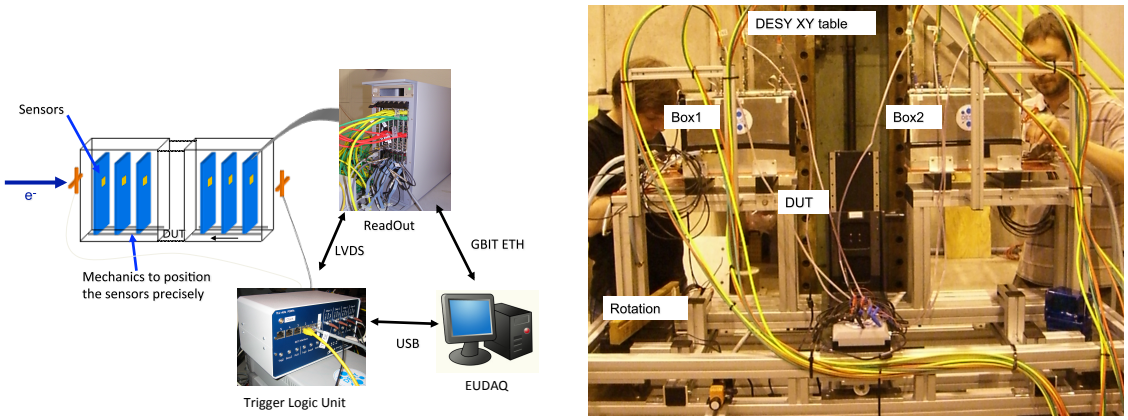

Figure 8: The telescope in the past

Converting the demonstrator into the final telescope (figure 9) involved replacing the old sensors (MimoTEL and Mimosa 18) with the new Mimosa 26 sensors[12][13][14], a major upgrade of the EUDRBs[15] including both extensive firmware changes and additional hardware[16], along with upgrading the DAQ software and analysis chain[17] to handle the new hardware. In addition the TLU also received many upgrades and improvements[18].

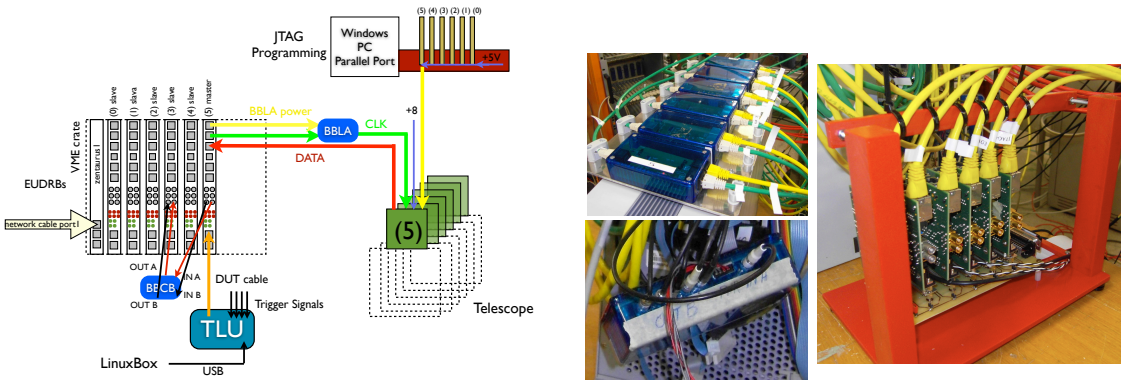

Figure 9: The telescope at present

5 Some numbers about the EUDAQ software framework

The EUDAQ software was first checked into a Subversion repository in February 2007[19]. At the time it consisted of about 30 source files. There are now more than 350 source files in the trunk, containing more than 30 kloc (thousand lines of code).
There have been over 1000 revisions to the code by 6 developers registered at HepForge, as well as changes from others not registered (for example sent by email).

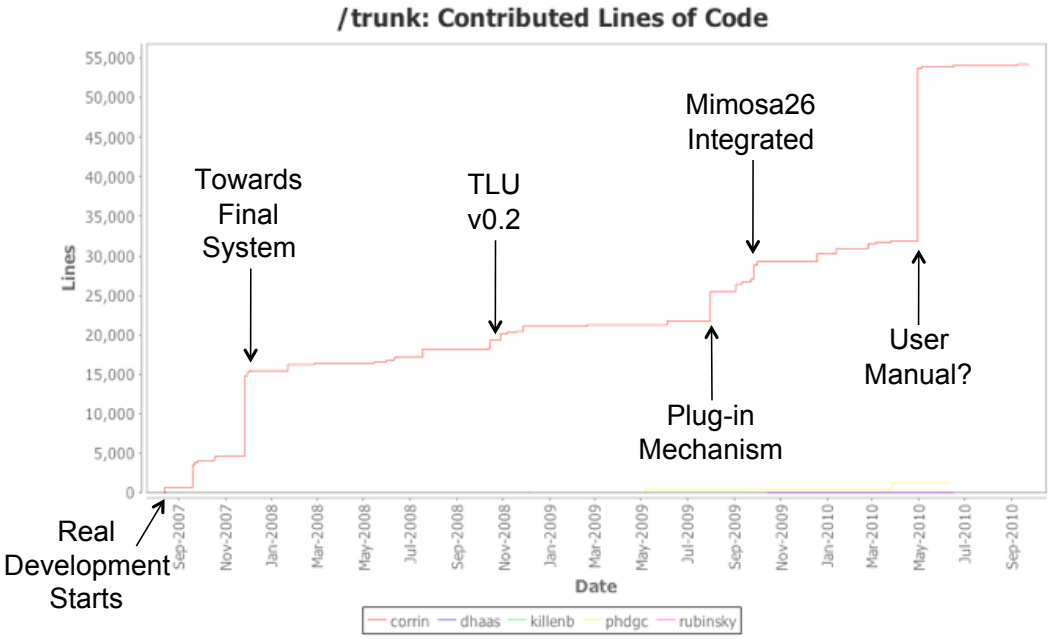

Figure 10: EUDAQ software repository growth

Figure 10 shows the growth of the EUDAQ framework over time, while the activity in the repository by day of the week and by hour of the day is shown in figure 11.

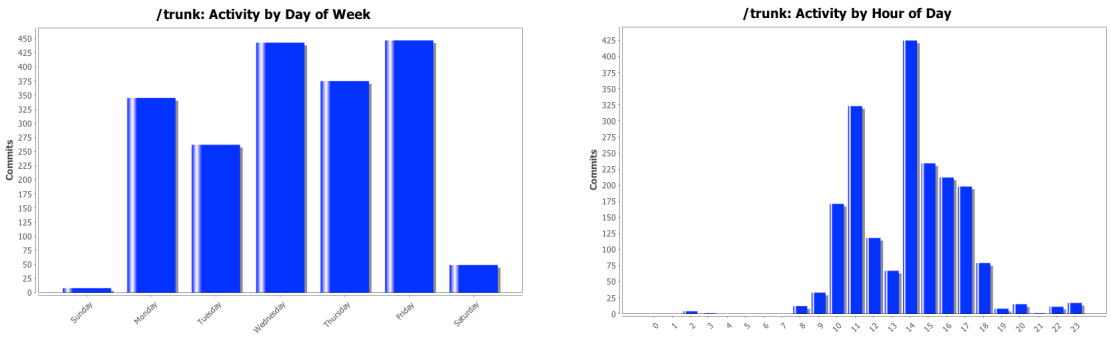

Figure 11: Repository activity by a) day of week and b) hour of day

6 Outlook to AIDA

AIDA will be an order of magnitude larger than EUDAQ, which will have implications both on the hardware, and the software.
The EUDRBs cannot scale to the needed level. They will be replaced with a commercial readout based on National Instruments boards, that is already under development (see figure 12).

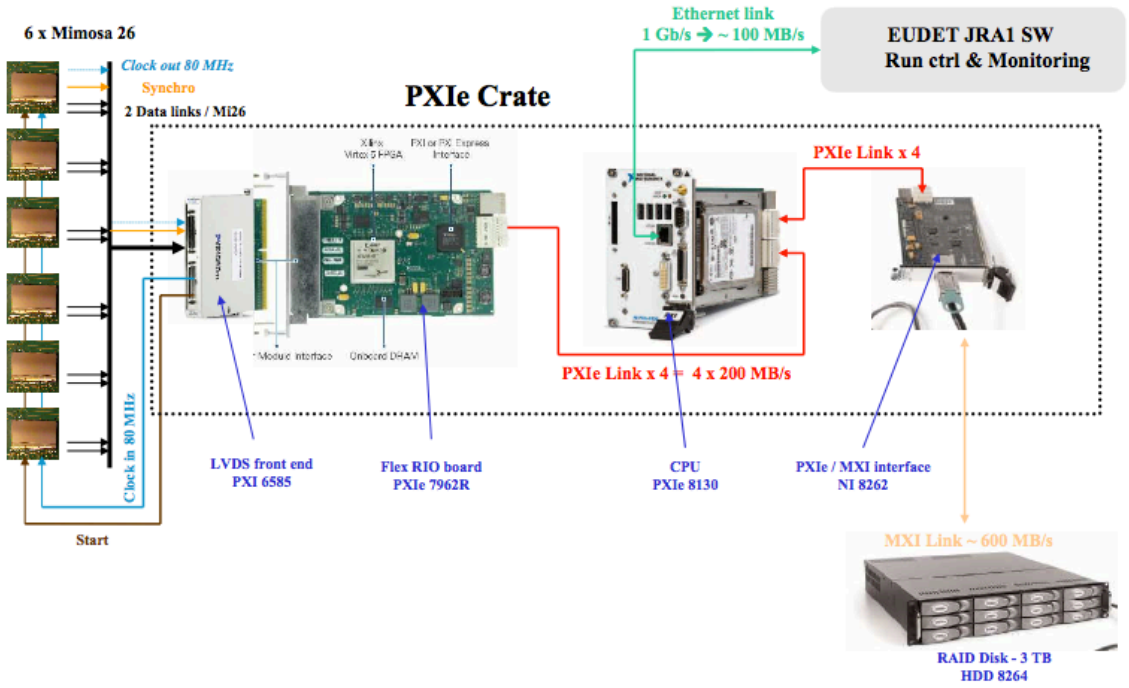

Figure 12: Proposal of DAQ based on Flex RIO[20]

The EUDAQ software can scale, but is now starting to go into competition with the 'big beasts' such as XDAQ[21].
A common effort is needed to streamline these changes, and it must start now.

7 Conclusion

It has often been asked why we build another beam telescope within EUDET, when everybody can do this themselves, or has already done it. But the EUDET beam telescope has been designed with the user in mind. Over the last 3 and a half years it has seen 84 weeks of use by about 30 different users. It has been running basically non-stop at CERN and DESY for the last 3 or 4 testbeam seasons, collecting more than 300 million events in 2010 alone.
The TLU has been a major selling point, providing a common starting point for integration. The EUDAQ software has been extremely successful, running with up to 8 DUTs,

and sometimes two different DUTs from different communities simultaneously. As the software has improved, it has become standard for users to integrate fully into the DAQ framework.
The old MVD telescope at DESY has been converted to run with EUDAQ, and copies of the EUDET telescope are already planned[22].
Overall, the activities within JRA1 have been a lot of fun, and even more work. The community building and transnational access aspects, although viewed suspiciously in the beginning, have proven very productive for JRA1.
The efforts of EUDET will be continued with AIDA, and hopefully it will profit from the achieved results.

Acknowledgement

This work is supported by the Commission of the European Communities under the 6$^{\text{th}}$ Framework Programme "Structuring the European Research Area," contract number RII3–026126.

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