

Milestones/Deliverables

2006

JRA1-C1

Small Digital Chip Prototype 1

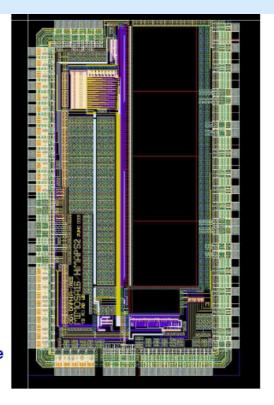
Fast Column Parallel Architecture

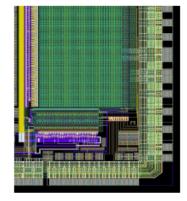
MIMOSA-16 design features :

- Fab. via STAR engin. run (Summer '06)
- AMS-0.35 OPTO translation of MIMOSA-8

 \hookrightarrow \sim 11–16 μm epitaxy instead of \lesssim 7 μm

- ullet 32 // columns of 128 pixels (pitch: 25 μm)
- on-pixel CDS (repeated at end of each column)
- discriminator at end of each column
- 4 sub-arrays :
 - \divideontimes 2 like MIMO-8: 1.7x1.7 & 2.4x2.4 μm^2 diodes
 - * 1 with ionising radiation tol. pixels
 - $\mbox{\ensuremath{\#}}$ 1 with enhanced in-pixel amplification (against noise of r.o. chain) & 4.5x4.5 μm^2 diode





24 col. with discri.

Status and Plans :

- ullet back from foundry < end Oct. '06 \longmapsto lab tests \gtrsim Nov. '06 (DAPNIA) \longmapsto beam tests \gtrsim Summer 2007
- next generations :
 - st small prototype (48+16 col. ? of 256 pixels, \gtrsim 16 μm pitch, optimised pixels)
 - * small prototypes with ADCs replacing or downstream of discriminators

JRA1-A1

Magnet





















