



SiLC R&D: design, present status and perspectives*

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Abstract

This paper briefly describes the main R&D objectives that are undertaken within the international R&D collaboration SiLC aiming to build the next generation of Silicon tracking devices especially in the case of the ILC.

1 Introduction

Over the last decade a consensus has emerged in the community of particle physicists that a high-luminosity high-energy electron-positron collider (now known as ILC - International Linear Collider) is an essential step on the road of understanding the standard model of particle physics and its limitations.

The enormous statistical power of the ILC machine and the favourable background conditions should be matched by a precision detector which is capable of taking collision data with the least possible introduction of biases and systematic errors. The required resolutions are challenging for most of the subsystems. In particular the reconstruction of hadronic final states requires an unprecedented jet energy resolution. Currently several overall detector concepts are studied. The main differences are in the choices for charged particle tracking and in the magnetic field and inner radius of the electromagnetic calorimeter. The SiD [1] concept employs a 5 T magnetic field and an all-silicon tracking system. The LDC [2] concept has a 4 T field and relies on a large time projection chamber (TPC) supplemented by few layers of silicon detectors for tracking. In the GLD [3] concept a 3 T magnetic field is compensated by an even larger calorimeter radius. While both in SiD and LDC a Silicon-Tungsten electromagnetic calorimeter (ECAL) with 1 cm² cells is foreseen, GLD relies on a scintillator - Tungsten ECAL with crossed 14 cm² scintillator tiles. Recently 4th concept [4] was presented differing namely in calorimetry and muon system.

The requirements for charged particle tracking are mainly high efficiency, robustness, and good double track resolution. Here momentum resolution is less important. However for some important physics channels very high momentum resolution ($\sigma(1/p_t) = 5 \times 10^{-5} \text{ GeV}^{-1}$) has to be achieved, approximately a factor five better than achieved at LEP. The current ideas are described in the following sections.

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2 Silicon Tracking at ILC

Two complementary approaches to achieve requirements posed on the ILC detector tracker are pursued: Silicon strip detectors which give a small (≈ 5) number of very precise (few micrometers) space points or a huge TPC with at least 200 space points of moderate ($< 100\mu\text{m}$) point resolution. In the case of Silicon tracking the major challenges are to achieve the desired point resolution with a minimum of material to reduce multiple scattering and photon conversions.

In the existing detector concepts various options are proposed: the SiD concept intends to use purely silicon as a sensor technology for most sub-detector systems. The SiLC collaboration [5] has proposed for the detector concepts that have a TPC as central tracking (i.e. LDC and GLD concepts) to complete this tracking system by a system of Silicon trackers that is called the "Silicon envelope" [6]. It consists of silicon sensors in the endcap region (ECT), in the innermost central (SIT) and forward (FCH) parts and in between the TPC and the central e.m. calorimeter (SET).

Silicon layers surrounding a TPC could provide for improved momentum resolution, improved interfacing to the calorimeter and vertex detector, and act as a robust fiducial for the calibration of the TPC (see Fig.1). On the other hand, current all-silicon tracking designs are expected to exhibit a precision fully competitive with that of gaseous tracking options, while offering the potential for a substantial savings in material (particularly in the forward direction), a more straight-forward calibration procedure, and greater resistance to backgrounds and aging.

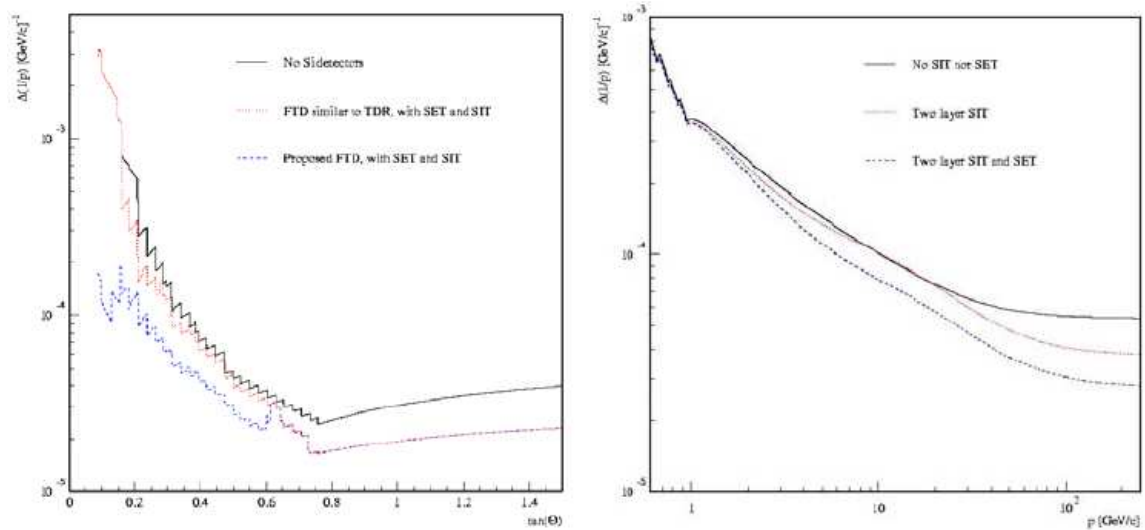


Figure 1: Effect of supplementary silicon tracking on the momentum resolution as a function of angle (left) and momentum (right)

3 Sensors

The current concept of a silicon tracker utilizes state-of-the-art technologies in all aspects of the design. In the sensor part, the baseline consists of microstrip sensors, built from larger size wafers (at least wafer of 8 inches), single and double-sided, and thinned by a factor 2 or 3. Therefore the thickness of sensors planned for ILC is a matter of studies. However, new pixel technology might be of interest in particular for the second layer near the vertex detector in the central inner part. Currently similar sensors fabricated for Glashow and CMS are being used for module building. Design and production of dedicated SiLC sensors is planned for 2007.

4 Electronics

The readout electronic system should not degrade significantly the intrinsic detector performance within the environment of the ILC detectors, matching therefore several constraints: comply the duty cycle of the ILC machine, ensure an electronics MIP to noise ratio of 25 at $3 \mu\text{s}$ shaping time, provide a continuous stream of lossless compressed digital data at the end of each bunch train. At the same time the electronics should dissipate a total average power under 15 W, minimize the on-detector total material regarding transparency to radiation and ensure the reliability of the whole system.

The general architecture of the front end chip (see Fig. 2) is based on a low noise preamplifier, a pulse shaper, a zero suppression decision, a sampling analogue pipe-line, an analogue to digital converter, a digital buffer, an internal calibration, and a power switching circuitry for power cycling. Two ranges of shaping times are implemented, namely a "slow" shaping time between 500 ns and a few μs , and a "fast" shaping time focusing on a few tenths of ns, in order to obtain a rough measurement of the z coordinate along the beam axis. This fast shaping time could also be used to provide a fine BCO tagging in case of high occupancy in some regions. As one of the first results of the

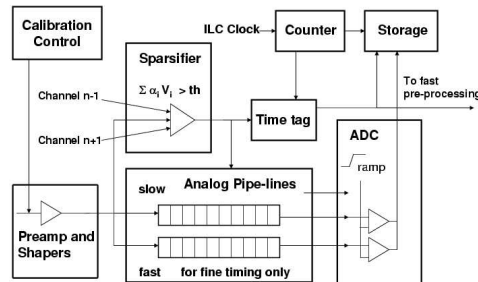


Figure 2: Front end architecture of a proposed SiLC chip

SiLC R&D program, a test chip in 180 nm CMOS technology has been designed and tested. Results have been encouraging concerning the main specifications such as noise and power. It confirms that a power dissipation below 1 mW/channel for the system from the preamplifier to the end of the front-end chain described above is achievable [7].

Notation	sensor	pitch [μm]	total length [mm]	FE electronics
A	GLAST	228	900	228 nm + VA1
B	CMS	183	283.5	180 nm + VA1
C	CMS	183	283.5	VA1 (reference)

Table 1: Characteristics of the module prototypes and their associated F.E. electronics

These chips have been built into two modules and their performance under realistic beam conditions is under study. As a further step, prototype chip in the 130 nm technology was designed and produced and it is now under tests. If successful, its version for 128 channels will be submitted and built into module prototypes in 2007.

5 Mechanics and alignment

The aims of the R&D on mechanics are low material budget, easiness of construction (simple modular structure, transfer to industry), robustness, low cost and easy integration issues. Various geometry options are under studies with the help of simulation systems. Simplicity of construction is foreseen to be achieved thanks to several innovative features (the large size of the sensors, the front-end chip directly sitting on the detector).

The conceptual design of infrared laser alignment system is built on its successful application to the AMS-1 tracking system [8], and on the current developments for the CMS silicon tracker alignment. According to the AMS experience few micron precision can be achieved.

6 Module prototypes

Several modules have been built using various sensor and chip generations during last years. Summary of 3 recent prototypes is at the Table 1. Here several features foreseen for the final detector have been implemented (both mechanical and electronic) to evaluate their performance and usability.

The modules built have been tested at a test bench in Paris using signal generated from laser stimuli.

7 Beam test

Further performance evaluation has been done at the first SiLC beam test which took place in October 2006 in DESY, within both the SiLC R&D program and the EUDET E.U. project [9]. Here modules were placed in the specially designed Faraday cage and tested in the beam of 1-6 GeV positrons. The beam position was monitored by the set of telescopes (6 planes of 50 μm pitch strip detectors). The track precision in the setup used

has been limited by several factors, namely by multiple scattering of low-energy beam and not optimised geometry. The detailed analysis of the beam data has only started, but one can state already now, that the precision obtained was sufficient to reliably distinguish between true hits and noise events and already allowed to determine the signal-to-noise ratio for the reference prototype. The main goal, though, is to achieve the same results with the two other modules that are read out with the new 180nm UMC chip. Regardless to its limitations the 2006 beam test was very important in development of test methods, DAQ synchronisation, event matching, analysis software, etc. The methods developed will be used in future beam tests planned both at DESY and CERN.

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