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HCAL mechanical design and electronics integration

Erika Garutti, Karsten Gadow, Peter Goettlicher,Mathias Reinecke, Felix S

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Abstract

A technical prototype of a tile hadron calorimeter (HCAL) for the International Linear Collider (ILC) detector is currently developed within the EUDET framework package JRA3. The aim of this prototype is to address the mechanical issues imposed by the requirement of high granularity and compactness. Issues like mechanical feasibility and stability, integration of electronics in the active layers, power pulsing, integration of a monitoring system for each calorimeter cell, have to be addressed.

The prototype is based on scintillating tiles that are read out by novel silicon photo-multipliers (SiPMs). The full prototype will contain about 2500 detector channels (one layer) and takes into account all engineering design aspects that are demanded by the intended operation at the ILC. This report focuses on the status of the three main deliverables of the HCAL work package namely, the availability of the mechanical structure, of the readout electronics for one basic unit and the LED monitoring system to calibrate and monitor the operation of the calorimeter cells inside one basic unit.

*DESY, Hamburg, Germany

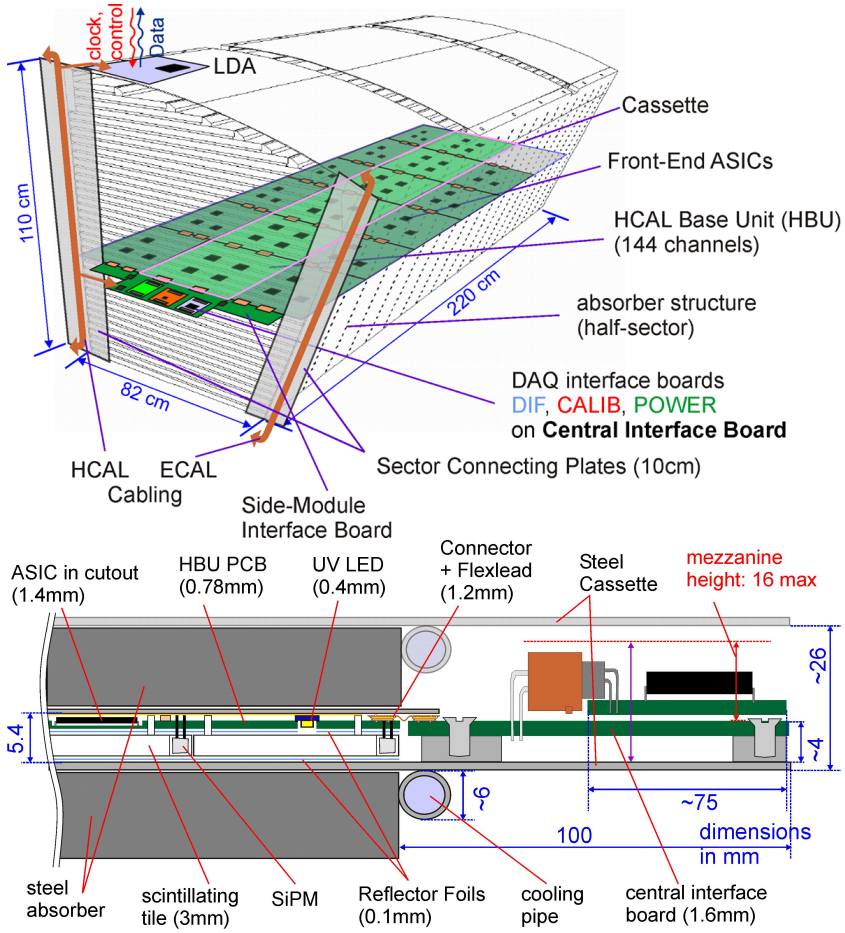

Figure 1: *(top) Electronics integration architecture for the technological AHCAL prototype. (bottom) Possible setup of the proposed HCAL Base Unit (HBU, cross section), showing the interface to the data acquisition modules at the endface. The numbers in brackets show the respective component heights.*

1 The Analogue HCAL technological prototype

In order to validate the concept of a highly granular scintillator based HCAL, it needs to be demonstrated that the high channel density can actually be realized without compromising the performance by too many dead spaces or reduced compactness and hermeticity once readout and calibration electronics or support structures have been accommodated. In this respect the construction of a technological prototype addressing these integration issues is mandatory.

The envisaged detector architecture [1, 2] is sketched in Fig. 1 (top). It is inspired by one variant of the ILD detector concept, but is very similar to those envisaged for SiD or CLIC. The figure shows one sector of a barrel subdivided only once along the beam axis. This layout provides access to electronics and service interfaces once the detector end-cap is opened, but poses tight space constraints to the barrel end-cap transition region.

Figure 2: *The two vertical (left) and the horizontal (right) mechanical structures for the technical HCAL prototype.*

Compared with existing hadron calorimeters, the particle flow HCAL has a rather fine longitudinal sampling, with a correspondingly high pressure on the thickness of the active layer gaps, but also on mechanical tolerances. This, together with the requirement of minimum dead zones represents an engineering challenge which is being addressed now. There are 48 independent read-out layers which must be as thin as possible in order to keep the overall detector volume small, as it has to fit inside the main solenoid of the collider detector and still provide maximum hadronic absorption depth. Each layer has a fine transverse segmentation, again with individual cell read-out, which requires concentrating the data at an early stage in order to keep connectivity issues manageable and reduce dead areas occupied by external electronics components.
The readout ASICs process the signals including digitization and intermediate storage. Thanks to their operation with pulsed power synchronous with the accelerator time structure, no cooling inside the modules is necessary. Only interfaces to DAQ, power supplies and calibration control are placed outside the volume.
For technical manageability reasons, the detector is subdivided into basic units with typically 144 calorimeter cells. In order to reduce the amount of non-absorbing material in the calorimeter, the thickness of the inner detector modules is optimized to only 5.4mm.
We foresee a staged prototype program to validate this concept:

1. A horizontal test structure (Fig. 2 right) to establish the mechanical tolerances and electronics signal integrity over the full area and length of the module. Heat dissipation and installation procedures can also be studied in full scale.

2. A vertical test structure (Fig. 2 left) to establish the mechanical stability under various orientation and stresses as well as multi-layer electronics integration and operation. This can be tested with electron beams and requires instrumentation of a small volume only.

3. The vertical structures can be stacked in a flexible way, according to the needed overall test beam geometry, and their instrumentation completed for hadron shower studies.

The first two steps can be accomplished with about one to two thousand channels, the third will require about 40'000 channels. The multi-layer setup need a compact realization of the interface electronics components.
In addition to the demonstration, that the mechanical and electronics design challenges can be met, there are operational and physics issues to be studied, which could not be tackled with the physics prototype:

- Establish stable operation with auto-triggering and on-detector zero-suppression. This will require continuous monitoring of thresholds and in-time adjustment of bias voltages to compensate for temperature induced variations of the signal.
- The new ASICs incorporate a TDC for a time measurement of calorimeter hits. It must be shown that this system can be timed in and operated stably.
- The usefulness of the timing measurement for neutron hit identification and shower reconstruction can be evaluated.
- The time evolution of hadron showers in simulation models can be confronted with experimental data; for the first time in a spatially resolved way.
- The stainless steel structure allows for operation of the calorimeter in a magnetic field, and to test the predicted influence of the field on hadron shower propagation.

1.1 Mechanical structures

The module consists of stainless steel plates with 16 mm thickness which are supported only by the 5mm thick side panels, without additional spacers. The gaps can be filled completely with active elements.
The mechanical stability of this ambitious design has been extensively studied using finite element methods. Deformations of the individual module as well as the overall barrel structure were validated, taking external support and the suspension of the ECAL into account.
It is straightforward to keep the required tolerances by precisely machining all absorber plate surfaces. However, the cost would be higher by a factor 2 to 3 with respect to the raw material. Since cost optimization is an important ingredient in a "realistic" structure, we aim at producing the structures from raw, commercially available rolled plates. In particular the flatness of the plates, as specified by commercial standards, exceeds the requirements by intolerable amounts. We have prepared devices for measuring deviations and found a cost-effective solution (roller leveling) to achieve the required flatness within a millimeter across the full module.
The horizontal and two vertical test structures are shown in Fig. 2. The first has 4 plates, 2160 mm long, the second is 360 mm deep.

1.2 Readout and calibration electronics

The electronics is subdivided into HCAL Base Units (HBUs) in order to keep the single modules at reasonable sizes concerning production and handling. The HBU with a typical size of 36×36 cm^2 integrates 144 scintillating tiles each with a SiPM readout. The analogue signals of the SiPMs are read out by four front-end ASICs (SPIROC, [3]). The cross section of a HBU is skatched in Fig. 1 (bottom). In order to achieve the aimed detector module thickness of 5.4mm, the HBU interconnection with the necessary high number of signals has to be realized in a very small volume. Two types of flexfleads have been realized for this purpose, one type for the signal-, the other type for the power-supply interconnection. The flexleads contain two 0.8mm thick 80-pin connectors (Kyocera 5801 series), a four-layer, rigid PCB below the connectors and a two-layer flexible part in between. In total, a thickness of 1.15mm above the HBU PCB can be achieved. The flexible part can compensate (distance) misalignments between HBUs of about ± 100 μm. No significant signal distortions for the fast signals or voltage drops of the supply voltages have been observed.
The full depth of a sector is covered by 6 HBUs that are connected together by flexleads. A chain of 6 HBUs forms an electrical layer unit. referred to as slab. At the end of the sector, the electronics of a detector layer are connected to the detector interface module (DIF) and the AHCAL specific modules for calibration (CALIB) and the power-supply module (POWER).
In order to keep the development time for the first prototype modules as short as possible, the first DIF module is realized by a commercial FPGA board. The modules CALIB and POWER are realized as mezzanine modules on top of the DIF, while the interface to the first HBU prototype is realized by the final thin flexlead interconnections via the CALIB module.
Module CALIB with a size of 11×10 cm^2 is based on a ARM7 microcontroller and controls the light-calibration system for the SiPMs on the HBU. Additionally, module CALIB reads out the slow-control monitors for temperature, supply-voltages and -currents. For the calibration task, an analogue bias voltage for the ultraviolet LEDs has to be generated in the range of +5V to +10V with a high stability and accuracy along with a differential fast LED trigger pulse with a width of about 40ns. Module POWER with a size of 12.5×11 cm^2 derives from three input voltages all necessary inner detector supply voltages, including the bias voltages for the SiPMs. It enables the power-cycling of the inner-detector electronics in the ILC bunch train scheme. Module DIF is based in a first extension stage of the prototype on a commercial SPARTAN3-1500 FPGA board. The DIF is the only interface to the global data acquisition and therefore hosts both, the fast interface path to the front-end ASICs, e.g. for the data readout, and all slow-control tasks as for example detector configuration.
The prototype setup shown in Fig. 3 can be used to test all electrical characteristics of a full layer in the horizontal test structure. The electronic commissioning has been completed using LED signals, and the first HBU prototype will be exposed to the DESY test beam by the end of year '09. The DIF board will be read out via USB; the final DAQ chain will be commissioned in 2010, this can start with the FPGA board. There

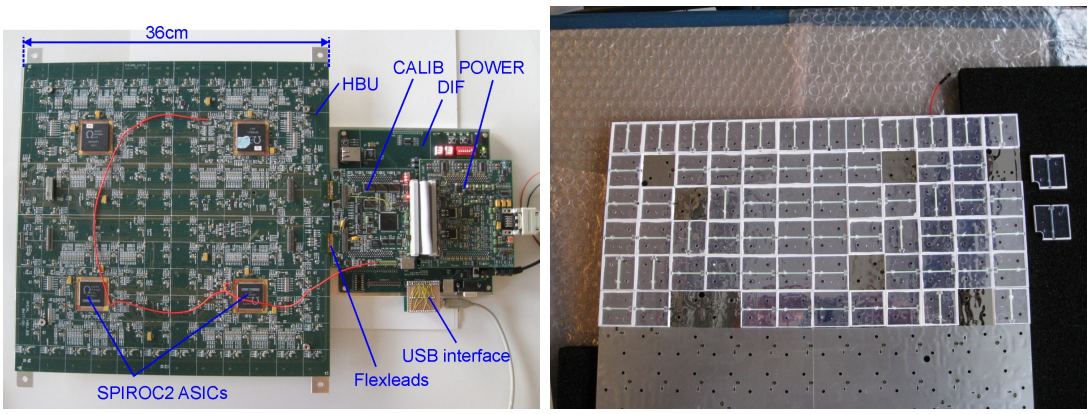

Figure 3: *Test bench set-up with the prototypes of the HBU and interfaces (left), back-side of the HBU with reflector foil and tiles.*

are still two SPIROC chips of the first version of the HBU, which have a thicker package, therefore a re-design of the board layout will be needed for the full layer test.
The AHCAL specific module CALIB is used to control and operate the light calibration system that is based on electrical signal distribution (see section 1.3) as well as a charge-injection system that can be used for calibration and debugging as well. The POWER module provides the supply voltages for the inner-detector electronics as well as for the modules DIF and CALIB, and the SiPM bias voltage. The architecture of the power regulator setup has been defined in detailed measurements of the power-pulsing characteristics. A settling time below 10 μs can be expected.

1.3 LED monitoring system

The LED calibration and monitoring system for the technological HCAL prototype needs to be a scalable system addressing the needs determined during operation and analysis of the HCAL physics prototype [4]. Two approaches are being followed for this system, one based on a central driver and optical signal distribution, one based on electrical signal distribution and an individual LED per tile. The latter is already integrated in the HBU, but not yet fully optimized. The aim is to equalize the light intensity and maximize its dynamic range. Preliminary results [5] using this system show that it is possible to obtain single photo-electron peak spectra from the SiPM on tile, i.e. to extract SiPM gain, using the light injected on the tile by the SMD-type LED integrated on the PCB board (144 LEDs on the board in Fig. 3). First histograms for a single SPIROC2 channel no. 34 at two different, low LED light intensities are shown in Fig. 4. Results obtained with the quasi-resonant LED driver and light distribution via optical fibers are reported in [6]. A six channels UV LED driver, which meets the basic requirements for SiPM calibration, has been realized and tested. The prototype is complemented by the optical system that distributes light from the LED via a single notched fiber to a row of scintillator tiles. The uniformity of the light radiated by the notches is constant within $\pm 20\%$.

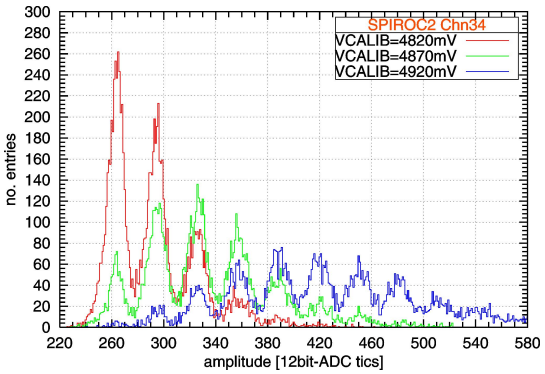

Figure 4: *Histograms of one-channel ASIC input for two LED light intensities and external triggering of the SPIROC2 ASIC. Each histogram contains about 9000 measurement entries.*

The future improvement on the electronic part will concentrate on further miniaturization of circuits and increase of the UV LED pulse width to 5-6 ns. Possibilities to improve the optical system are in the increase of the light output from fiber notches by a factor up to five by better optical coupling of the LED to the fiber, more powerful UV LEDs and better homogeneity of the emitted light from notches.

1.4 Scintillator and photo-sensor development

Following the successful operation of the physics prototype, progress was made by various manufacturers, e.g. in Russia or Japan, to provide sensors with lower dark count rate and / or smaller inter-pixel cross-talk which allow to decrease the noise occupancy above threshold of 10^{-3} in the present prototype by an order of magnitude and thus fulfill the requirements from both physics (for neutron hit identification) and DAQ band width. These groups will be the first to use the EUDET structure for testing their novel sensors in a realistic environment.
For the coupling of sensors to scintillator and PCB different approaches are being followed, based on either wavelength-shifting WLS fiber mediated or direct read-out, which becomes possible with blue-sensitive photo-diodes. In the direct coupling case, the sensor is mounted either in SMD style with its sensitive surface in the PCB plane, or in the same position as for tiles with fibers. In both cases it collects the scintillation light directly from the tile, which has to be shaped in a dedicated way to compensate for the otherwise prohibitive light collection non-uniformities. In this case the positioning of the sensor with respect to the scintillator is somewhat less critical. The different schemes can be accommodates and tested with only modest modifications of the HBU design.

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