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STATUS OF LUMICAL READOUT ELECTRONICS

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Abstract

The design and measurements of the prototypes of readout electronics for the luminosity detector (LumiCal) at the ILC, developed within the EUDET consortium, are presented. The proposed front–end (FE) architecture comprising switched-gain preamplifier, pole-zero cancellation circuit (PZC) and switched-gain shaper is described. The preamplifier works for a wide range of input capacitance values up to 100 pF. The input charge dynamic range is 0.4 fC to 10 pC and covers more than 4 orders of magnitude. The circuit has to be fast with a peaking time of about 70 ns. The prototype ASICs are designed and fabricated in 0.35 μm CMOS technology. The results of measurements on gain, noise, high input rate performance and crosstalk are presented. In parallel to the FE ASIC the digitizer ASIC (ADC) is also developed and the prototypes are fabricated in 0.35 μm CMOS technology. The design of the pipeline 10 bit ADC with 1.5-stage architecture is described. The functional ADC unit works up to about 35 MHz sampling frequency. Wide spectrum of measurements of static (INL, DNL) and dynamic (SNHR, SINAD, THD) parameters are presented.

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1 Introduction

In the future International Linear Collider (ILC) the luminosity measurement will be done by LumiCal detector which constitutes an important part of the Forward Calorimetry region [1]. The development of the infrastructure for a prototype test of the LumiCal detector is supported by the European Community under the EUDET project [2].
The LumiCal is built as Si/W sandwich calorimeter composed of interleaved layers of passive absorber (W) and active sensor (Si) [3]. It is assumed here that the active part of LumiCal comprises 30 layers of 300 μm thick DC-coupled silicon sensors whereas each layer is divided into 24 azimuthal sectors. Each sector, with the inner radius of 8 cm and the outer of 35 cm, is segmented into 96 radial strips with a constant pitch. In total the system requires about 140,000 readout channels.
The design of the LumiCal front–end electronics depends on several assumptions and requirements concerning detector architecture [3]. The front–end should work in two modes: the physics mode and the calibration mode. In the physics mode the detector should be sensitive to electromagnetic showers resulting in high energy deposition and the front–end should process signals up to 10 pC or even more per channel. In the calibration mode it should detect signals from relativistic muons, i.e. should be able to register the minimum ionizing particles (MIPs). It means that the signals as small as 2 fC (corresponding to low end of the Landau distribution for MIPs in 300 μm thick silicon) should be detected. Proposed sensor geometry results in very wide range 10 pF – 100 pF of strip capacitance connected to a single front–end channel. Because of very high expected strip occupancy, the front–end should be fast enough to resolve signals from subsequent beam bunches which are separated in time by about 350 ns. The simulations of LumiCal indicate that the reconstruction procedure needs about 10 bit precision on the measurement of the deposited energy. Severe requirements set on readout electronics power dissipation may be strongly relaxed if switching of the power between bunch trains is implemented. This is feasible since in the ILC experiment after each 1 ms bunch train there will be about 200 ms pause [4].
From the above specifications the general concept of the full readout chain is outlined as shown in fig. 1. The main blocks of the signal chain are: front-end electronics, A/D conversion plus zero suppression and data concentrator with optical driver.
In the following the design and the measurements of prototype front–end and digitizer (ADC) ASICs are presented.

2 Front–end electronics design

To fulfill the discussed requirements the front–end architecture [5, 6] comprising a charge sensitive amplifier, a pole–zero cancellation circuit (PZC) and a shaper is chosen, as shown in fig. 2. In order to cope with large charges in the physics mode and the small ones in the calibration mode a variable gain in both the charge amplifier and the shaper is applied. The "mode" switch in fig. 2 changes effective values of the feedback circuit components R_f, C_f, R_i, C_i and so changes the transimpedance gain of the front–end.

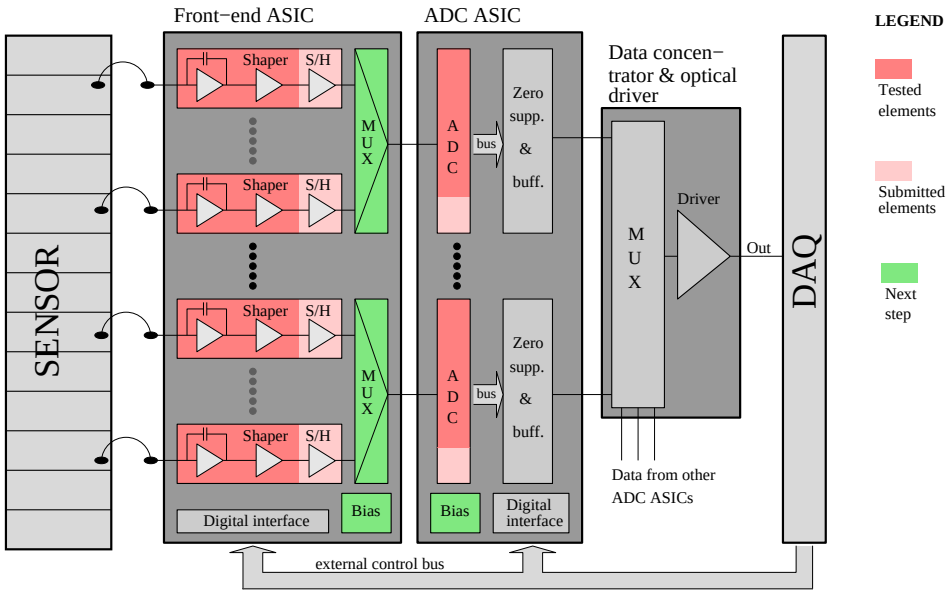

Figure 1: Block diagram of the LumiCal full readout chain

The low gain (large C_f) is used for the physics mode when the front–end processes

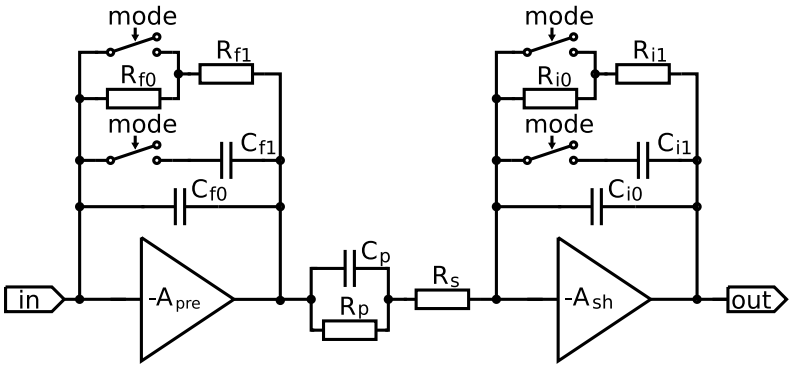

Figure 2: Block diagram of the single front–end channel

signals with large charge depositions in the sensor, while the high gain (small C_f) is used in the calibration mode when a MIP sensitivity is needed. In the following the terms physics mode and low gain mode are used interchangeably. The same concerns the terms calibration mode and high gain mode. Assuming high enough open loop gain of the preamplifier (A_{pre}) and the shaper amplifier (A_{sh}), the transfer function of this circuit is given as:

$$\frac{U_{out}(s)}{I_{in}(s)} = \frac{1}{C_f C_i R_s} \cdot \frac{s + 1/C_p R_p}{s + 1/C_f R_f} \cdot \frac{1}{(s + 1/C_i R_i)(s + 1/C_p(R_p||R_s))} \tag{1}$$

Setting properly the PZC parameters ($C_f R_f = C_p R_p$) and equalizing shaping time constants ($C_i R_i = C_p(R_p||R_s)$) one obtains the first order shaping, equivalent to a CR–

RC filter, with a peaking time $T_{peak} = C_i R_i$. A simple first order shaping is chosen as a tradeoff between the noise and the power dissipation. Regarding the noise a main requirement is to obtain in calibration mode the signal to noise ratio (S/N) of about 10 for the largest sensor capacitances. This requirement can be fulfilled with a first order shaping. Increasing the shaping order would still improve the S/N in the calibration mode but it would increase the power dissipation and deteriorate the S/N in the physics mode configuration. In the physics mode the signal arrives to the shaper without any amplification and so the main noise contribution comes from the shaper.
Both of the amplifying stages (A_{pre}, A_{sh}) are designed as the folded cascodes [7] with active loads, followed by the source followers. The input transistor of the preamplifier stage is biased with a current of about 2.2 mA. Because of a wide input charge dynamic range a large total feedback capacitance ($C_{f0} + C_{f1}$) of about 10 pF is implemented in the preamplifier. A more detailed schematic of the preamplifier is shown in fig. 3. In order to maximize the gain–bandwidth product (GBP) of preamplifier the active load is designed as a cascode current source. In the prototype ASIC 8 front–end channels are

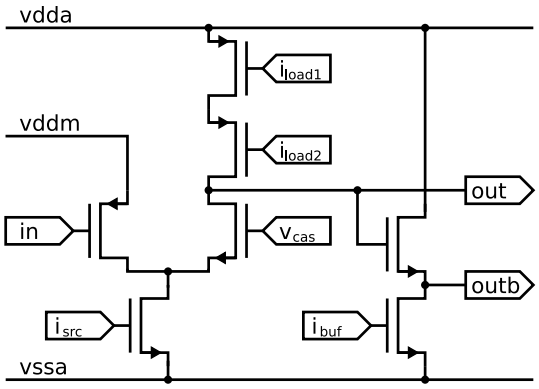

Figure 3: Schematic diagram of the preamplifier

implemented. Four channels are designed with passive feedback and PZC resistances R_f, R_p while the other four channels use MOS transistors in a triode region to this aim [8]. This allows us to compare overall performances of the two feedback schemes. The maximum value of passive resistance ($R_{f0} + R_{f1}$ in the calibration mode) is 1.5 MΩ, while the resistance of MOS transistors is externally controlled and may reach much higher values. In the motivation of active feedback implementation not less important than the high resistance is the small parasitic capacitance and the possibility to compare the matching of the PZC network for active and passive solution. The value of calibration mode feedback capacitance (C_{f0}) of 0.5 pF is chosen for the channels with the passive resistors and 0.23 pF for the channels with the MOS resistors. The test capacitance (not shown in fig. 2) of 0.5 pF is added at the input of each channel and the test inputs are grouped separately for odd and even channels. This allows us to test the ASIC without a sensor. The area occupied by single channel is 630μm × 100μm. Prototype ASICs have been fabricated in 0.35 μm, four–metal, two–poly CMOS technology.

3 Front–end electronics measurements

Three prototype ASICs have been bonded on dedicated PCB boards to test the front–end functionality and to measure their electrical parameters. The photograph of prototype ASIC glued and bonded on the PCB is shown fig. 4. The power consumption of about

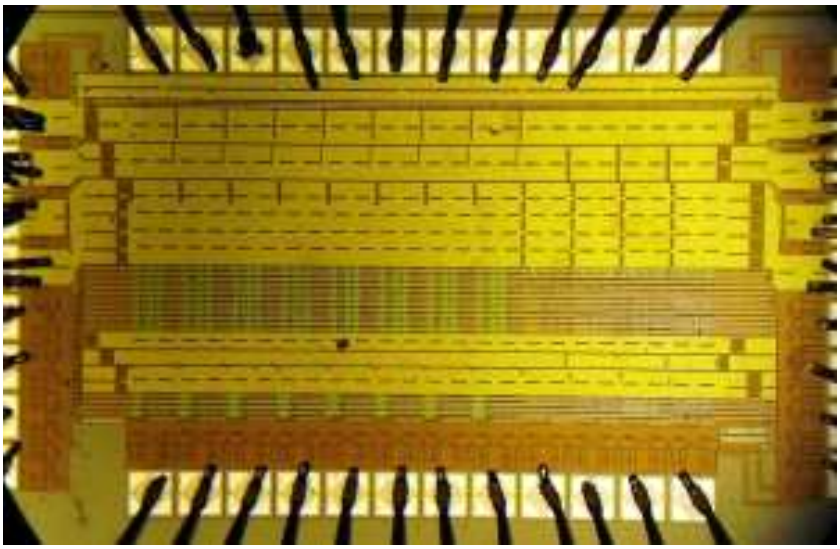

Figure 4: Photograph of glued and bonded FE prototype. First 4 channels from the left have passive feedback and next 4 channels have active feedback

8.9 mW/channel is measured what confirms well the simulations. After checking the basic functionality the systematic measurements of the essential parameters, gain, noise, high count rate performance and crosstalk, have been performed. The results of these measurements are discussed in the following sections.

3.1 Pulse shapes

Fig. 5 shows the response of the front–end channel to charge injected through the input test capacitance for different values of input capacitance (C_{det}) within the interesting range. The sensor capacitance is simulated with an external capacitor.
For the physics mode the results obtained for active (MOS) and passive (R_f) feedback are exactly the same and so only the active feedback curves are shown in the plot. It is seen that both, the amplitude and the peaking time (∼70 ns), are not sensitive to the value of the input capacitance in this case. In the calibration mode the amplitude and the peaking time slightly depend on the input capacitance (C_{det}). This dependence is more pronounced for the active feedback case. This can be explained keeping in mind that in the calibration mode the preamplifier's feedback capacitance C_f is small (∼230 fF for MOS, ∼500 fF for R_f) and so the ratio of C_{det} to the effective input capacitance $C_{eff} \simeq A_{pre} \cdot C_{f0}$ is not negligible for the preamplifier gain of about 1000 and the input capacitance reaching 100 pF. In such a case a fraction of the input charge is lost on the

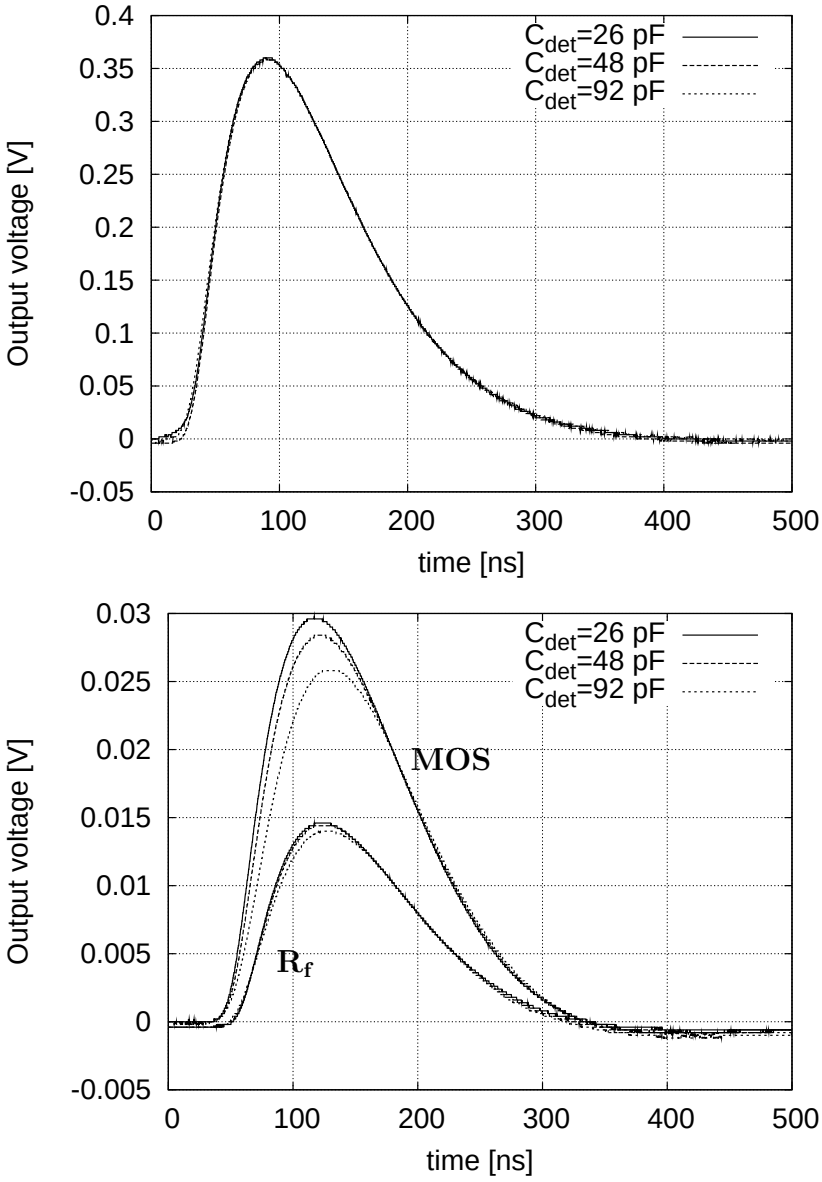

Figure 5: Output pulses for MOS resistor front–end channels in physics mode (upper) and for MOS and R_f resistor in calibration mode (lower), as a function of input capacitance. In calibration mode $Q_{in} = 10\ fC$, while in physics mode $Q_{in} = 3.3\ pC$

sensor capacitance and the preamplifier can not be considered as purely charge sensitive since C_{det} affects its transfer function. The effect is more pronounced for the channels with active MOS feedback for which C_f is smaller. In the physics mode, where the feedback capacitance is large (∼10 pF) the preamplifier can be considered as an ideal charge sensitive one and so no amplitude sensitivity on the input capacitance is seen. The described measurements are in good agreement with Hspice simulations performed for both types of feedback resistors and both gain modes.

3.2 Gain measurements

Systematic measurements of charge gain covering full input signal dynamic range have been performed for a number of channels. The results are shown in fig. 6 for the physics

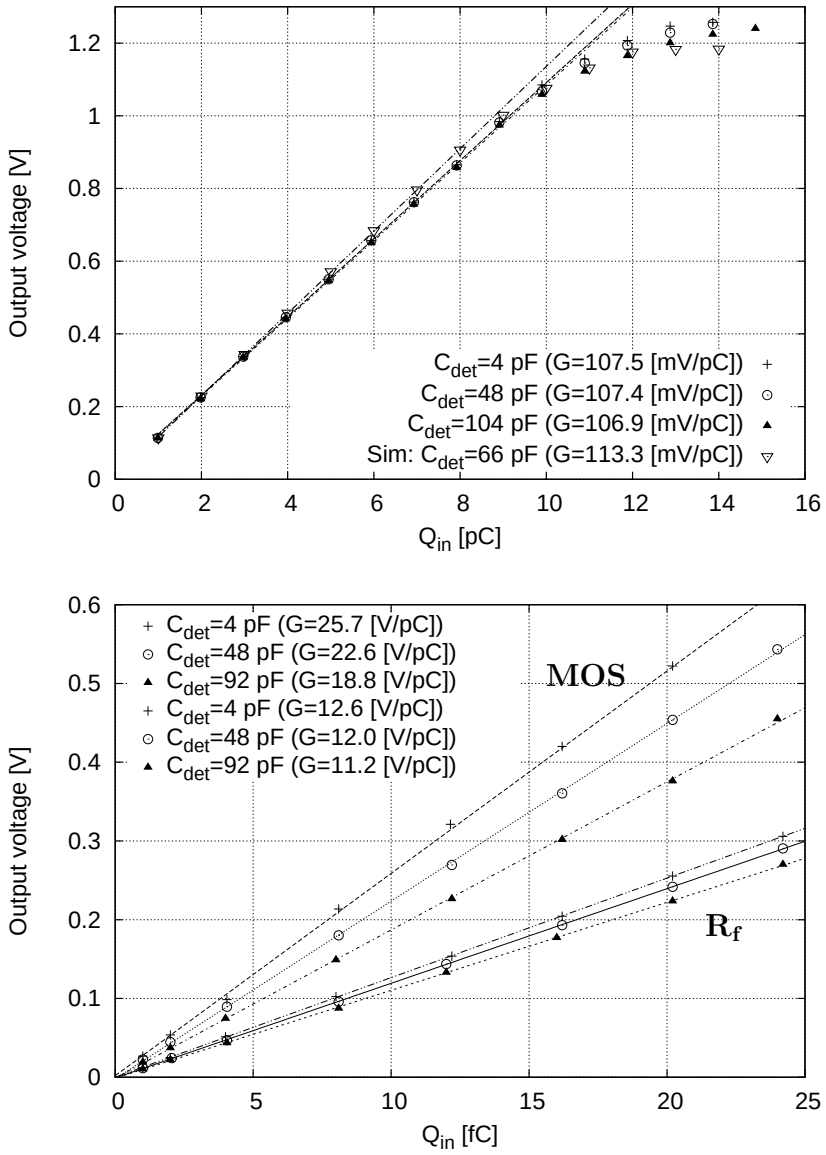

Figure 6: Gain measured in physics mode for channels with R_f feedback (upper), in calibration mode (lower) for channels with MOS and passive R_f feedback

mode (upper plot) and for the calibration mode (lower plot). In the physics mode the measurements are performed injecting the charge through an external capacitance. Injecting input charges through the internal test capacitors of 0.5 pF would require the input voltage step up to 30 V, which would damage the input transistor. The measurements are done for charge injections up to 15 pC. Such input range is chosen

because the experimental requirement is to extend the input charge range as far as possible, while a good linearity is needed only in the region for which significant channel occupancy is expected (∼6 pC). Fig. 6 (upper plot) shows only the results obtained for the channels with the passive feedback. The same results are obtained for the active feedback channels. It is seen that the circuit response is linear with input charge and saturates for the highest charges injected. The measurement of linearity have been performed in the most interesting range for physics i.e. up to 6 pC. In this range the observed integral nonlinearity is below 2%. Such deviations are measured using as ADC the general purpose scope (TDS3000) and may be overestimated. To make the linearity measurements more reliable we kept the scope vertical scale unchanged during the scan over the injected charge. This caused the relative error for the smaller amplitudes to be significantly higher than for the larger ones. This trend is also observed in the measured deviations for all (low and high gain, passive and active feedback) performed scans. Unfortunately we have not had more precise ADC which would be able to cope with signals of T_{peak} below 100 ns. As expected the circuit response is not sensitive to the input capacitance value. The performed measurements are in good agreement with the simulation results which are shown in the same plot.
For the calibration mode the measurements performed for both feedback types are shown in fig. 6 (lower plot). Only the most interesting input charge range (up to several MIPs) is shown. For all input capacitances both channel types show linearity similar as in physics mode. In both cases the gain slightly depends on the input capacitance value, decreasing with increasing C_{det}. Such behavior is expected from theory and simulations. For the active feedback the effect is more pronounced since in this case the channel feedback capacitance C_f is about half of the value used for the channels with the passive feedback.

3.3 Noise measurements

The rms values of the output noise have been measured using the HP3400 true rms meter. The equivalent noise charge (ENC) as a function of input capacitance for both front–end types is shown in fig. 7. Results obtained for the physics and calibration modes are shown on the same plots. Since the HP3400 bandwidth is only up to 10 MHz the numbers may by underestimated by about 20%. The ENC vs C_{det} behavior and the measured values are generally in agreement with simulations. In particular, in the calibration mode the signal to noise ratio of 10 is maintained for input capacitances up to 100 pF. For a few points additional noise measurements have been performed by measuring the output noise spectra using HP4195A spectrum analyzer and then integrating it numerically to get the rms noise values. The results of such measurements for the channel with the passive feedback are added in fig. 7 (upper plot). They agree within their uncertainties with the HP3400 rms measurements. For a complete noise picture the measurements with particles impinging a sensor are needed and will be performed as soon as the LumiCal sensors and fanouts are fabricated.

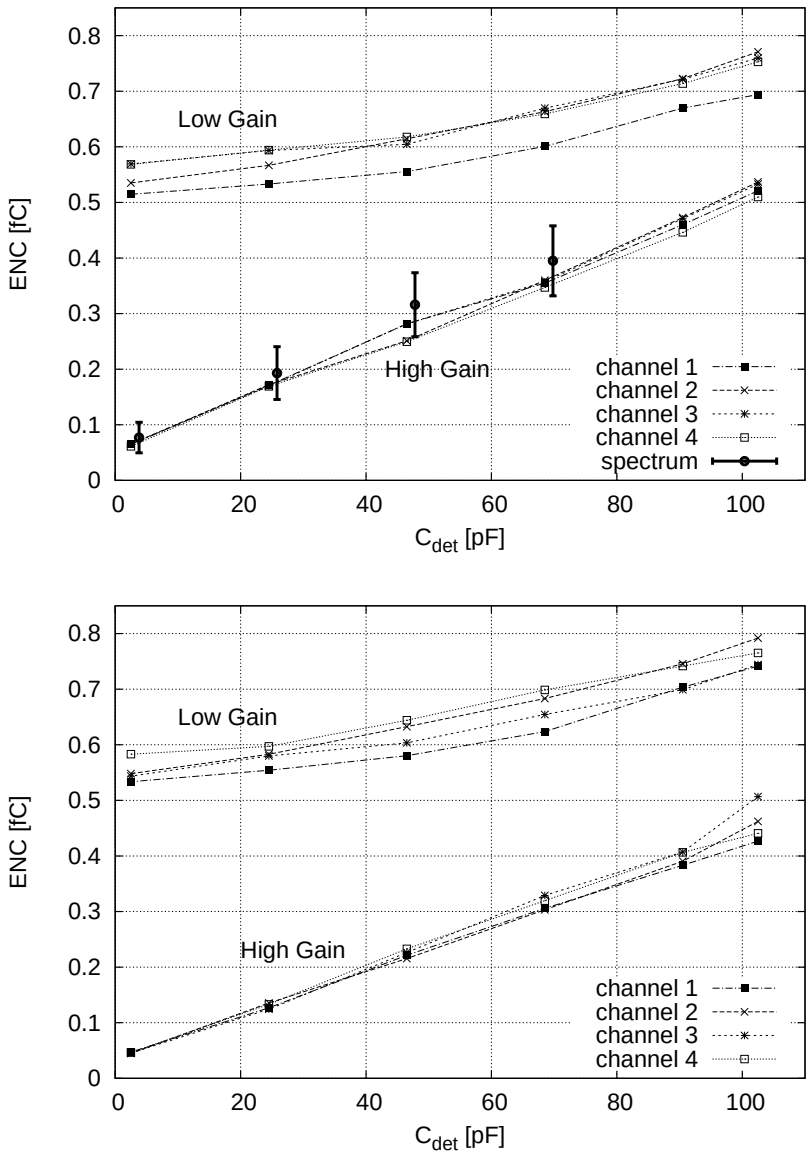

Figure 7: Noise ENC measurements obtained with true rms meter for the front–end with passive feedback (upper) and active feedback (lower)

3.4 High count rate performance

In order to test the effectiveness of the PZC circuit the front–end response has been measured as a function of the rate of input pulses. To avoid input charges of both polarities when using a square–wave test signal, the staircase test waveforms are synthesized using the Tektronix AWG2021 waveform generator. The effect of pulse frequency is estimated comparing the output amplitude obtained for the given input frequency to the amplitude obtained for the reference (low) input frequency. The comparison is done measuring the amplitudes of the signals at the ends of pulse trains (usually ∼20 pulses

in the train).

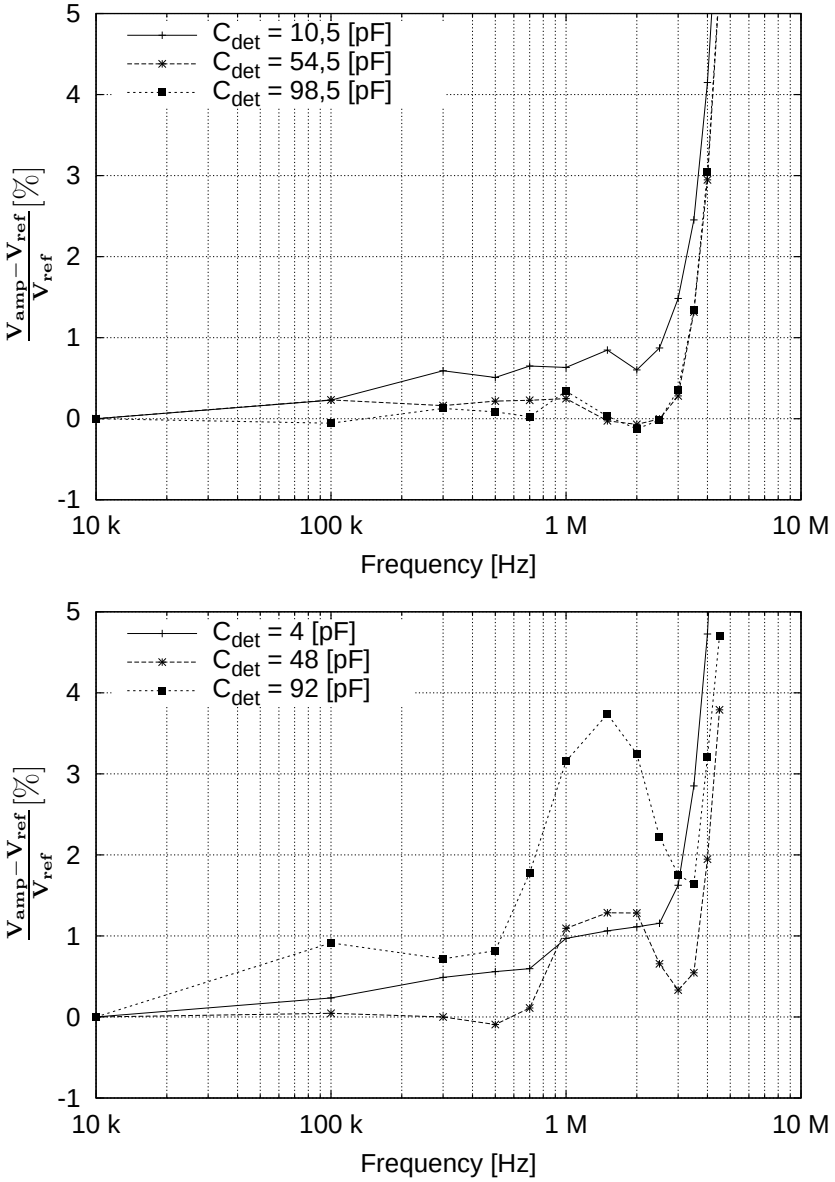

Figure 8: Amplitude change for R_f resistor front–end channels in physics mode (upper) and in calibration mode (lower)

Fig. 8 shows the relative change of the amplitude as a function of pulse rate for the passive feedback channels. The results are shown for the physics mode (upper plot) and the calibration mode (lower plot). One can see that for the physics mode the change in amplitude reaches 2% for input rates of about 3 MHz and is almost not sensitive to input capacitance. Both, the amplitude change and the lack of sensitivity to C_{det} are in good agreement with the simulations results. In the physics mode (high C_f) the PZC operation should depend only on the $C_f R_f$ and $C_p R_p$ matching which seems to be very

good. On the opposite, in the calibration mode, as it is already seen in the simulations, C_{det} affects the preamplifier operation and good PZC cancellation is obtained only for a given input capacitance. This is confirmed by measurements shown in in fig. 8 where large spread of curves obtained for different C_{det} is observed. Nevertheless, also in the calibration mode the PZC works well up to sufficiently high rates. The change in the amplitudes is below 4% in the worst case (highest input capacitance). Similar results are obtained for the front–end with the active feedback channels although the absolute effect of high pulse rate is slightly higher.

3.5 Crosstalk

To estimate the crosstalk between the channels a dedicated setup with a simple general purpose PIN diode used as sensor and a laser has been prepared. Using physical signals generated by light pulses in the diode allows us to exclude the possibility of additional crosstalk through the parasitic capacitances on the PCB. Such crosstalk could appear in case of electrical charge injection through a test capacitance. In the calibration mode relatively low crosstalk is observed which is below 0.1% for the front–end with the active feedback and below 0.3% for the passive feedback. A slightly higher level in the latter case may be well explained by the large parasitic capacitance of the feedback resistance (1.5 MΩ) which occupies much larger area than the MOS transistor in the front–end with the active feedback. Significantly higher crosstalk is observed for both front–end types in the physics mode. In case of the active feedback almost 1% crosstalk is measured while for the passive feedback it is about 1.5%. It seems that such a large crosstalk can be explained by the influence of parasitic capacitance associated with the very large feedback capacitor of 10 pF. This effect will be addressed in the layout of the next prototype.

4 ADC design

One of the most efficient architecture assuring a good compromise between the speed, area and power consumption is a pipeline ADC, and this architecture was chosen for the LumiCal data conversion. The pipeline ADC is built of several serially connected stages as shown in fig. 9. In the proposed solution a 1.5-bit stage architecture is chosen because of its simplicity and immunity to the offsets in the comparator and amplifier circuits. Since single stage generates only three different values coded on 2 bits it is called 1.5-bit stage. Each stage from fig. 9 generates 2 bits which are sent to digital correction block. In the correction block 18 output bits from 9 stages are combined together resulting in 10 bits of ADC output.
The block diagram of a single stage is shown in fig. 10. Each 1.5-bit stage consist of two comparators, two pairs of capacitors C_s and C_f, an operational transconductance amplifier, several switches and small digital logic circuit. To improve the ADC immunity to digital crosstalks and other disturbances a fully differential architecture is used. The operation of the stage is performed in two phases. In phase φ_1 (see fig. 10) capacitors C_s

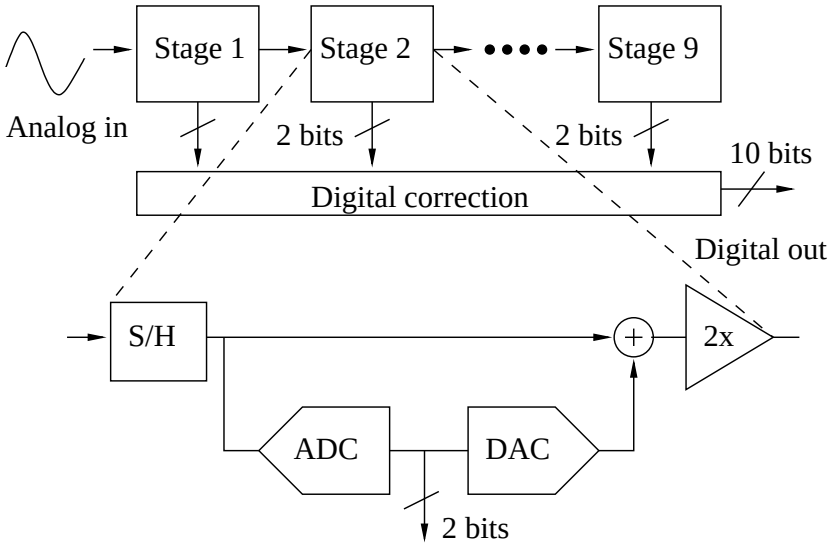

Figure 9: Pipeline ADC architecture

and C_f connected to ground through S_1(in reality to common voltage, ground is used in description only for simplicity) are charged to voltages $V_{i\pm}$. In phase φ_2 the switches S_2 and S_3 change positions and S_1 is open. The C_f are now in the amplifier feedback while the C_s are connected to DAC reference voltages ($\pm V_{ref}$ or 0 depending on comparators decision). Such a connection results, if $C_f = C_s$ which is a common choice, in a gain of two in the 1.5-bit stage transfer function.

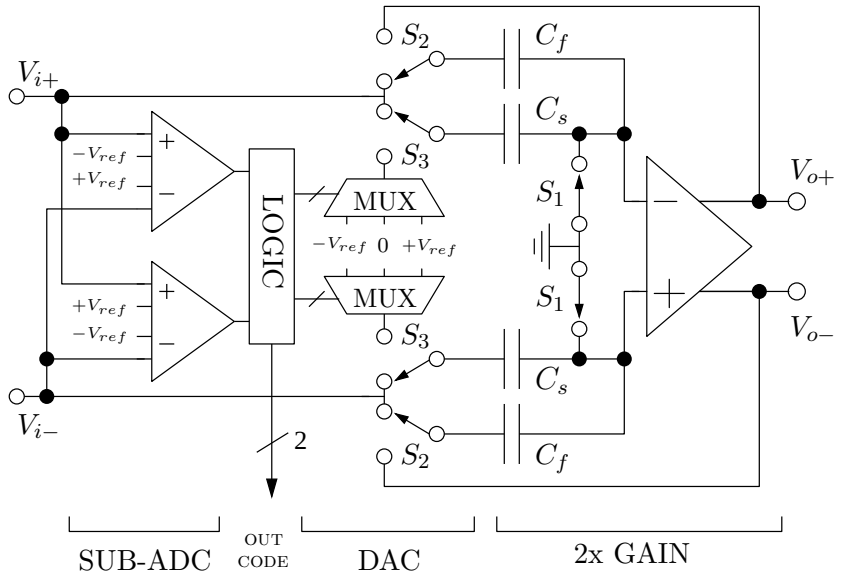

Figure 10: Simplified schematic of a 1.5-bit stage. Switches set to φ_1 phase

In the present design the functional ADC unit i.e. the eight 1.5-bit stages is implemented. In last 9th stage the amplifier multiplying by 2 (MDAC) and other components are

not necessary but only sub-ADC consisting of comparators is needed. To simplify the layout design this sub-ADC is not yet implemented at present development stage. An important component of typical ADC, i.e. the input sample and hold (S/H) circuit, is also not implemented because it is planned to be the last stage of a front-end channel. For this prototype all reference voltages are assumed to be applied externally. The eight designed pipeline stages are almost identical with the only difference in the values of sampling C_s and feedback C_f capacitances and the current drawn by the amplifiers in the following stages. For this reason, regarding analog part, only the description of single stage components, i.e. of the amplifier and the comparator is presented in this work.
The digital logic block contains several gates to generate an output code and to control transistor switches in MUX block. These two blocks are not discussed here because of their simplicity.
Below we discuss the design and the measurement of the first ADC prototype. We would like to add here that with the experience gained with the discussed prototype, we have already completed the design of full 10 bit ADC version. This new ADC design has been already fabricated and will be tested soon.

4.1 Fully differential amplifier

A critical block of pipeline ADC is the fully differential amplifier. A telescopic cascode amplifier configuration is used here since compared to commonly used configurations i.e. folded cascode or two stage amplifier it represents the most efficient solution with respect to speed vs power. On the other hand, the considered technology with 3.3 V supply voltage leaves enough space for the signal dynamic range which would be the weak point of telescopic configuration at lower supply voltage. In order to obtain high enough gain in a single stage amplifier a gain-boosting scheme is implemented in both upper and lower cascode branches [13, 14].
The block diagram of the implemented fully differential amplifier is shown in fig. 11. In fact the simulated architecture achieves above 100 dB open loop gain, which leaves a large margin for the requested 10 bit resolution ADC. Both boosting amplifiers are fully differential single stage amplifiers. The lower branch amplifier (A1) uses the telescopic cascode configuration similar to the main amplifier while the upper branch amplifier (A2) uses the folded cascode configuration with the NMOS input transistors. The main amplifier as well as both gain-boosting amplifiers use continuous common mode feedback (CMFB) scheme with MOS transistors working in the triode region connected between the ground and the source of transistor M9. The amplifier power consumption is scaled in the subsequent pairs of ADC stages decreasing the bias current by a factor of about 0.7.

4.2 Dynamic latch comparator

Since the 1.5-bit stage architecture leaves very relaxed requirements on the comparators ($\sim$100 mV threshold precision) a simple dynamic latch architecture can be used. For this work the circuit shown in fig. 12 is chosen [15].

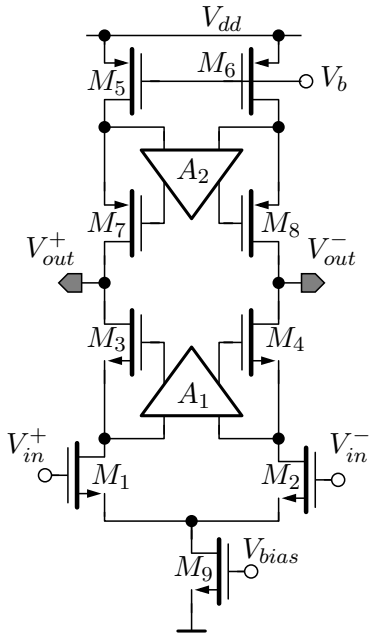

Figure 11: Block diagram of fully differential amplifier with boosted gain

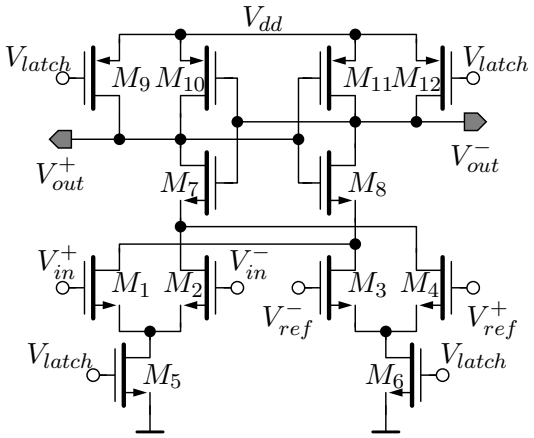

Figure 12: Schematic diagram of the latched comparator

The choice is motivated by a particularly good insensitivity to transistor mismatch and input signal common mode value. A small inconvenience is the fact that the threshold in this implementation is not given by a simple ratio of transistor dimensions but is given by a second order equation. As shown by the authors [15], assuming transistor widths $W_1 = W_2, W_3 = W_4$, bias currents $I_{D5} = xI_{D6}$ and requesting the threshold point $V_{in} = yV_{ref}$, the threshold condition is governed by the equation:

$$2xy^2 I_{D6}\frac{W_1}{L} - \mu C_{ox} y^4 V_{ref}^2 \left(\frac{W_1}{L}\right)^2 = 2I_{D6}\frac{W_3}{L} - \mu C_{ox} V_{ref}^2 \left(\frac{W_3}{L}\right)^2. \qquad (2)$$

Using above equation one can get the transistors dimensions for the assumed x, y values.

5 ADC Measurements

The ADC prototypes are fabricated in a 0.35μm, four-metal two-poly CMOS technology. The dimensions of the ASIC are 1.1×1.2 mm. The photograph of prototype glued and bonded on the PCB is shown fig. 13. Eight identical MDAC blocks are placed around the chip. Biasing and clocks generation blocks are located in the center of the chip. The power consumption of the whole analog part is measured to 48 mW independently

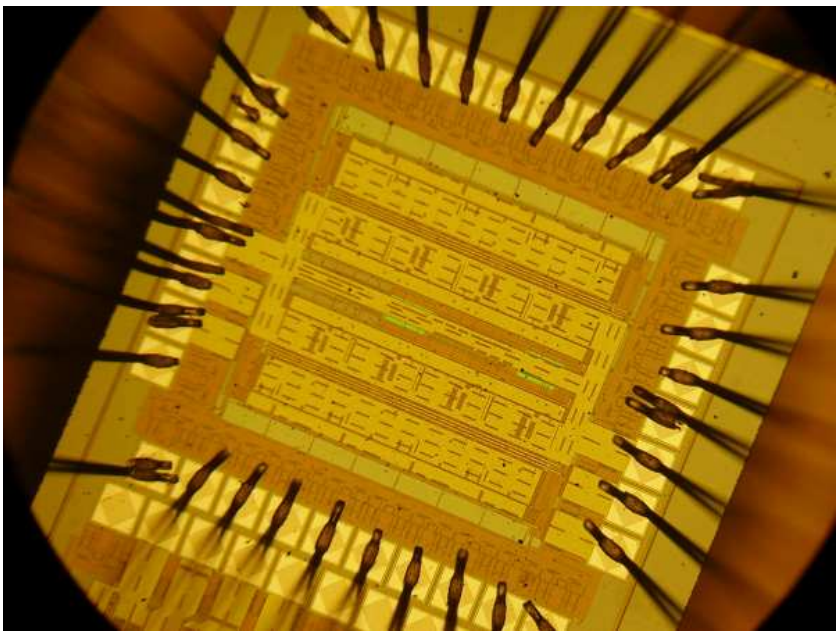

Figure 13: Photograph of glued and bonded ADC prototype

of sampling frequency. In first tests, the basic functionality is studied with DC input signal. Then the essential static (INL, DNL, missing codes) and dynamic (SFDR, SNHR, SINAD, THD) parameters are measured. Dedicated measurements are performed to get better insight into the operation of the key blocks of a single pipeline stage i.e. the MDAC and the sub-ADC.

5.1 Test Setup

The block diagram of the complete test system is shown in fig. 14. In order to perform the tests with single-ended input signals a dedicated circuit based on fast differential amplifier converting single ended signals to differential is added. As a source of input signal a 12 bit arbitrary waveform generator (Tektronix AWG 2021) is used. For measurements with static signals the AWG is used as a precise voltage source while for dynamic measurements it generated step signals as shown in fig. 15. The step signals are used because the S/H circuit is not implemented at the ADC input. The clock signal is also generated by the AWG. All reference voltages are applied with HP4145B precise

power supply which is controlled through GPIB interface. Such configuration allowed us to determine the effect of biasing conditions on overall circuit performance.

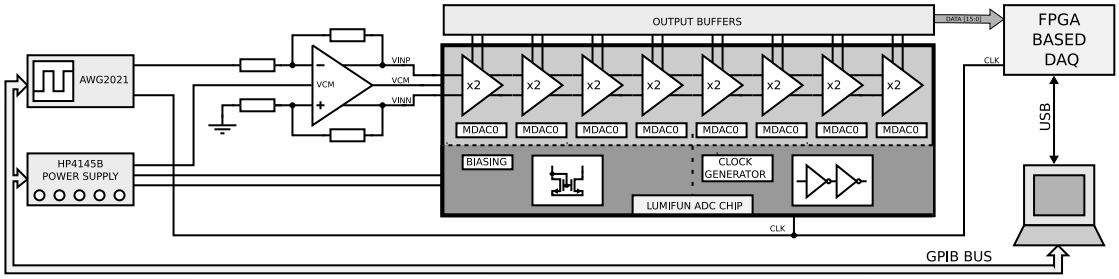

Figure 14: Block diagram of the complete test system

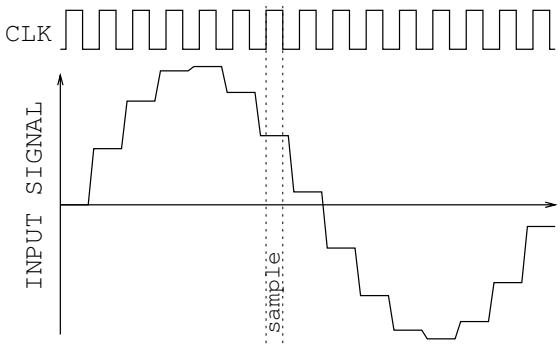

Figure 15: Input signals generation and clocking

Because digital correction algorithm is not yet implemented in the ASIC all 16 bits had to be read out (instead of 9 in case if correction is implemented). Practically the readout is done by FPGA based data acquisition system connected to a PC via USB link. Digital correction is performed by software during data analysis.

5.2 INL and DNL measurements

The Integral Nonlinearity (INL) and the Differential Nonlinearity (DNL) results showed in fig. 16 are measured statically with the ADC sampling frequency of 10 MHz. These parameters are obtained with histogramming method. The integral nonlinearity is measured to be within ± 3 LSB. The Effective Number of Bits (ENOB) of 6.65 is calculated from the measured INL curve.
Differential nonlinearity stays mostly within ± 0.5 LSB, but there are some codes with larger DNL. Six of the codes with DNL less than -0.9 are identified as missing codes [16]. These 6 missing codes (about 1% of the total) and quite high INL are the main issues to resolve in the present ADC version.

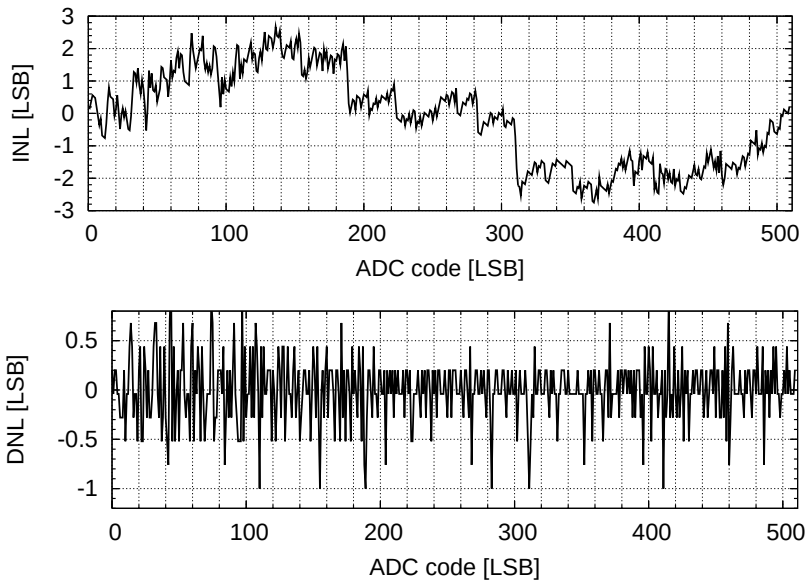

Figure 16: Static measurements of INL and DNL errors

5.3 Dynamic FFT measurements

To estimate dynamic circuit performance measurements with pure sinusoidal wave input are performed [16]. Fast Fourier Transformation (FFT) is used to calculate output signal spectrum. Having in mind that ADC output signal is superposition of input signal, distortions and noise one can use few metrics to determine ADC performance. To estimate pure noise level in a circuit one has to compare the ratio of FFT signal amplitude at the input signal frequency f_0 to the integrated FFT spectrum excluding harmonic frequencies ($2f_0$, $3f_0$, $4f_0$, ...). Such metrics is called Signal to Non Harmonic Ratio (SNHR). The ratio of a signal amplitude to all harmonics is called the Total Harmonic Distortion (THD). The ratio of the FFT signal amplitude at the input frequency to the amplitude of the largest harmonic or spurious spectral component observed over the whole Nyquist band is called the Spurious Free Dynamic Range (SFDR). To determine the overall ADC performance the Signal to Noise and Distortion Ratio (SINAD) is used. Its value is calculated as a ratio of the signal at the input signal frequency to the integral over all frequencies (excluding input signal frequency).
Measured spectrum for 3.4 MHz full scale (0 dB) input signal sampled at 35 MHz is shown in fig. 17. The SINAD of 40.4 dB is obtained. It is dominated by the harmonic distortions (THD) which is equal to 40.9 dB. It is too low for 8 bit ADC (in the ideal 8 bit case it should be 49.9 dB). Detailed studies showed that such behavior is due to MDAC gain mismatch (MDAC gain is lower than 2). It is verified with simulations that the gain mismatch is not caused by too low gain of the differential amplifier but is connected to not precise enough timing of MDAC switches. It will be improved in the next version. The SNHR of 49.1 dB is obtained and it's quite promising because it shows that the pure noise level is equivalent to the ideal 8 bit ADC. The effective

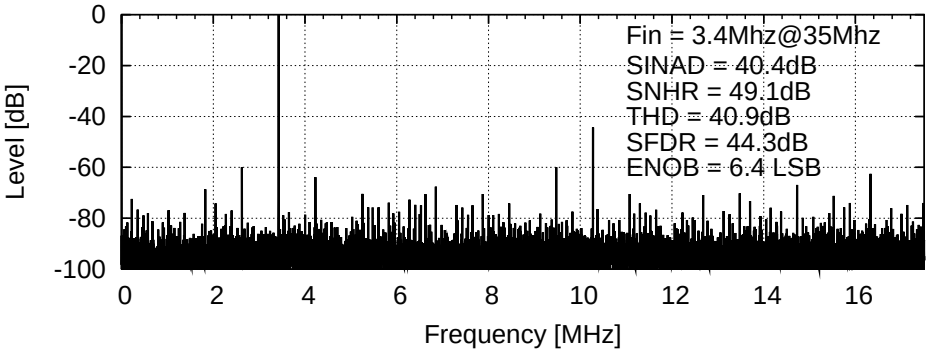

Figure 17: Example of FFT measurement with f_{in}=3.4 MHz and f_{clk}=35 Mhz

number of bits (ENOB) calculated from dynamic measurements equals 6.4 which is in good agreement with the results obtained from static measurements.
The dependence of all discussed above metrics on ADC sampling frequency is also investigated. The results of this measurements are shown in fig. 18. One may conclude that

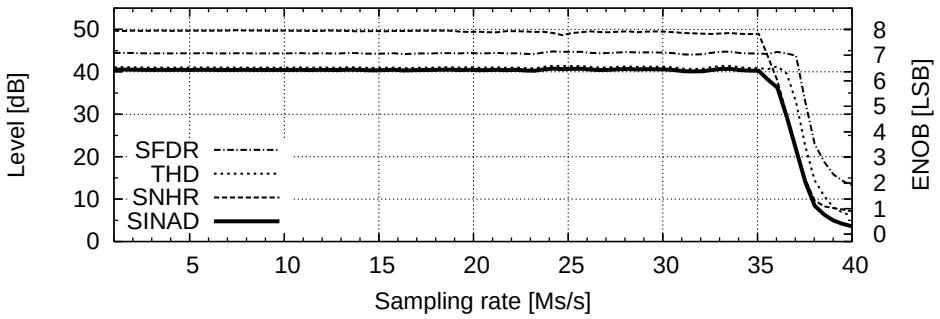

Figure 18: ADC performance as a function of sampling rate

the ADC works well in a wide frequency range up to 36 Mhz. Above this frequency all the metrics fall due to bandwidth limit of MDAC amplifier. Also the effect of the input signal frequency is investigated and the measurements showed that it does not affect the ADC performance over the whole Nyquist band.

6 Conclusion

The prototypes of the readout electronics for the LumiCal detector have been designed and fabricated. The performed tests confirm expected functionality.
The quantitative measurements of the front–end ASIC concerning the peaking time, the gain, the noise and the high count rate performance are in agreement with the Hspice simulations. The two types of the front–end with different feedback resistors show similar good performance with only small differences. Therefore it is not obvious which solution is better, although smaller area and crosstalk slightly favor the active MOS one.

Concerning the digitizer, the key static (INL, DNL) and dynamic (SFDR, SNHR, THD, SINAD) parameters are measured and a proper functionality for sampling frequencies up to 36 MHz is verified. The measured noise (SNHR) of about 50 dB corresponds to expected value for 8 stages. Some imperfections in the linearity (THD, INL, DNL) are found and understood. The new complete version of ADC, with the improved linearity, has been designed and fabricated.
Summarizing, the FE ASIC is tested and ready to be integrated into the detector system. The new complete digitizer ASICs will be tested soon. In the next development step, as soon as the LumiCal sensors and fanouts are fabricated, the performance of the complete detector chain will be studied.

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