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Achievement of milestone: prototyping the data acquistion system for calorimeters

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Abstract

This memo briefly describes the status of work on the data acquisition (DAQ) system for the calorimeters and in particular presents a DAQ system prototype, which is one of the milestones of the project and the first of this task.

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1 Introduction

As part of the EUDET effort to produce technical calorimeter prototypes, UK groups will contribute the data acquisition (DAQ) system. This is based around the generic R&D ongoing in the UK which is considering providing DAQ solutions using commercial components instead of more traditional bespoke hardware. This "backplaneless" system should then be scalable and easily upgradeable and applicable to several sub-detector systems.
A schematic of the DAQ system is shown in Fig. 1, which shows the detection slabs with ASICs communicating with the DAQ, which constitutes the rest of the diagram. The front-end electronics consist of two components: the detector interface board (DIF); and the link/data aggregator (LDA). The DIF is detector specific, sends and receives information to the ASICs and LDA and also has controls, e.g. power. The LDA (and indeed everything further back) is then generic and can be used for all flavours of calorimeter and one LDA will be connected to multiple DIFs. The LDA is then connected to the off-detector receiver (ODR) which is a PC containing PCI cards. Communication between all the components is bi-directional as clock, control and configuration data need to be sent up as well as data coming off the detector.

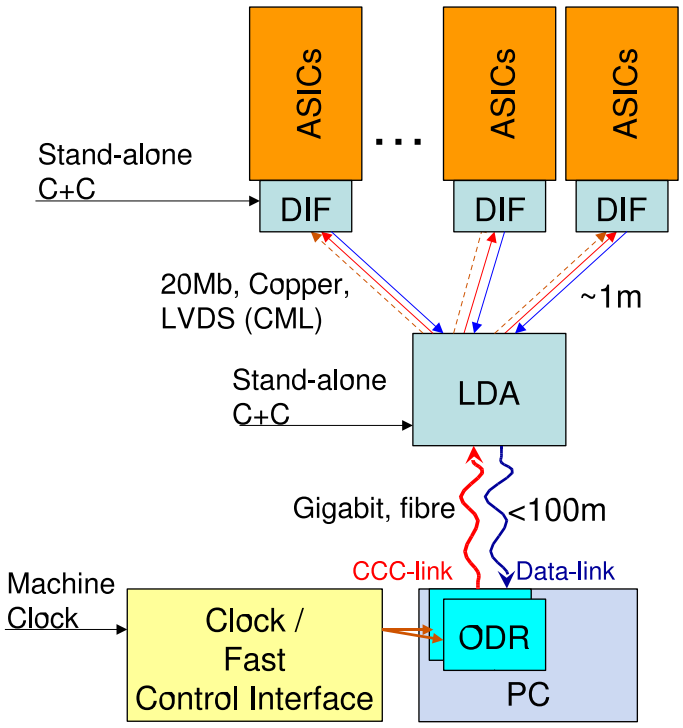

Figure 1: DAQ stream for EUDET prototype modules

The status of the PCI card development and hence the ODR is the main subject of this

memo as the prototyping of this forms the first milestone of the DAQ work in the JRA3 work-package of the EUDET project.

2 Current status of the off-detector receiver

The milestone, which was achieved before the prescribed date of June 2007, was the development of a prototype ODR as originally planned consisting of a system of PCI cards with a modern serial bus, in this case PCI Express [1], housed in a PC. The use of PCI Express as a serial bus forms part of the philosophy of using modern commercial technology. Other requirements were the ability to cope with high rates and large data volumes. To this end, the card was also required to have optical and copper links and a large FPGA.
It was originally planned to develop these boards and fabricate them, going through (at least) one iteration to perfect their production. However a survey of the needs of the board for the DAQ system and products available from companies revealed a set of boards from PLD Applications [2] which matched our exact needs and is shown in Fig. 2.

Figure 2: PCI Express prototyping board obtained from PLD Applications [2].

The main features of the PCI Express Xpress FX 100 board [3] of relevance to the DAQ system are:

- a large FPGA, Xilinx Virtex-4 FX100 [4];
- PCI Express $\times 8$ lane;
- Gigabit optical and copper transceivers;
- large, up to 2 gigabit, DDR-SDRAM2.

These cards are hosted in computers in our University laboratories. The next step was to write the firmware and test software to be able to pass data to and from and within the card. A modular structure was developed with each task forming part of a box diagram, with each box being the task of one person and all developed code placed in a central repository.
With the prototype firmware and test software, performance tests have started with an example shown in Fig. 2. This shows a series of plots, with different actions performed as described in the caption. From this study, it shows that file creation and closing is a bottleneck. Other studies have shown bottlenecks in disk storage. Optimal file systems and storage arrays are being consider to alleviate these bottlenecks, which will the allow us to assess the ultimate performance.

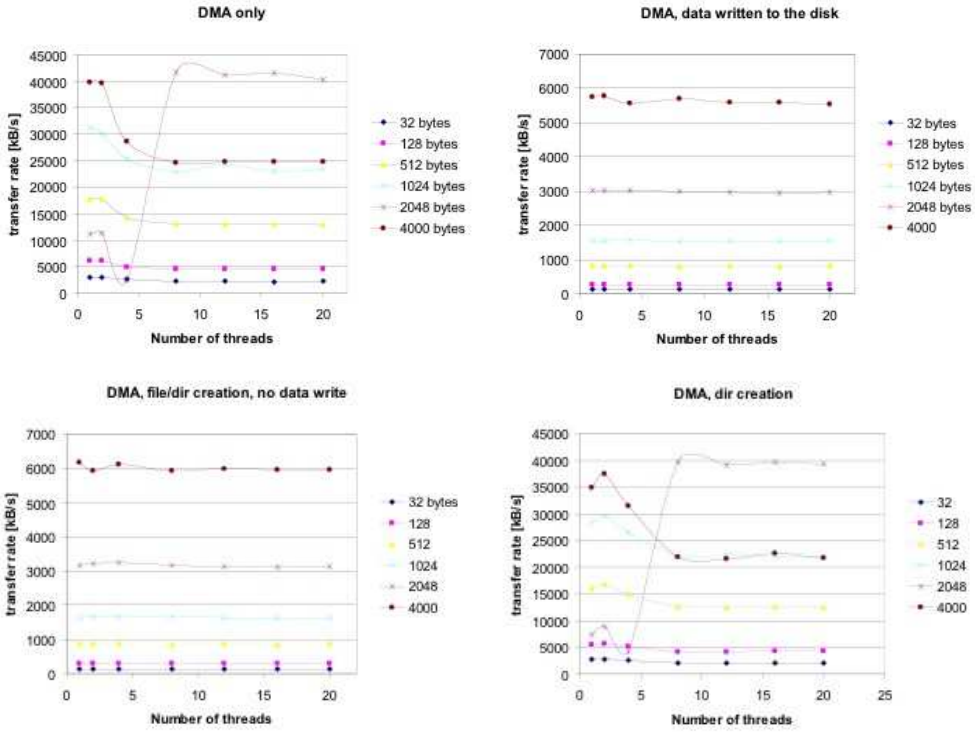

Figure 3: Examples of performance tests of data transfer for the PCI Express card. The transfer rate is shown versus the number of I/O threads and the plots are parametrised by data size. (a) shows the case for just DMA, (b) also includes writing data to disk, (c) includes file and directory creation, but no write to disk and (d) includes just directory creation.

3 Future plans

The next milestone for this task is the availability of the the DAQ system prototype, which should be complete by September 2008. The immediate tasks on the way to this goal are: definition of interfaces, such as the LDA-DIF connection; optimisation and measure of ultimate performance of PCI Express card; defining and building a clock, control and configuration system; and writing the DAQ software. Other ongoing and immediate work is to provide input to the ECAL design by testing new ASICs and investigating different layout options using a model test-slab.

Acknowledgement

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References

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[2] www.plda.com

[3] www.plda.com/products/board_pcie_fx.php

[4] www.xilinx.com/products/silicon_solutions/fpgas/virtex/virtex4/index.htm