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# Milestone Report: Analogue Telescope integrated in Beam

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**Abstract**

Within the EUDET JRA1 project a number of milestones were defined to ensure a successful outcome. This memo describes the EUDET JRA1 milestone "Analogue Telescope integrated in Beam" for summer 2007, the end of the first phase of the project.

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# 1 Introduction

Within EUDET JRA1 a test beam telescope will be developed. It will provide a high precision of better than 3 $\mu$m, even at the lower energies available at the DESY test beam facility. In addition to high precision, a high readout speed and easy handling is of importance.
The project is divided into two phases. During the first phase a first test facility with analogue readout and a much lower readout speed will be build. This gives the opportunity to check the design and to have a first telescope quickly available for the groups working on detector R&D. The use of an established pixel technology with analogue readout and no data reduction gives the possibility to have such a telescope ready on a very short time scale.
This memo describes the results of this first phase. In Figure 1 the time line of the project is shown. The Demonstrator Telescope is foreseen for summer 2007. At the same time the first test beam period at DESY is planned.

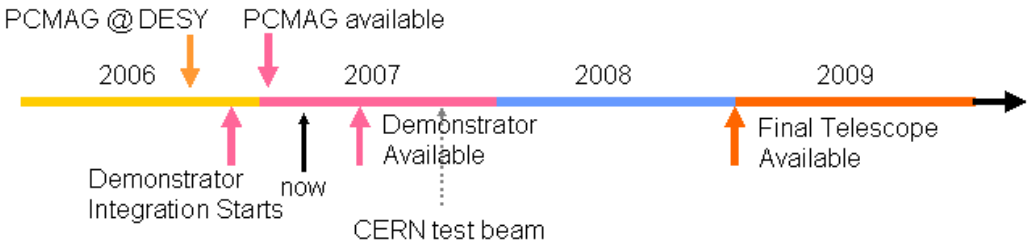


Figure 1: Time line of the EUDET JRA1 project.

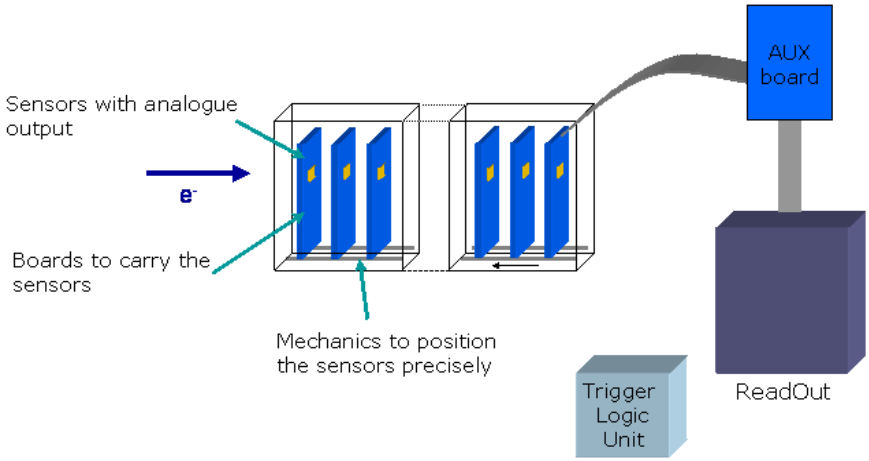


Figure 2: Overview of the ingredients needed for an analogue telescope.

In Figure 2 all "ingredients" for such an analogue telescope are shown. In the following sections the availability and status of all this components will be described.

# 2 Reference Plane Sensors: MimoTel

As sensors for the reference plane the MimoTel prototype is used. This is a chip processed in the AMS 0.35 OPTO process with 14 and 20$\mu$m epitaxial layer. It is subdivided into four sub-arrays of 64 $\times$ 256 pixel. The pixel pitch is 30 $\times$30 $\mu$m$^2$ resulting in an active area of 7.7 $\times$ 7.7 mm$^2$. The engineering run was in summer 2006 and the chips were received October 2006. From November to end of 2006, two test setups were prepared in parallel in Strasbourg: A Probe station setup preparation for wafer with 14 $\mu$m EPI and laboratory test setup for circuit tests with 20 $\mu$m EPI. End of 2006 to January 2007 the 14 $\mu$m EPI wafers were diced and the laboratory tests started.
It was soon evident that AMS did not respect one of the specifications given by Strasbourg: the high-resistivity poly was thinner than desired. This resulted in the DACs biasing being out of range, Therefore it was difficult to make the circuit working at nominal conditions. But by rearranging a number of passive components on the sensor boards this problem could be solved. This problem did not affect Mimosa18, the high resolution sensor for the telescope.
The necessary PCBs to hold the sensors and to refresh the signals traveling from and to the sensor chips were produced in Strasbourg and populated in Strasbourg and at DESY. By early summer 2007 the PCBs were produced and enough chips were tested to equip the Demonstrator.

# 3 EUDRB (EUDET Data Reduction Board)

The DAQ Card developed by INFN (EUDRB) consists of:

- One mother board, hosting an ALTERA Cyclone II FPGA and the core resources (SRAMs, FIFOs, VME64x interface, trigger port, diagnostic UART). A 32 bit soft (NIOS II) microcontroller implemented in the Cyclone II FPGA handles tasks like on board diagnostics, on-line calculation of pixel pedestal and noise (not interfering with data taking operations), and remote configuration of the FPGA via RS-232, VME, and USB2.0. The clock rate of the FPGA is 80 MHz (40 MHz for the NIOS II processor), and the clock rate of the A/D converter is up to 20 MHz.

  Functionality of motherboard includes on-line calculation of pixel pedestal and noise, cluster finding, ADC, remote configuration of the FPGA, on-board diagnostics.

- One analog daughter card with 4 independent signal processing and digitizing stages

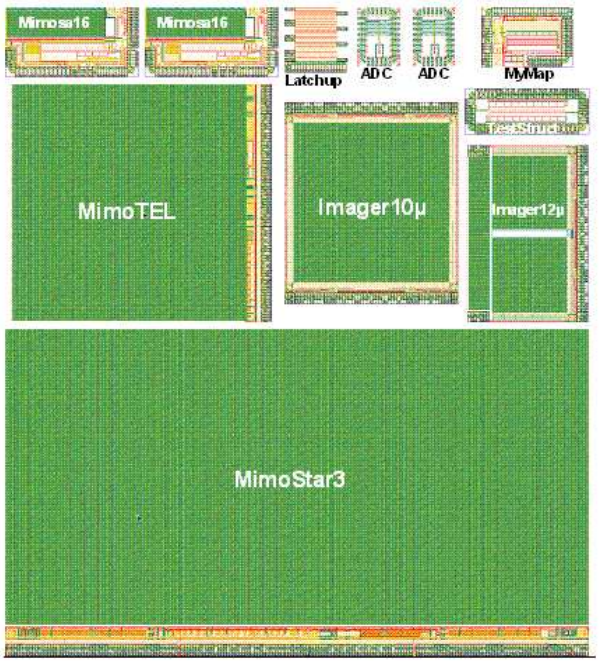


Figure 3: Layout of the reticle of the engineering run AMS-035 OPTO 07/2006 on 14 $\mu$m (standard) and 20 $\mu$m epi substrate

- One digital daughter card, featuring a standard PCI Mezzanine Card interface to the mother board. It drives/receives control/status signals for the detectors and it features a USB 2.0 link.

The EUDRB also implements the interface to the EUDET trigger bus and a VME64X slave interface capable of 2e-VME transfers (for a peak bandwidth of about 80 to 100 MB/s).
The whole system can run in two readout modes:

- Zero Suppressed readout to minimise the readout dead-time while in normal data taking.
- Non Zero Suppressed readout of multiple frames for debugging or off-line pedestal and noise calculations.

### 3.0.1 Full Frame readout mode:

The card responds to a trigger by sending out all raw pixel data for at least three frames: the frame being acquired at trigger time, the preceding one and the following one, for a total of 6 MB per event. The TRIGGER BUSY is set as soon as the trigger is received and released when data has been transferred to the host PC.

#### 3.0.2 Zero Suppressed readout mode:

The card responds to a trigger by sending out a formatted block which includes a header and a trailer identifying the event number and the number of hits. Processing of triggers in this mode does not stop the scan of the detector and therefore no data are lost due to trigger processing. The trigger processing time is at least one frame time. The TRIGGER BUSY is set as soon as the trigger is received and released when data has been transferred to the host PC.

The EUDRB boards were delivered end of July 2006 and all initial tests of hardware were successful. The operation connected to a sensor (Mimosa V and MimoTel) was performed before the test beam period in June 2007. The USB-2 link is fully working and can be used for diagnostics and debugging. Both the zero- and the non-zero-suppressed modes are established and the board has been tested with the MimoTel sensor Also the TLU interface has been integrated before the test beam.
Altogether 6 boards (+spares) are needed for the complete telescope. For the first test beam in June 2007 three EUDRBs were available, the number agreed before by the collaboration.

# 4 Data Acquisition

The main challenge of this telescope is integration of the different DAQs. The typical telescope users will bring their own DAQ and should not need to invest time in rewriting code or reconfiguring the hardware. A "plug-and-play" system would be desirable. Therefore it was decided to use different hardware and DAQ for the DUT and the reference planes, and to integrate the two systems on the trigger level. Synchronisation will be done with the Trigger, Busy and Reset signals. The Readout Software, DAQ and data storage is provided by the DUT user. The events are then combined offline.
The basic idea for the DAQ software was to create a simple and easy to use DAQ system for the beam telescope and distributed across multiple computers. The software framework was based on a DAQ software written by the DEPFET group in Mannheim and Bonn.
For sending of the data and command sockets are used. Furthermore is the software reasonably portable, achieved by the use mainly standard C++.
One main Run Control controls the DAQ:

- Controls all the other applications Producer
- Communicates with hardware and sends data to Data Collector

Data Collector:

- Collects and merges data from all Producers

Monitor:

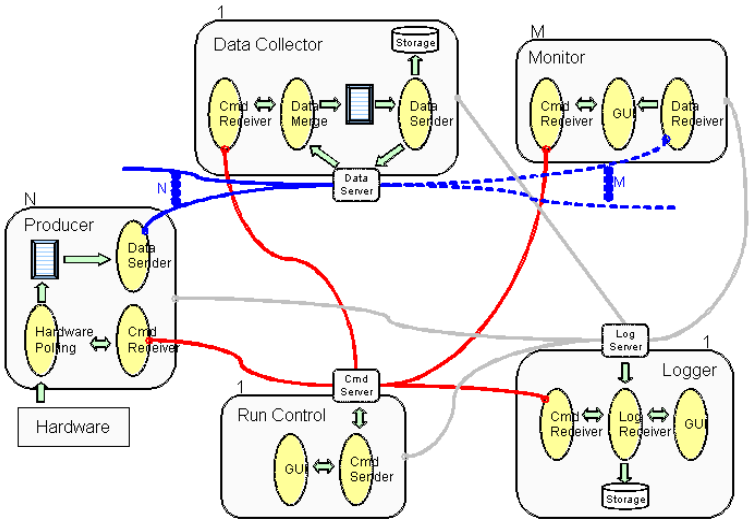


Figure 4: Organigram of the DAQ software.

- Receives data from Data Collector for display/statistics

Logger:

- Collects logging messages from other applications

It was also decided to use LCIO/Marlin for data storage and processing. The Data will be sent within the DAQ in a simple custom format, and converted to LCIO before being written. In Figure 5 screen shots of the DAQ software are shown. A first version is available for the use in the DESY test beam June 2007.

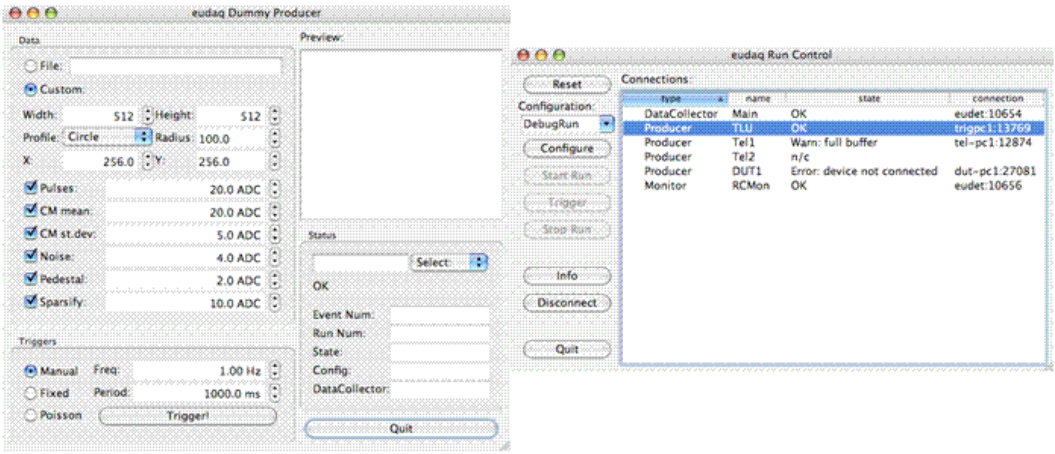


Figure 5: Screen shot of the DAQ software for the DESY test beam.

# 5 Conclusion and Outlook

In the previous sections it was shown that all the components necessary for an analogue telescope in beam are ready and can be tested during the first test beams at DESY in June 2007. The JRA1 collaboration already agreed on the next important steps towards a complete telescope in beam by September 2007. Table 1 summarises these milestones.

| item | Name | Date | Partner | Description/Remarks |
|---|---|---|---|---|
| 1 | TLU | 18 Oct 06 | Bristol | TLU working. Ship to Geneva. |
| 2 | DAQ0 | 18 Oct 06 | Geneva, Bonn Strasbourg | DAQ + TLU work together |
| 3 | FE0 | 15 Jan 07 | DESY | 15 Populated FE board sets with sensors available. Ship to Ferrara, Geneva, Strasbourg. |
| 4 | EUDRB0 | 15 Jan 07 | Ferrara | EUDRB board partial functionality. Ship to Geneva |
| 5 | DAQ1 | 5 Mar 07 | Geneva | DAQ partially integrated with EUDRB |
| 6 | EUDRB1 | 5 Mar 07 | Ferrara | EUDRB board tested with FE board set and sensor. Ship 1 full set to Geneva. |
| 7 | FE1 | 5 Mar 07 | Strasbourg, Geneva, Ferrara, DESY | FE board sets fully qualified |
| 8 | EUDRB2 | 30 Apr 07 | Ferrara | 2 EUDRB boards synchronized. Ship 1 set to Geneva and 1 set to DESY |
| 9 | DAQ2 | 31 May 07 | Geneva | DAQ fully integrated with two full FE board sets + EUDRB |
| 10 | TB0 | 10 June 07 | DESY | Mechanics and TB infrastructure ready for integration |
| 11 | Int1 | 10 June | All | One Demonstrator Arm in beam |
| 12 | int2 | 15 Aug | All | DESY test beam with improved DAQ and two arms |
| 13 | Int3 | 12 Sep | All | Demonstrator Ready for shipping to CERN |
| 14 | DEMO0 | 19 Sep 07 | All | Demonstrator in SPS beam |

Table 1: List of milestones within JRA1

# Acknowledgement

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