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SITRA/SiLC beam test in 2006

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Abstract

During October and November 2006 first SITRA/SiLC test beam took place at DESY. Here 3 prototype modules were tested in a beam of 1-6 GeV electrons. Data acquisition system was set up that allowed synchronisation of trigger and telescope signals with signals read by SITRA electronics

1 Introduction

SITRA is one of the tasks of the JRA2/EUDET reasearch activities. Its aim is to provide silicon tracking infrastructure for R&D groups for the future International Linear Collider (ILC). It's closely linked to the SiLC R&D [1, 2].
During October and November 2006 first SiLC test beam took place at DESY. Here 3 prototype modules were tested in a beam of 1-6 GeV electrons. 3 module prototypes were placed in the beam line after the telescope set (see Fig. 1). Data acquisition system was set up that allowed synchronisation of trigger and telescope signals with signals read by SITRA electronics

2 Module prototypes

Several modules have been built using various sensor and chip generations during last years. Summary of 3 recent prototypes is at the Table 1. Here several features foreseen for the final detector have been implemented (both mechanical and electronic) to evaluate their performance and usability.
The modules built have been tested at a test bench in Paris using signal generated from laser stimuli.

3 Electronics

The general architecture of the front end chip is based on a low noise preamplifier, a pulse shaper, a zero suppression decision, a sampling analogue pipe-line, an analogue to digital converter, a digital buffer, an internal calibration, and a power switching circuitry for power cycling. Two ranges of shaping times are implemented, namely a "slow" shaping time between 500 ns and a few μs, and a "fast" shaping time focusing on a few tenths of ns, in order to obtain a rough measurement of the z coordinate along the beam axis.

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Notation	sensor	pitch [μm]	total length [mm]	FE electronics
A	GLAST	228	900	228 nm + VA1
B	CMS	183	283.5	180 nm + VA1
C	CMS	183	283.5	VA1 (reference)

Table 1: Characteristics of the module prototypes and their associated F.E. electronics

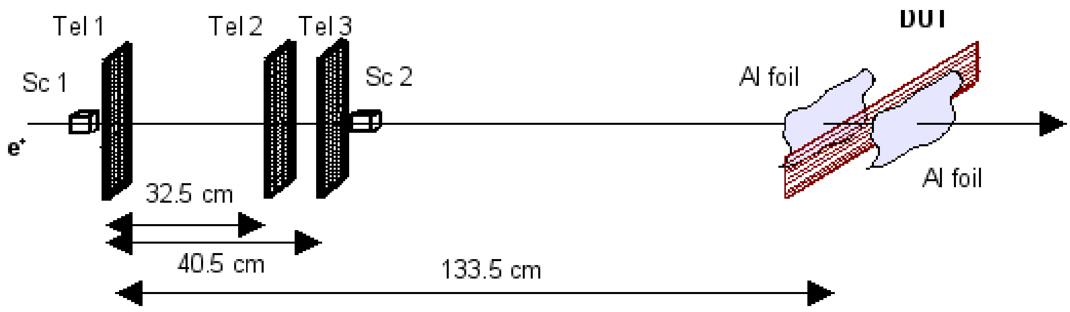

Figure 1: Telescope and DUT arrangement in November 2006

This fast shaping time could also be used to provide a fine BCO tagging in case of high occupancy in some regions. As one of the first results of the SiLC R&D program, a test chip in 180 nm CMOS technology has been designed and tested. Results have been encouraging concerning the main specifications such as noise and power. It confirms that a power dissipation below 1 mW/channel for the system from the preamplifier to the end of the front-end chain described above is achievable [3]. These chips have been built into two modules.

4 Beam test

Further performance evaluation has been done at the first SiLC beam test which took place in October 2006 in DESY, within both the SiLC R&D program and the EUDET E.U. project. Here modules were placed in the specially designed Faraday cage and tested in the beam of 1-6 GeV positrons (see Fig. 1).

4.1 Beam telescopes

DESY based ZEUS telescopes were used to determine the beam position. They were 50 μm-pitch strip detectors oriented both in x and y, thus giving 2-dimensional information with the precision of about 20 μm. The track precision in the setup used has been limited by several factors, namely by multiple scattering of low-energy beam and not optimised geometry. The readout system was VME PowerPC based and the operating system was Lynx [4].

4.2 SITRA DAQ

Labview DAQ SW from Paris controlling the National Instruments PCI scope card was used to read out the DUT – silicon strip module prototypes.

4.3 Synchronisation

Both readout system have been used in parallel. Synchronisation of the events was done via the set of NIM modules, where BUSY signals of both systems were ORed and served as VETO for triggers. The crosscheck of both systems was performed in the Canberra 512 Dual Counter/Timer. Here BUSY signals of both systems were counted, giving the relative correspondence of the event. This helped to reveal the event slippages in the offline analysis.

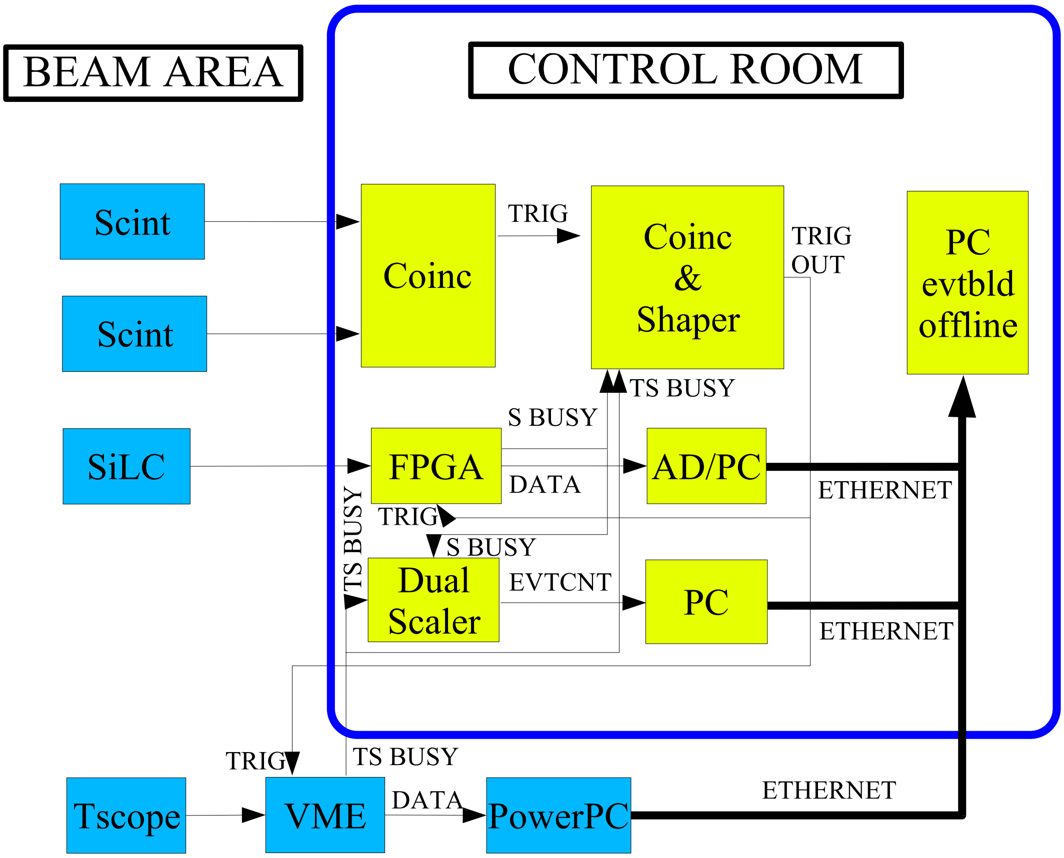

Figure 2: DAQ setup in November 2006

Bias voltage [V]	S/N (MPV)
200	13.62
260	15.79
299	15.70
350	16.52

Table 2: Signal-to-noise vs. bias voltage

5 Results

The data acquired were analysed in a standard way and basic results were obtained. The figures 3 and 4 and Table 2 show S/N spectrum and correlations. The spatial resolution achieved was basically driven by geometry not optimised for the multiple scattering. The comparison of measurement and GEANT4 simulation is shown at Fig. 5.

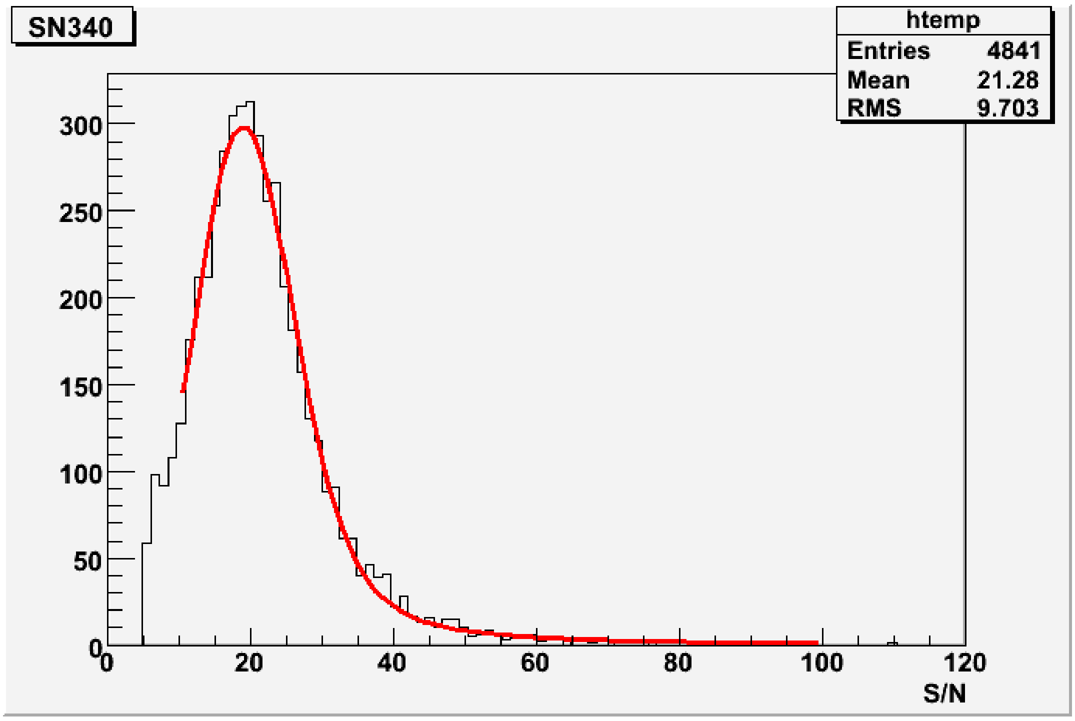

Figure 3: Amplitude spectrum of signal, in units of Signal-to-noise

6 Conclusions

Despite non optimised geometry and problems in data acquisition the DESY test beam in 2006 was a very important step in development of silicon tracking prototype within

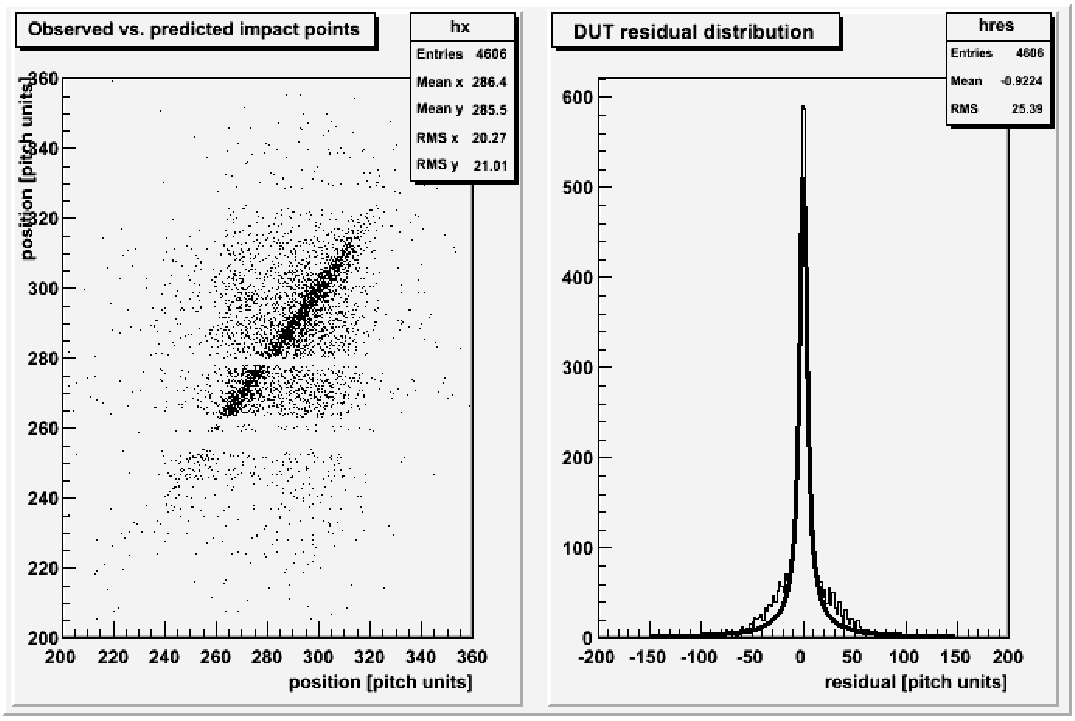

Figure 4: Correlation between predicted and measured position(left), Residuals(right)

the EUDET/SITRA project. Given its limitations further beam test is needed to obtain more results.

Acknowledgement

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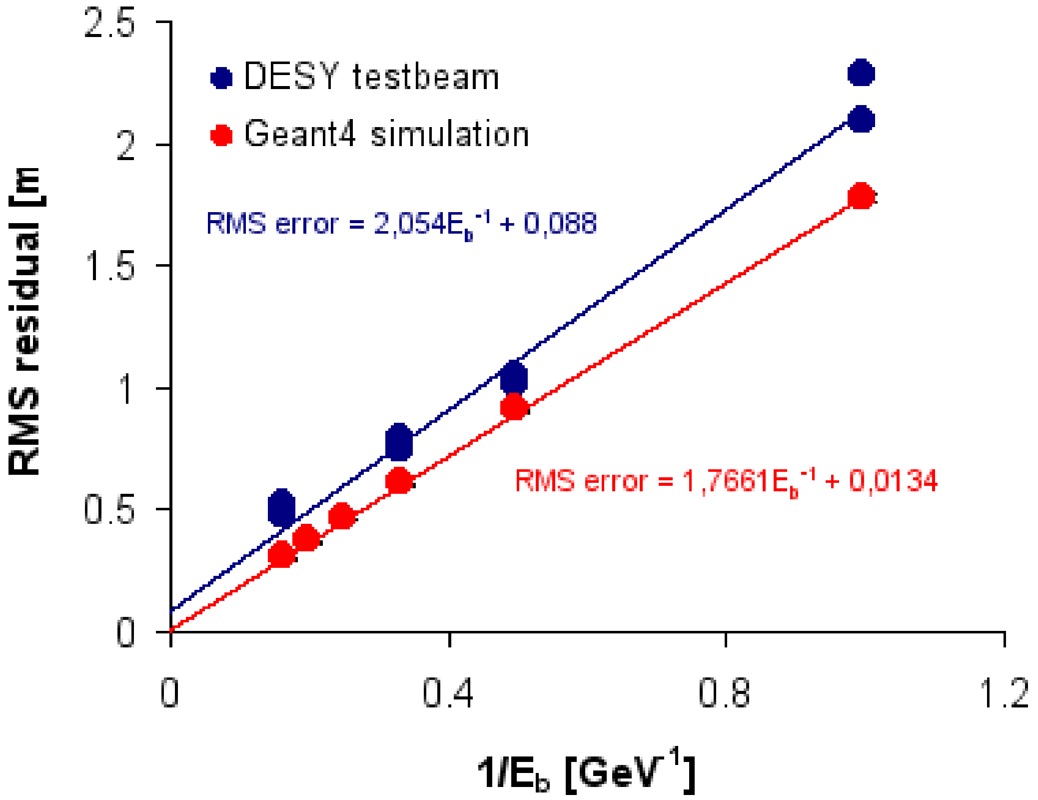

Figure 5: Infinite energy extrapolation for the 2006 beam test configuration (simulation and measurement

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