Generic Silicon Strip Detector R&D

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Abstract

The baseline of the SiLC (Silicon for the Linear Collider) collaboration for future silicon strip detectors is presented together with ideas to reduce material budget and thus the effect of multiple scattering in the detector modules using a novel module design. It proposes to integrate large parts of the front-end hybrid directly into the silicon sensor by the help of additional routing lines. The current status of sensor production with a company (Hamamatsu) is presented with first results from measurements on these detectors. Another goal of the collaboration is to establish new sensor producers. For this, contacts with vendors like VTT, ON Semi and ITE Warsaw have been established. The status of these collaborations and results from first prototypes are presented.

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1 Introduction

The SiLC (Silicon for the Linear Collider) collaboration is a generic R&D collaboration to develop the next generation of large area Silicon Detectors for the ILC. It applies to all detector concepts and gathers teams from all proto-collaborations. The collaborators of SiLC which are also EUDET partners are forming the SiTRA (Silicon Tracking) group. This group has, together with the whole SiLC collaboration, developed plans for development of new silicon strip sensors, established contacts to different semiconductor detector producers and established a comprehensive quality assurance based on the experiences gathered during the CMS silicon sensor procurement.

2 SilC Silicon Sensor Baseline

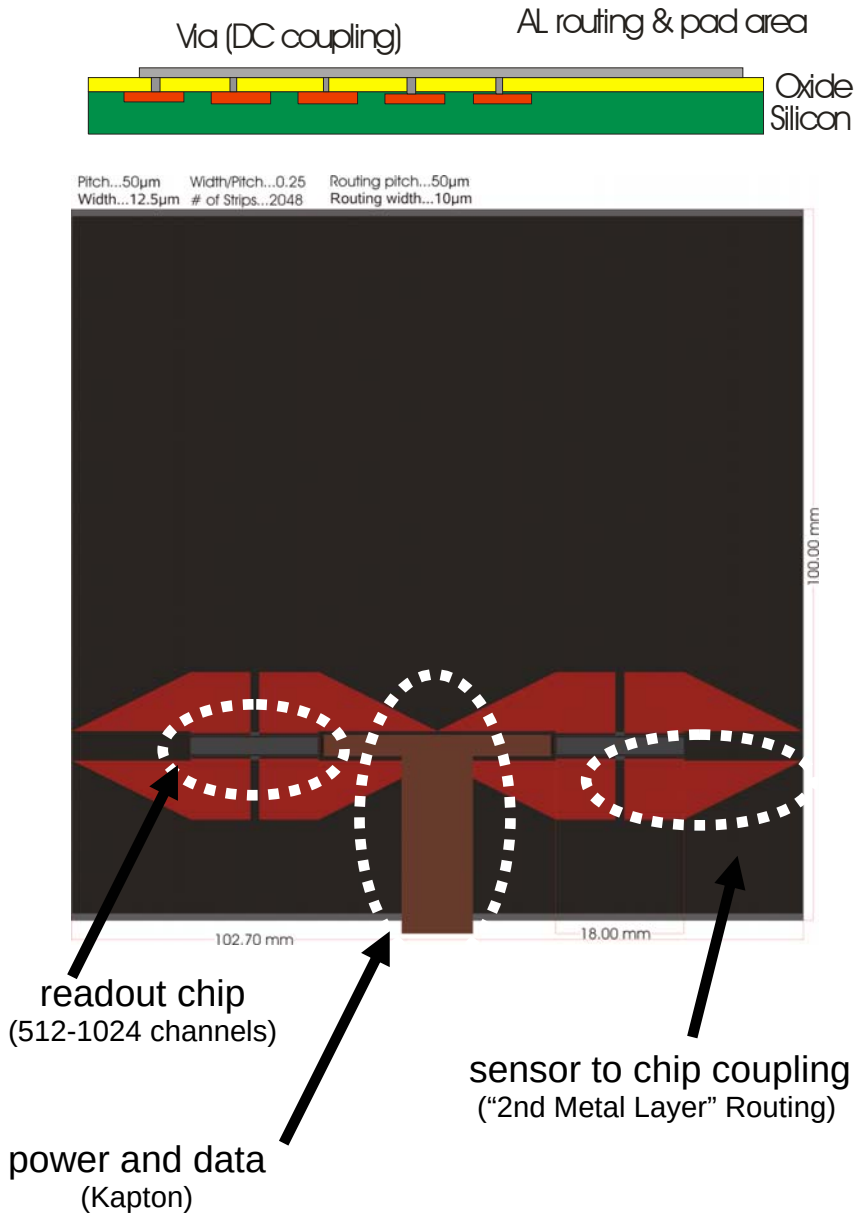
A baseline sensor design has been established to get comparable results from different sensor producers. Since future silicon strip sensors for the ILC will need a very high resolution, a readout strip pitch of 50µm is foreseen, possibly with intermediate strips in between, resulting 25µm pitch. Smaller pitch becomes very complicated in terms of wire bonding, contacting the strips with needles for testing but also because of the fact that the charge generated by particles traversing the detector is shared by too many strips reducing the effective S/N ratio.

The sensor bulk material is agreed to be p-on-n float zone silicon, which means that there are p+ implants for strips in n-type bulk material. The bulk material should be of high resistivity (5-10 kΩ cm) and rather thin (100-300µm). However, the lower limit of the thickness is limited by the noise figures of the readout chip. The detector must have a very low dark current of <1nA per strip, since the noise is mostly defined by the dark current and bias resistors. This is true for long integration times because of the beam time structure of the ILC. This implies very high values for the bias resistor in the order of 20 to 50 MΩ, realized either using poly-silicon, punch-through or FOXFET technique. While poly-silicon has been used for LHC (since it is more radiation hard), PT or FOXFET would be cheaper.
For the inner silicon layers, we propose AC coupled double sided detectors made on 6" wafers, while for outer layers, larger wafers of 8" or even 12" inch would be needed to reduce the material necessary for mechanical support. In this region, we propose single sided detectors preferable DC coupled for cost reduction

3 Material budget minimizations

Since multiple scattering is a crucial point for high-precision ILC experiments, the amount of material inside the detector must be kept on a very low level to avoid degradation of the feasible resolution of the devices. For silicon strip modules, a possible solution to address this issue would be a reduction of the active material by thickness reduction of the silicon itself with the drawback of a reduced signal. A much more effective way is the minimization of the non-active material like the module support carrier, the front-end hybrid, the readout chips on it and the pitch adapter which is used to connect the silicon sensor to the readout electronics. The most radical solution is to integrate the pitch adapter completely into the sensor. The connectivity of the strips to the readout chip can be made by an extra metal layer for signal

routing which is separated from the strips using an additional oxide layer. In this scenario, the readout chip can be bump-bonded onto the sensor as for pixel detectors. This is shown in the following figures.



4 Future SiLC Work Program

To achieve the goals mentioned above, the work program for the future has been separated into three steps.
Step 1 is has already started and comprises mostly of preparatory steps for the long term goals, in particular to build silicon detector modules with long strips and strip pitch of 50 µm. Another important point is to improve the test structures and test setups to allow effective testing and determination of process parameters during sensor production. Along this, tests of new readout chips for DC coupling and power cycling are foreseen.

The next step starting in 2009 is separated into three parts. For the first part it is planned to build silicon detectors with in-sensor-routing and to test the crosstalk and capacitive load of those sensors. Secondly, vendors interested to build 6” double sided sensors are asked to build prototypes of those sensors which will be thoroughly tested. Finally, the third part comprises of a similar goal but for 8” or even 12” inch single sided DC wafers.

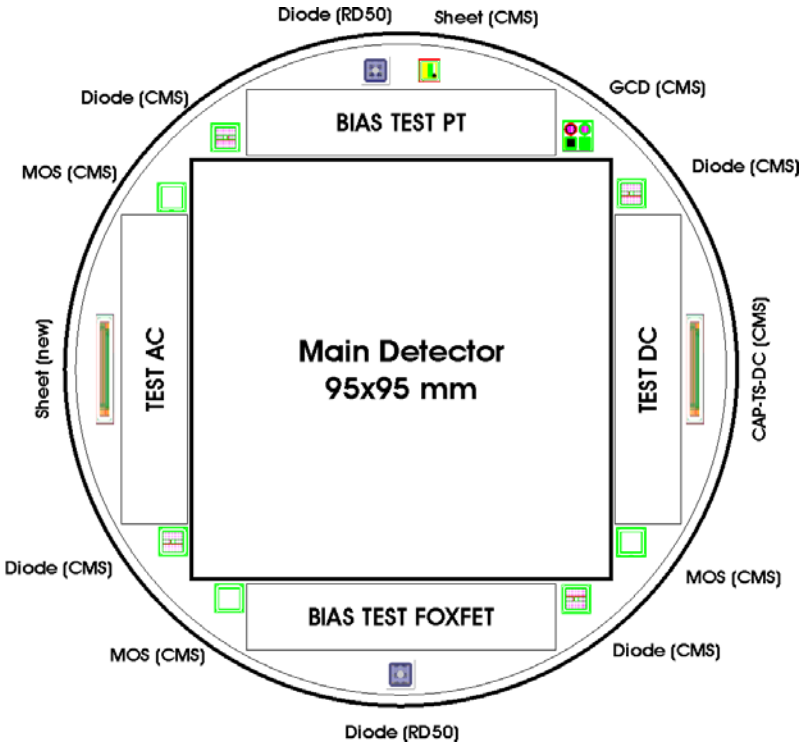
5 Status of Sensor Producers

The SiLC collaboration is in contact with different sensor producers and has already started to collaborate with them to produce the first prototypes according to the first step of the work program. Only vendors which are willing to collaborate and to provide sensors and test structures now are considered for the future parts of the work program.

5.1 Hamamatsu

One batch of silicon sensors has been ordered at Hamamatsu Photonics (HPK) in Japan. This order consists of 30 normal sensors plus 5 “alignment sensors” which have a hole in the backplane metallization to allow laser light to pass through the silicon.

The layout of the Detector was design by the SiLC collaboration together with HPK and the result is shown in the following figure.



It is a single sided AC coupled strip detector with a sensor size of 91,5 x 91,5 mm² and a thickness of approx. 320 µm. The resistivity was requested to be such that the depletion voltage is between 50 and 100 Volt, while the leakage current is requested to be below 10 µA per sensor. Poly-silicon resistors with 20 MΩ (± 10 MΩ) have been chosen to bias the 1792

strips, which are placed on the sensor with 50 µm pitch, without intermediate strips. The strip-to width ratio was set to 25%, which results in a strip width of 12.5 µm. A dielectric sandwich structure of Oxide (SiO_2) and Nitride (Si_3N_4) between the implant and the readout metallization was requested.

This main detector will be used to

- Build prototype modules to test new readout chips
- Build modules for LC-TPC project
- Build long ladders

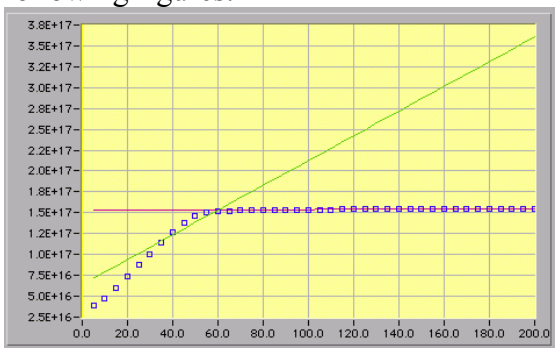
Various test structures have been placed around the main detector on the wafer. Apart from common diodes and MOS structures, there is a gate-controlled diode, dedicated structures to measure inter-strip resistance and capacitances. Aluminum, p^+ implant and poly- Silicon lines are available to determine the sheet resistivities.
Four large test structures have been designed with two different purposes. Two structures called TESTAC and TESTDC are geometrically identical, but one is made with AC-coupled strips while the other is made DC-coupled. Both comprise 256 strips with the same pitch as the main detector, but with regions of different strip widths and different intermediate strips. Each region consists of 16 individual strips with the same geometry. The following table shows the exact layout.

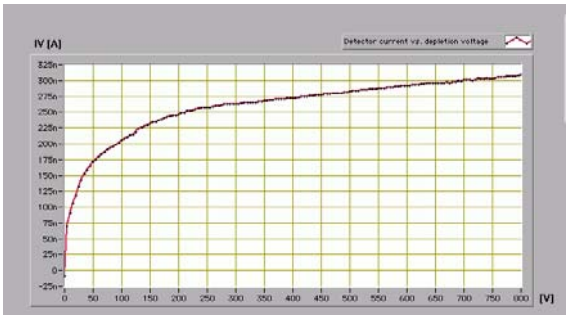
strip width [µm]	intermediate strips
5	no
10	no
12.5	no
15	no
20	no
25	no
5	single
7.5	single
10	single
12.5	single
15	single
17.5	single
5	double
7.5	double
10	double
12.5	double

Both structures will be used to test cross-talk and inter strip capacitances in a test setup and the resolution in a future beam test.

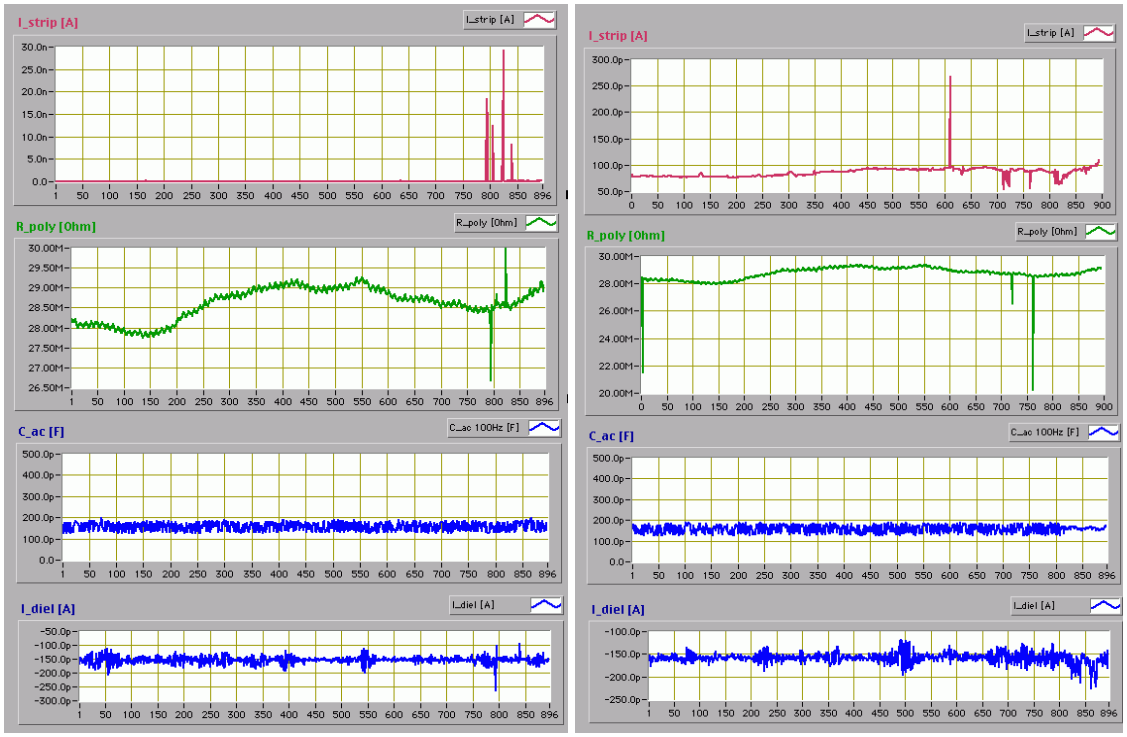
The two other test structures on the wafer are called BIASTEST FOXFET and BIASTEST PT (punch-through). These structures are also geometrically identical and comprise 128 channels with a pitch of 50µm, but take advantage of different biasing schemes: FOXFET and punch-through. While the first one is like a MOS transistor, the second one is similar, but without a gate metallization. These structures will be used to test both biasing methods in contrast to the poly-Silicon biasing of the main detector.

We received the sensors in October 2007 and first measurements have already been performed. The results are as expected for the resistivity and the dark current behaviour. This is shown in the following figures:





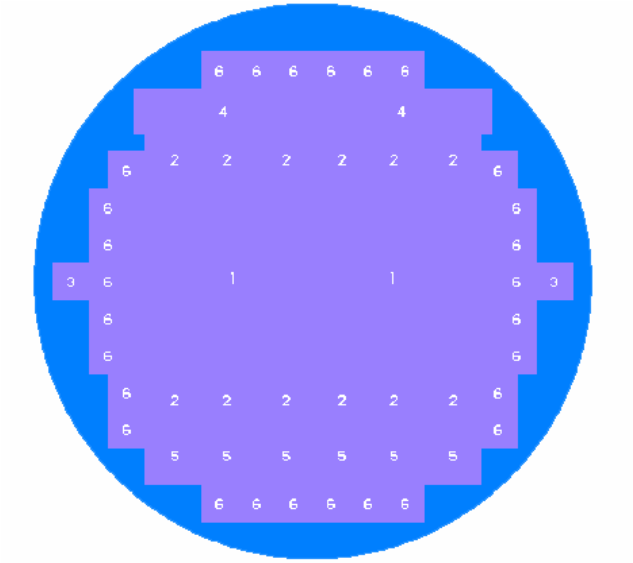
Both, resistivity and dark current meet the requirements. On one sample of the sensors, a full strip scan has been performed as well. It consists of the determination of the single strip dark current, the poly-Si resistor value, the coupling capacitance and the dielectric current. These measurements are repeated for every single strip. Results are shown in the following figures for the even (left) and the odd strips (right) of the sensor.



The results show that the sensor is well within the specified limits. No pinhole has been found. The value of the poly-silicon resistor is around 28.5MΩ and the coupling capacitance is around 160pF. This results in a thickness of the dielectric which is approx. 30% thicker than comparable sensors for CMS.

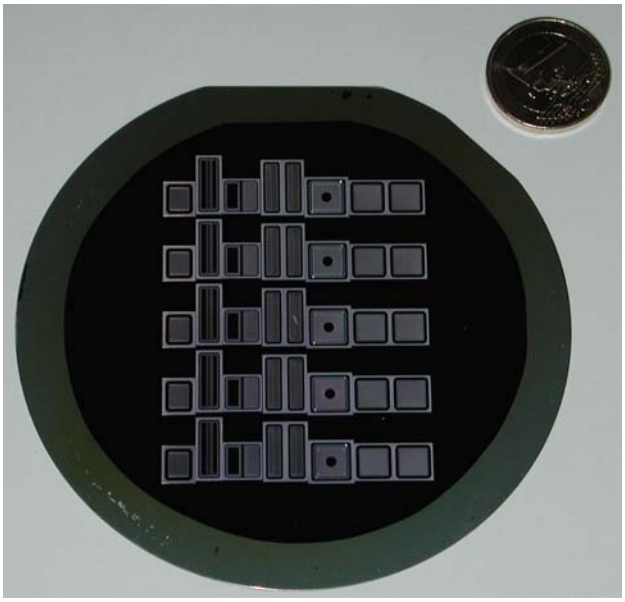
5.2 VTT

VTT (*Valtion teknillinen tutkimuskeskus*) is a large technical research center in Finland. The goal of the collaboration is the development edgeless detectors. We agreed to build two main sensors with 5 x 5 cm^2 on 4" wafer, one DC coupled and the other one AC coupled with FOXFET biasing. These sensors are labeled with (1) in the drawing below. Apart from that, there will be similar test structures on the wafer like for IET and HPK (4). Additionally, there are many edgeless test structures (5) with an area of 1.5 X 1.5 cm^2 and conventional baby detectors (6) with 1 X 1 cm^2 around. The wafer design is finished and the processing at VTT has been delayed due to the lack of the resources. The current plan is to finish it by the end of the year.

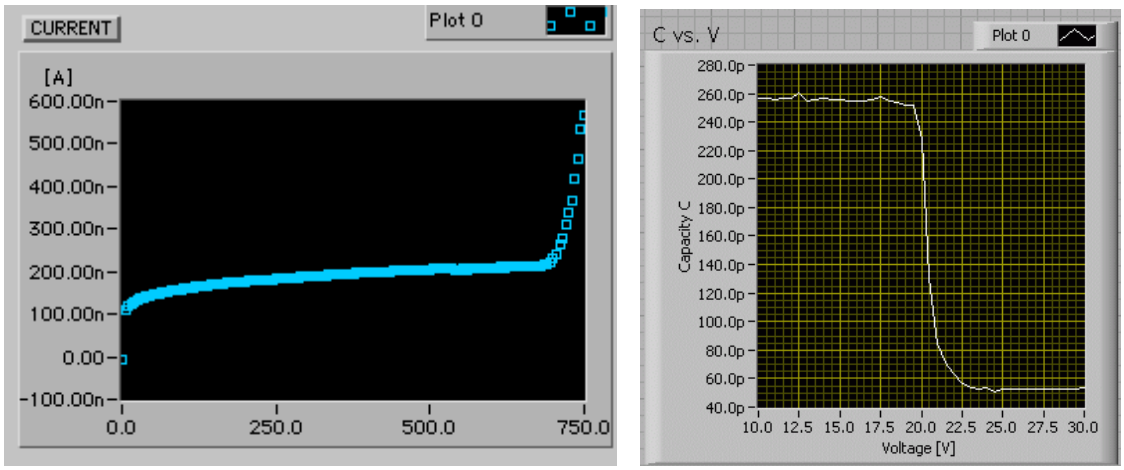


5.3 IET Warsaw

The contact with *Institute of Electron Technology* in Warsaw was established already three years ago with the goal to develop test structures and sensors. Up to now the institute has experience with SOI and chip production, but not with fully depleted devices. This collaboration started with the design of test structures with the goal to be able to produce full detectors in the future. The test structures have been processed on 4" wafer this summer. A picture of the wafer can be seen below.



Measurements on these structures have been performed in Vienna and Karlsruhe and the results are promising. However, some issues have to be discussed with the producer to improve future batches. The dark current of one wafer was very low with a break through voltage of above 700 V (left picture), while it was around 50V for another wafer. The oxide charges determined by measuring the flatband voltage on a MOS structure (right diagram) were too high for detectors being operated in a radiation-harsh environment.



Despite these minor issues the results are excellent for the first batch of wafers received and we are looking forward to discuss our measurement results with IET for improvements of the next production.

5.4 ON Semiconductor

ON Semiconductor is a company located in Czech Republic. It now belongs to an US group, but they have already experience with detectors under their former name “Tesla”. This company is able to produce 4” and 6” with a rather high throughput. After establishing the first contact in June this year, we agreed to start collaboration with the goal to design and build sensors and test structures with dual-metal layers. The design of those sensors already started in Vienna and the procurement of 6” wafer is also ongoing. We will submit the first design for verification by the end of the year.

6 Summary and Outlook

The SiLC collaboration and the EUDET partner institutes had a very fruitful year. The sensor baseline was defined to have a clear starting point for discussions with each sensor producer. It was presented to HPK and it was agreed to order detectors based on this design. 30 sensors have already been delivered by HPK in October, which have successfully passed the QA measurements done in Vienna. Two of them have already been used in a test beam which took place in October this year at SPS at CERN.
One of the goals of the SiLC collaboration is to establish companies to deliver silicon detectors for future HEP experiments. With this in mind, new fruitful collaborations started with VTT, ON Semi and IET with very promising results, which allows us to go to the next step with these vendors very soon. This helps to establish the procedures, processes and contacts with the producers very early to have a good basis for future steps. Other vendors willing to cooperate in the future have to fulfill the same requirements which these vendors already passed.

The next goals are the development of sensors with dual metal layer structure for in-sensor routing. Together with this, a cheap, industrial bump-bonding technology must be established to take full advantage of this technique. In parallel, sensor producers will be encouraged to

build doubled sided detectors, together with evaluation of companies capable of 8” inch or even larger wafers.

Acknowledgement

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