Silicon Strips Detectors Readout Chip in Deep Sub-Micron CMOS Technology

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Abstract

In the context of the Silicon for a Linear Collider (SiLC) R&D supported by the EUDET I3-FP6 , a 4-channel evaluation chip intended to read Silicon strip detectors has been designed in 130nm CMOS technology, and successfully tested. Optimized for a detector capacitance of 10 pF, it includes four channels of a full signal processing chain, including low-noise charge integration and pulse shaping, a 16 deep-analog sampler triggered on an analogue sum of adjacent inputs, and a parallel 10-bit analog to digital conversion. Laboratory and in-situ tests results of the chip are reported, demonstrating the behavior and performance of the full sampling process and analog to digital conversion, on a laboratory test stand, and from radioactive source as well as beam tests. Each channel occupies an area of 100 x 600 square microns on Silicon, and dissipates less than half a milliwatt of static power.

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1 Introduction.

This R&D aims at integrating in Deep Sub Micron CMOS technology the readout electronics required by Silicon strips detectors for a future International Linear Collider (ILC), in the context of the SiLC (Silicon for the Linear Collider) international project, that includes several worldwide institutes.

The main characteristics of the Silicon detectors are :

- A few millions Silicon strips 10 - 60 cm long,
- Detector thickness between up to 300 μm,
- Strip pitch between 50 and 120 μm

In such detectors readout Front-End electronics, the integration of a k-scale channels readout chip is deemed necessary. The R&D aims at demonstrating that the of Deep-Sub-Micron CMOS technology allows such an integration, merging low-noise analog amplification and pulse shaping, mixed design blocks such as AD converters, and pure digital electronics.

A transverse resolution of a few micrometers is expected from the detectors, requiring pulse amplitude measurements, and time has to be also recorded in order to identify Beam Crossings at 150-300 ns intervals. To achieve such a performance, pulse height and time will be reconstructed from data obtained using detector pulse analog sampling. A shaping time of the order of the microsecond depending upon strip length (capacitance) is envisaged to optimize the signal to noise ratio. A 6-12 MHz analog pulse sampling followed by on-chip digitization on 10-12 bit should allow to reconstruct efficiently both amplitude and time. On chip pre-processing using DSM is envisaged [1-6].

2 Milestones.

A first milestone is the implementation and tests of a demonstrator 4-channel chip in Deep-Sub-Micron CMOS technology fulfilling the requirements of the SiLC detectors readout, as reported below.
A second milestone will be the implementation of a 128-channel chip, using the building blocks tested with the 4-channel chip (First milestone). The following functionalities are planned:

- Preamp-Shaper Gain of 30mV/MIP
- Sparsification Trigger decision on analog sums,
- Sampling 8-deep sampling analog pipe-line,
- Dynamic range 30 MIP
- Analog event buffering: 8-16 deep event buffer,
- On-chip digitization 10-12 bit ADC,
- Buffering and pre-processing, centroids, least square fits, lossless compression and error codes,
- Calibration and calibration management,
- Power switching (useful at the International Linear Collider where a 1:200 duty cycle is envisaged.

The following quantitative specifications are targeted:

- Integration of at least 128 channels in 90nm CMOS:
- Amplifiers: - 30 mV/MIP over 30 MIP range
- Shapers: - Two ranges: 500ns–1ms, 1ms-3ms
- Sparsifier: - Threshold the sum of 3-5 adjacent channels
- Samplers: - 8 samples at 80ns sampling clock period
- Event buffer 8-16 deep
- S/N = 20 @ 90cm long strips
- ADC: - 10 bits
- Buffering, digital pre-processing
- Calibration
- Power switching in order to save a factor up to 200 at the ILC.

A third milestone will be the implementation of a 1000-channel chip in 90nm CMOS technology, the final one to equip the detectors.

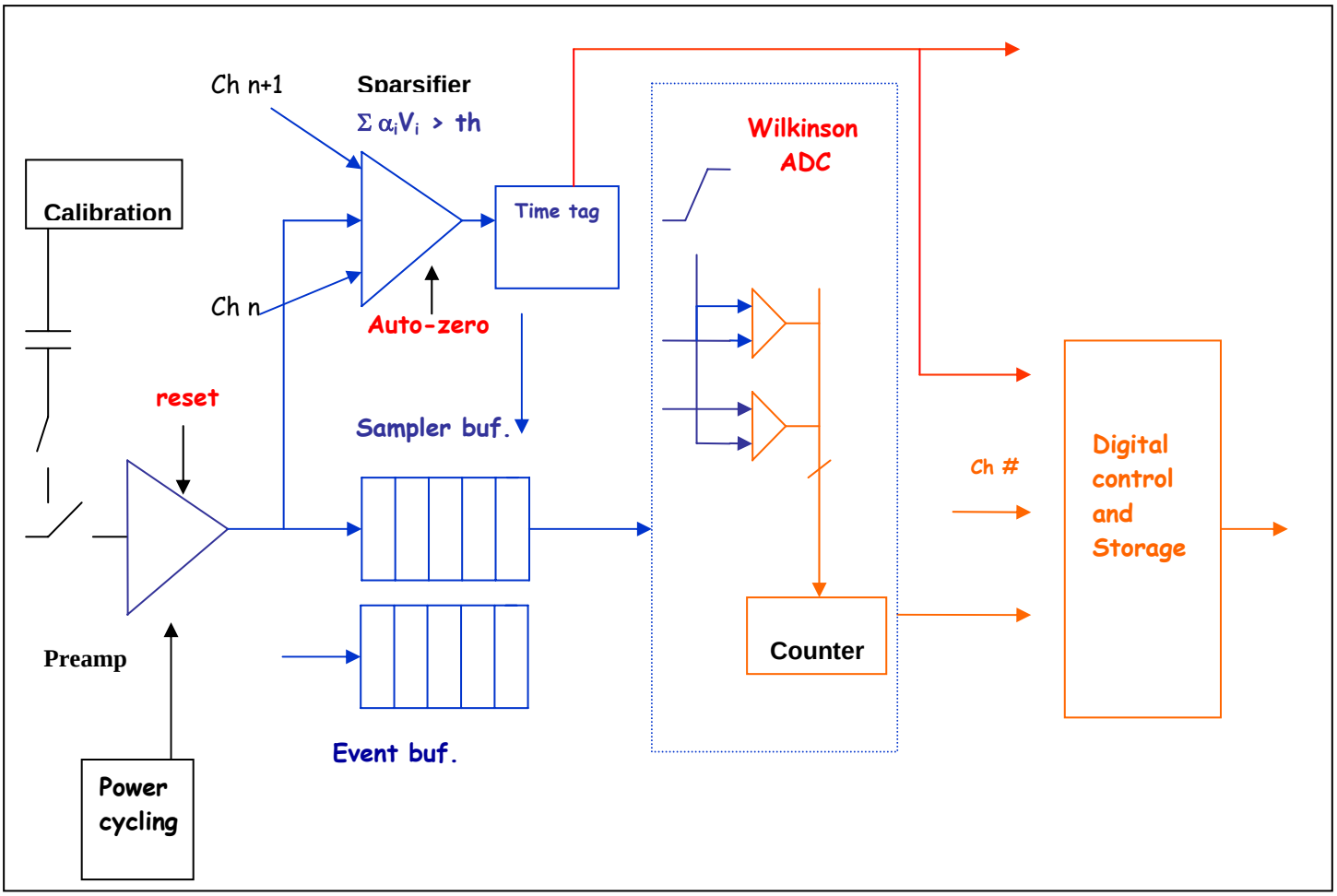


Figure 1. Readout chip block diagram

A block diagram of the Front-end chip is shown Figure 1:

A first prototype in 180nm CMOS launched in August 2004 has been evaluated and gave good results in terms of noise. As 130nm CMOS technology emerged at that time, it was decided to use it to design the next chip. The motivations were the following:

- Smaller for the same functionality,
- Faster,
- Less power consuming ,
- Dominant in industry,
- More radiation tolerant .

Some drawbacks appeared, but all of them could be overcome using an ad-hoc design:
:

- Reduced voltage swing (Electric field constant),
- Noise slightly increased (1/f),
- Leaks (gate/subthreshold channel),
- Design rules more constraining,
- Models more complex, not always up to date.

3 4-Channel chip

The 4-channel prototype chip is a demonstrator of the 130nm CMOS technology for this application. Block diagrams are shown Figure 2. This chip is a 4-channel prototype for a future Silicon strips readout multi-channel unit intended to equip the ILC Silicon strips detectors. Each channel includes a preamplifier-shaper, an 16-deep analog pipeline sampling the shaper output, a channel trigger decision on the sum of three adjacent channels (sparsifier) that freezes the pipe-line awaiting for A/D conversions. After data recording, pipelines outputs are converted in parallel using a single-ramp Wilkinson A/D converter. Four channel registers store Gray encoded digital values of the same order cell from the four pipelines.
The chip is designed using the 130nm gate length mixed mode CMOS process from UMC (United Microelectronics Corp, Taiwan, China) with the Cadence based design kit provided by Europractice (Leuven, Belgium).

4 Functional description

4.1 Preamplifiers

Each charge amplifier is a folded-cascode looped on a 133 fF integrating capacitor. Gain is therefore 5 mV/fC or 20 mV per Minimum Ionizing Particle at 25000 electrons in a 300 μm thickness Silicon detector. Input transistor capacitance is of the order of 2 pF, matched to a few centimeters long detectors.
The preamp biasing point can be tuned with the external analog voltage **v_preamp**, as well as the feedback capacitor time discharge time constant through **v_ref**, and the output voltage follower buffer to the shaper input through **v_preamp_buf**. Nominal value for **v_preamp** is -1.37 V corresponding to a current of 37 uA, 500 mV for the buffer current control **v_preamp_buf**, for a 60 μA current. Nominal value for **v_ref** is 1.1V, corresponding to a

decay time constant of 10 µs. The substrate of the input transistor is **v_sub**, whose nominal value is 1V.

The output of preamp channel_0 is available on the **out_preamp** pad. One should be careful using this output since the channel is sensitive to any external capacitance to ground in terms of rise time. As an order of magnitude, a load of 1 pF on this pad degrades the rise time by 50ns.

4.2 Shapers

Shapers use basically the same amplifier structure as the preamplifiers, over a CR-RC network whose values can tune the peaking time between 700ns to 3µs. The shapers biasing point can be tuned as well using **v_shaper**. Nominal value is -1.37V, as well as the analog control for the shaper buffer voltage control **v_buf_shaper**.
The noise performance has been simulated at 400+9e-/pF at 37uA input stage biasing and 3 µs peaking time. 375+10.5 e-/pF has been obtained in a prior version using the UMC 0.18µm CMOS process, at the same power dissipation.

4.3 Sparsifiers

A threshold is set above the sum of two or three adjacent channels (0-1 for ch#0, 0-1-2 for ch#1, 1-2-3 for ch#2, 2-3 for ch#3) to decide whether and when to trigger an acquisition. There are four independent threshold controls **zerosparse<0:3>.** The analog sum biasing point is set with an input reference current **v_sparse_IS**, the comparator with **v_sparse_IC**. Nominal values are 40 and 100 µA respectively. An analog gain of 5 is set in the summation.
For example, an effective threshold set at half a MIP corresponds to a threshold control on **zerosparse<0:3>** of 5 x 20mV/2 = 50 mV.
Upon a sum signal exceeding the threshold, the pipeline clock is stopped after 2, 4, 6, or 8 cycles, depending on the selection **pedestal<0:1>,** in order to sample the complete shaper output. The sparsifier auto-zeroes the shaper output on activation of the **in_pipeline** control. The offset value is held in a capacitor and subtracted for the data taking stage, not longer than 2 ms. For longer data taking durations, this control should be refreshed periodically. Two sparsifier outputs are available on **sparse<0:1>.** The sum from ch#1 is available on **sumsparse**.

4.4 Analog Pipeline

A 16-deep analog memory is running continuously as a circular buffer during the data taking stage defined by the activation of both **cmdW_N** and **cmdW_P**. In this write mode, samples of the shapers outputs are taken continuously at the write clock cycle rate. Write clock is applied on **ck_12MHz**. Frequencies between 2 up to 24MHz can be used. Upon a sparsifier decision, the write clock is stopped as described above, the history is stored in the pipeline including the shaper output pedestal, provided the control **pedestal<0:1>** has been properly set, with respect to the write clock frequency, the shaper peaking time, and the pipeline depth (16). The dynamic range of the full analog chain is 40MIPs. The analog pipeline outputs are

available on **outpipe<0:3>. In_pipeline** sets a logic "one" in the shift register digital pipeline control, to be stored on a read clock (**ck_12MHz**) leading edge before chip is used. A 30 ns minimum duration is required. (see Figure 8).

4.5 ADC

Once data are stored in the analog pipeline waiting for A/D conversion, a read pipeline control applied on **cmdR_N** and **cmdR_P** connects the last pipelines cells of each channel to a 12-bit ADC.
As soon as **startconv** is activated for at least 200ns, a conversion is initiated for a maximum duration of 40μs, at an ADC clock frequency up to 100MHz applied on the **ck_48MHz** input. **startconv** is active low. Four data words are ready in the output registers.
The 12-bit data words are multiplexed onto an 8-bit output bus, **out<0:7>**. Bits **csreg<0:1>** selects the channel to be read, **lh** selects either data bits <0:7>, or data bits<4:11>. Then, on activation of **ck_read_pipeline** for at least 20ns, the pipelines are shifted by one cell for the next conversion, followed by **startconv**.
This process should be repeated 16 times to get all the pipelines content converted. Therefore, a full read sequence is achieved in 4 (channels) x 16 (samples) x 2 (bytes) = 128 read clock cycles at up to 100 MHz taking 16 x 40μs + 1.28μs = 161.28μs. The ADC calibration is performed with two analog controls: **v_slope_ramp** and **v_offset_ramp** tuning the zero and full scale of the converter. The reference ramp is output on **ramp.**

4.6 Misc

A general reset is available on **rst** and should be activated for 50 ns at less before data taking.
The bias point of the ramp generator can be tuned using **v_buf_ramp,** nominal value is –1.4V.
A independent reset of the pipeline capacitors is also available on **rst_pipeline.** It is to be activated for 50 ns before any data taking.
A "manual" DC offset of the shapers can be used on **DC_shaper**, if the auto-zero is not to be used.
Pipeline clock phases can be tuned in length and rise time with two controls **v_delay_top** and **v_delay_bottom**. Nominal values are and –1.42V and –680mV respectively.
All digital controls are active high, unless specified (**startconv**).
Eleven 6-bits DACs control the on-chip analog voltages and current sources

4.7 Voltage supplies

Two main supplies are used: analog 3.3V and digital 1.2V, referred to two separate grounds tied externally to the same potential. Chip's substrate is tied to ground.

4.8 Package and die size

The chip is not packaged. Die size: 3240 x 1525 μm2.

The corresponding functional diagram is presented Figure 2.

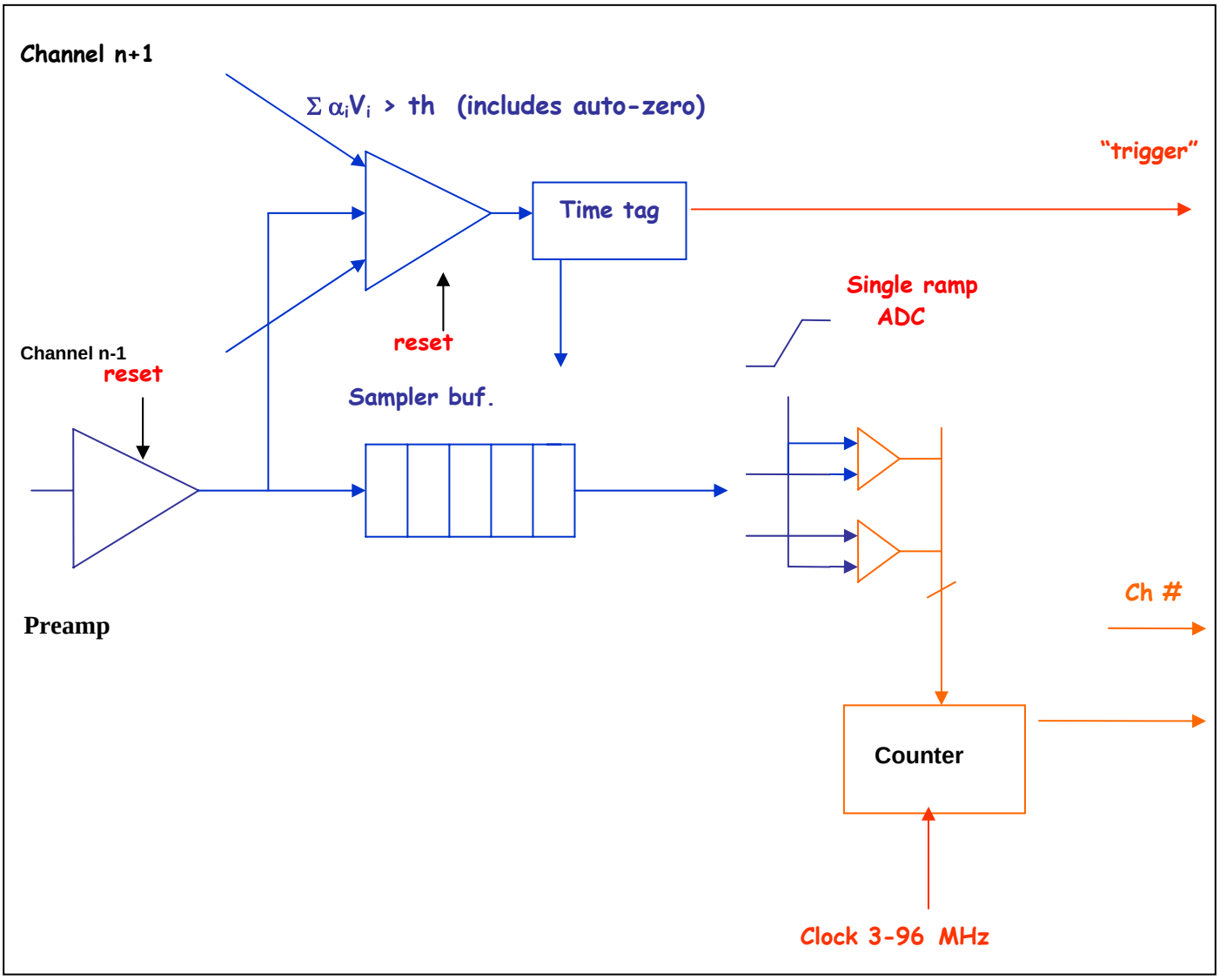


Figure 2. 4-Channel chip block diagram

The chip was launched in May 2006, received in September 2006. Most of its functions and critical parameters have been presently tested, but some functionalities are still under tests. The sparsifying mechanism could not be tested due to a bad assignment of one of the multiplexed I/Os. The layout and photo are presented in Figure 4.

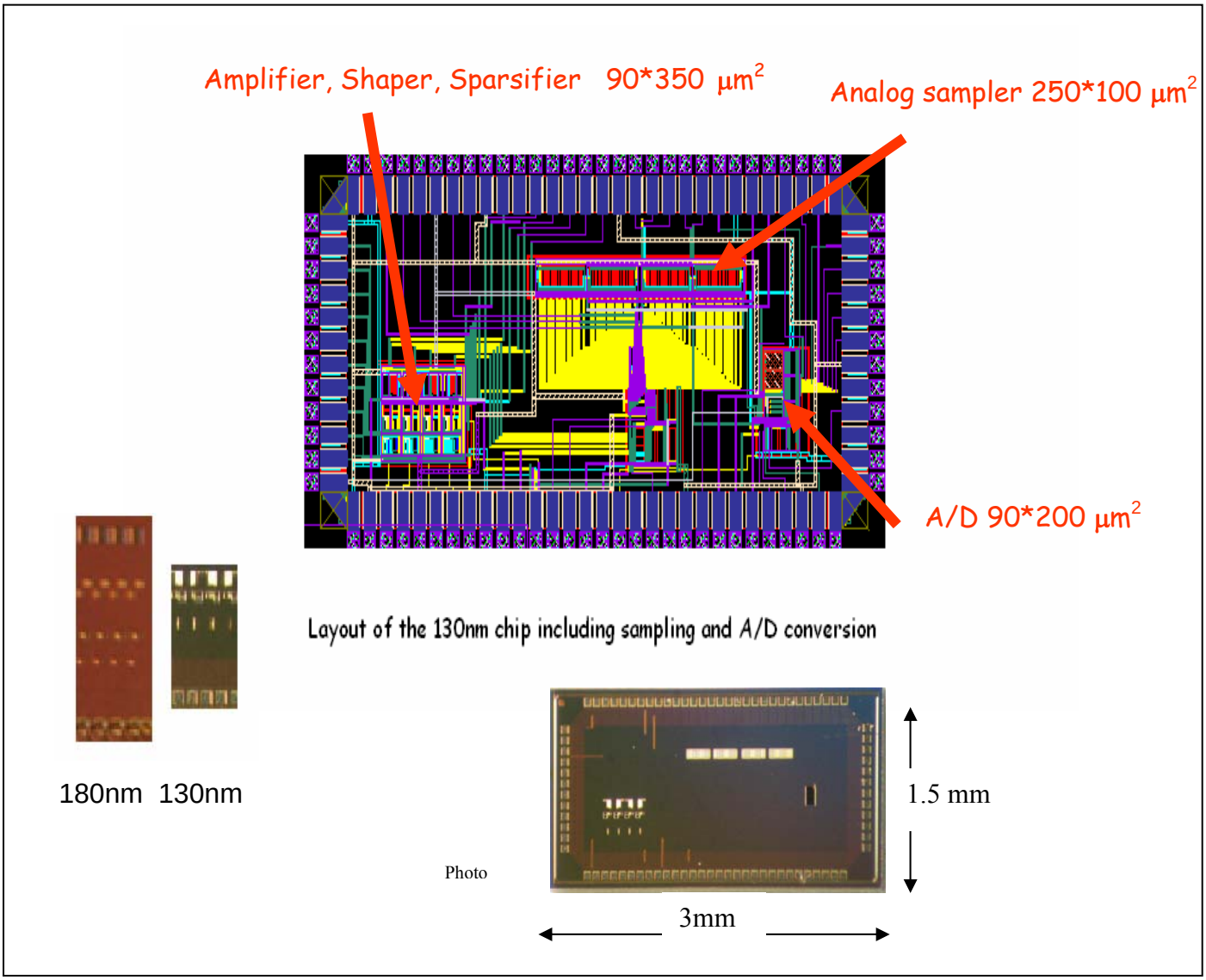


Figure 3. 4-Channel chip Layout and Photo.

5 Results

The chip has been tested first on a laboratory test bench with analogue pulse generators and a dedicated electronics card where it has been wire-bonded. All functions were checked, at the exception of the sparsifier due to a faulty I/O pads multiplexing of the pipeline control register with the auto-zero control. However, the storage of analog data in the pipeline was possible using the analog zero input of the sparsifier, allowing also the tests of the rest of the chain.
Figure 4 shows gain and linearity measurements, together with the preamplifier and shaper output waveforms. Figure 5 compares noise performance in 180 and 130nm CMOS technology.
Figure 6 shows the ADCs output for a typical shaper pulse. AD unit is 250 μV. Actually, 9-10 bits are obtained on an 1V input range, for 12 implemented. This measurement is presently under improvement using more efficient decoupling and grounding scheme on the test card.
Figure 8 shows the shaper pulse reconstructed from 120 GeV pions events taken at a beam test at CERN in October 2007. 22 events exceeding a given threshold were selected, scaled, and averaged. Figure 9 shows the Signal to Noise ratio obtained at the same beam test.

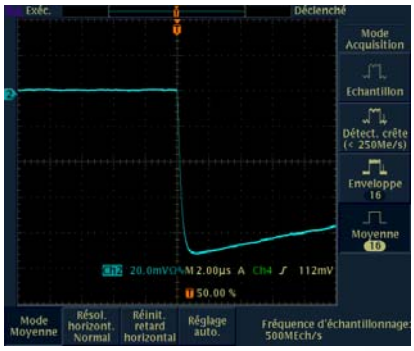
6 Power and Silicon area

Power and area on Silicon are 500 μW, and 100 x 500 μ^2 per channel respectively. There is no package, the chip being intended to be wire-bonded straight on PCB, or Silicon.

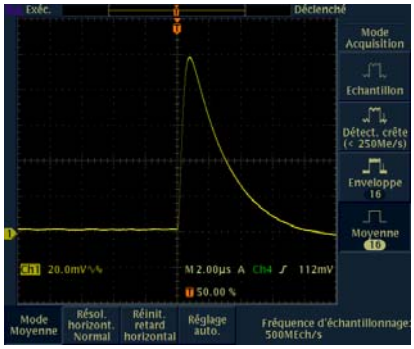
7 Conclusion

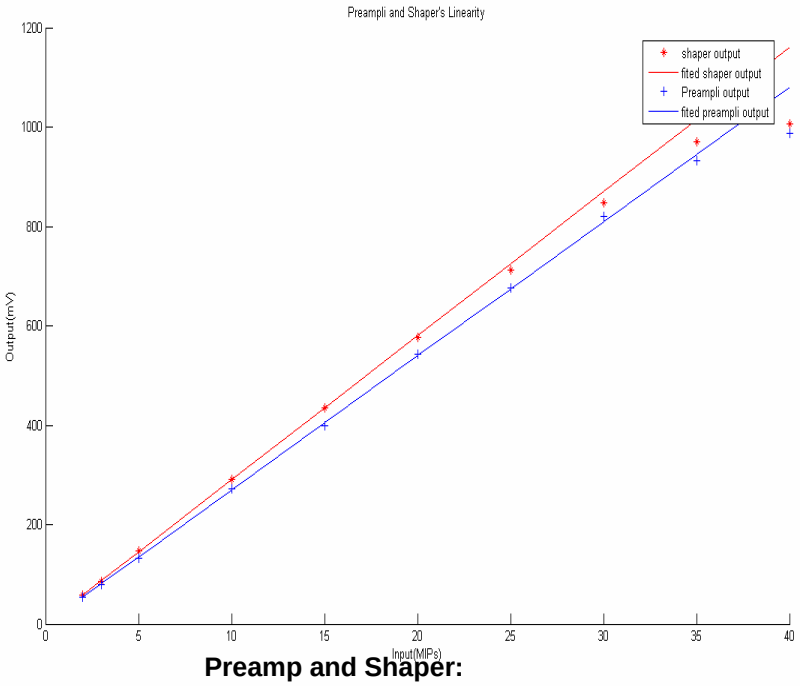
As presented in the previous sections, the 130nm CMOS 4-channel chip milestone has been successfully passed, at the exception of the self-triggering functionality. Thus, all the other implemented functions (preamplifier, shaper, pipeline, ADC) will be used as building blocks for the next milestone, a 128-channel chip aiming at reading a full Silicon strips detector equipped with 16 such chips.

The self-triggering function will also be taken as is from the first milestone, since the simulations showed a correct behavior. It will be therefore fully tested as one of the first items of the second milestone objectives.



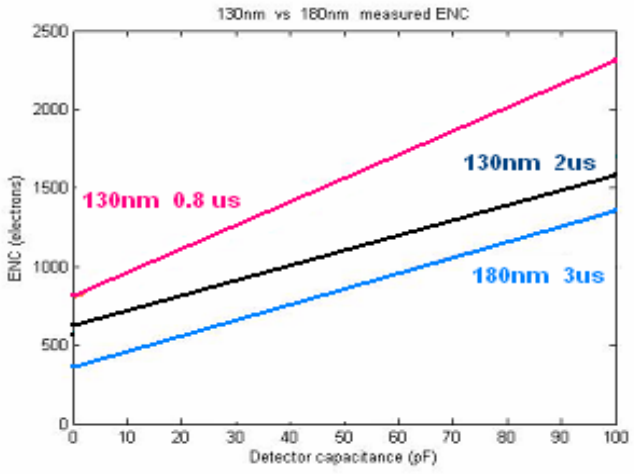
Shaper output





Preamp and Shaper:

Gain	**29mV/MIP**
Dynamic range	**20 MIPs @ 1%** **30 MIPs @ 5%**
Peaking time	**0.8-2.5µs / 0.5-3µs expected**



Power (Preamp+ Shaper) = 245 µW

Noise: 130nm @ 0.8 µs : 850 + 14 e-/pF 245 µW (150+95)
130nm @ 2 µs : 625 + 9 e-/pF
180nm @ 3 µs : 375 + 10.5 e-/pF 210 µW (70+140)

Figure 4 and 5. Gain and Linearity measurements. Noise: 180 and 130nm compared

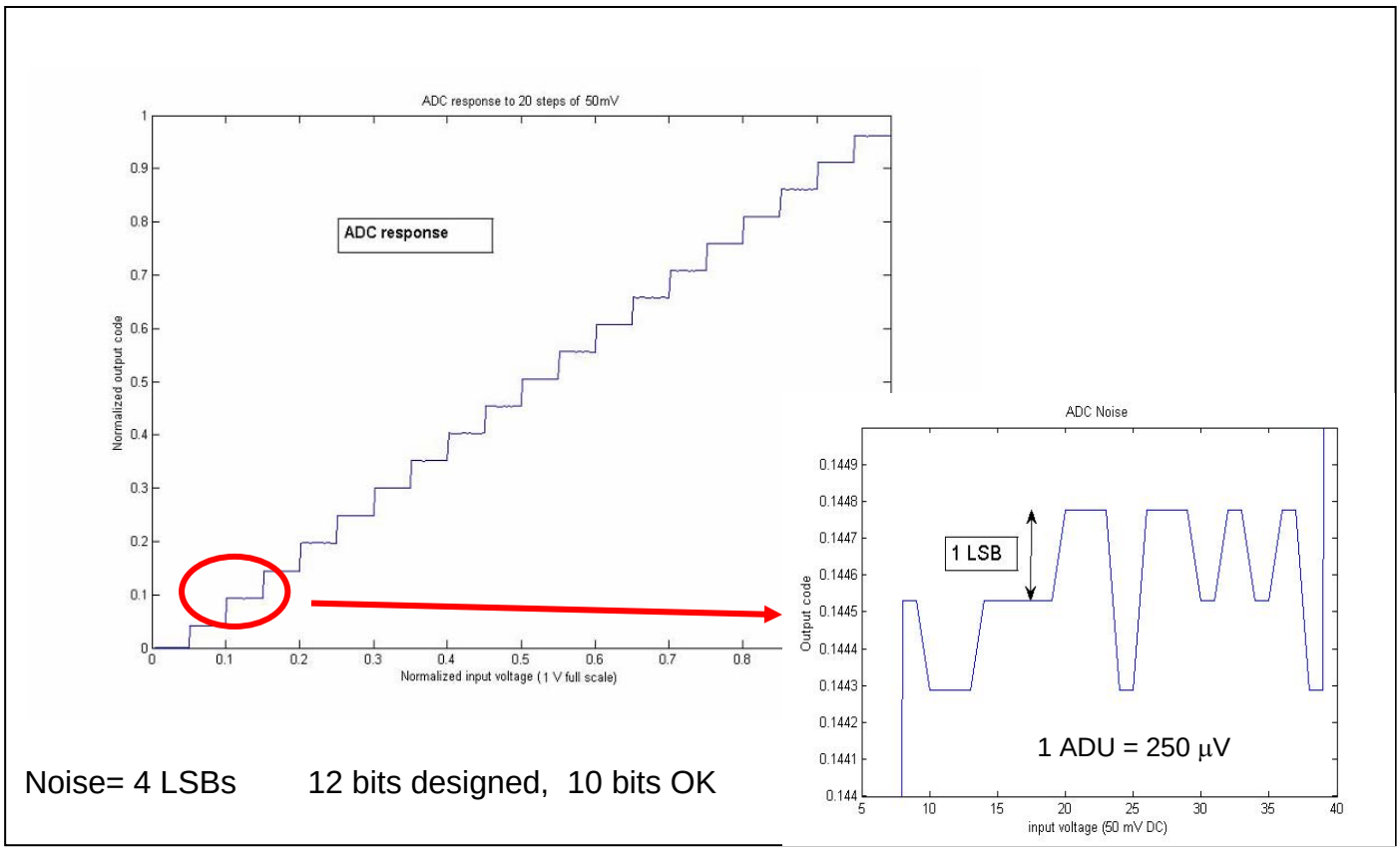


Figure 6. Digitized shaper output waveform.

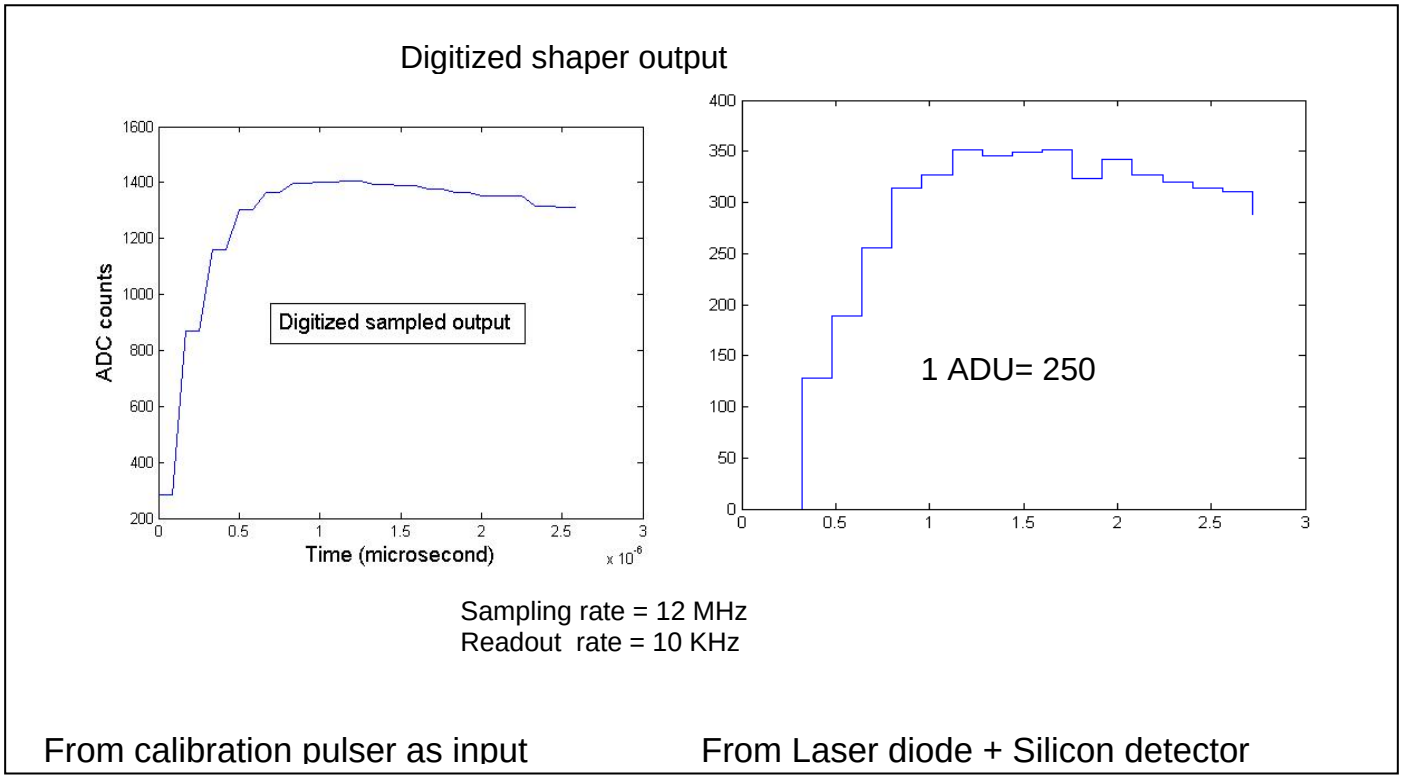
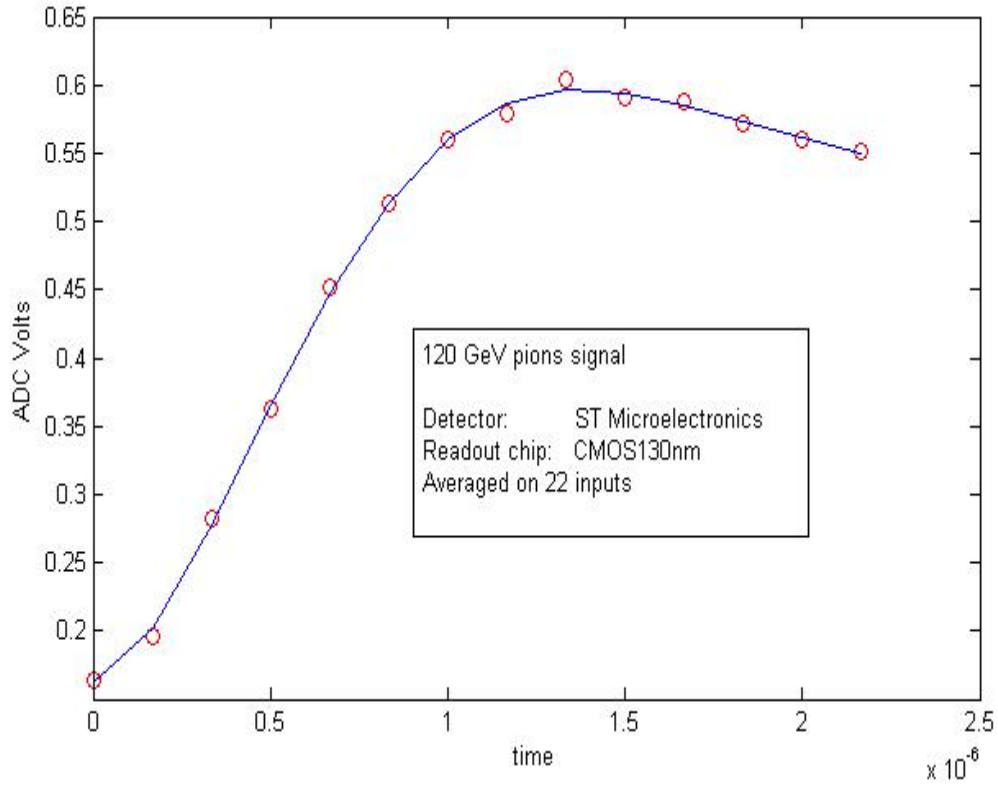


Figure 7. ADC performance



- **Averaged response of 120 GeV pions through 500 μm thick Silicon detector**
- **Actual pedestal spread: 100mV under investigation (decouplings on PCB)**
- **Pedestal subtracted off-line.**

Figure 8. Reconstructed shaper pulse. (120 GeV pions)

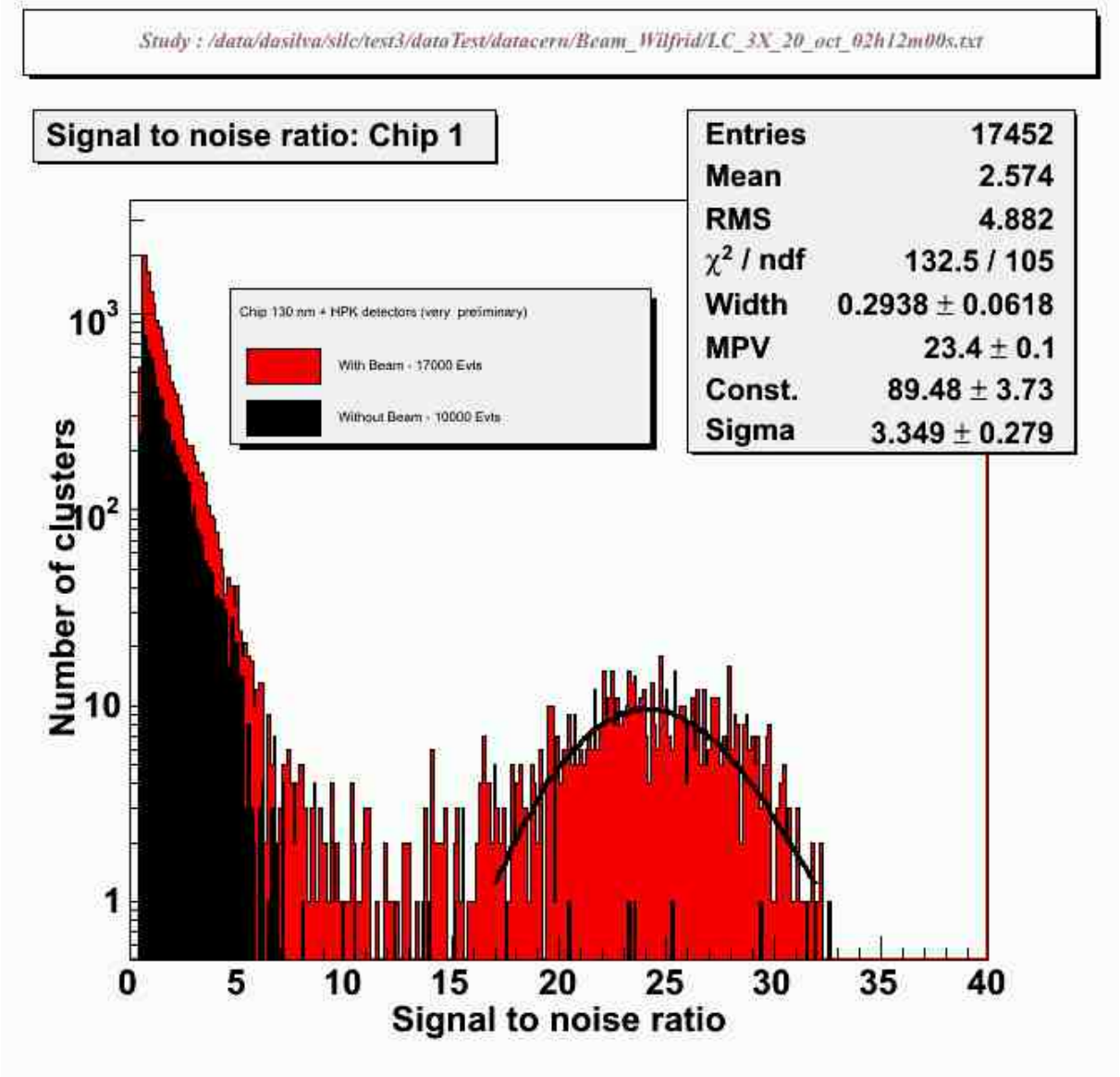


Figure 9. Signal to Noise ratio (120 GeV pions)

8 Pin-out

N° pin	Name	Type		Note	V mes
1	WVVSS	Supply	-1,65V		
2	IN1	Input			
3	IN2	Input			
4	GND1V65	Supply		GND	
5	IN3	Input			
6	IN4	Input			
7	V_SUB	Supply	1V	Polar Substrat Plus	
8	WVVDD	Supply	-0,45V		
9	PEDESTAL0	Logic_in			
10	PEDESTAL1	Logic_in			
11	V_DELAY_TOP	Bias		Découplage à VSS	-1,4
12	V_DELAY_BOTTOM	Bias		Découplage à VSS	-0,8
13	WVVASXR	Supply	-1,65V		
14	WVVADXL	Supply	+1,65V		
15	IN_PIPELINE	Logic_in			
16	CLK_READ_PIPELINE	Logic_in			
17	RST	Logic_in			
18	WVVSS1	Supply	-1,65V		
19	CLK_12MHZ	Logic_in			
20	WVVDD1	Supply	-0,45V		
21	WVVASXR1	Supply	-1,65V		
22	STARTCONV	Logic_in		Debut de séquence de conversion	
23	CSREG0	Logic_in		Changer de voie en lecture	
24	CSREG1	Logic_in		Changer de voie en lecture	
25	WVDD2	Supply	-0,45V		
26	V_OFFSET_RAMP	Bias	Voltage (-0.65V->-0.4V)	Découplage à VSS	-0,6
27	V_SLOPE_RAMP	Bias	Current 166nA	Découplage à VSS	-1,257
28	V_BUF_RAMP	Bias	Between-1.4 et -1.35	Découplage à VSS	-1,4
29	OUT_RAMP	Output			
30	WVVAS	Supply	-1,65V		
31	WVVAD	Supply	+1,65V		
32	WVVADXL1	Supply	+1,65V		
33	WVVSS2	Supply	-1,65V		
34	CLK_48MHZ	Logic_in		20ns	
35	WVVDD3	Supply	-0,45V		
36	WVVASXR2	Supply	-1,65V		
37	DATA7				
38	DATA6				
39	DATA5				
40	DATA4				
41	DATA3				
42	WVV0IO	Supply	-1,65V		
43	WVV3IO	Supply	+1,65V		
44	DATA2				
45	DATA1				
46	DATA0				
47	OUTPIPE1				

48	OUTPIPE2				
49	WVVSS3	Supply	-1,65V		
50	LH	Logic_in			
51	CMDR_N	Logic_in		niveau logic -1.65/+1.65	
52	CMDR_P	Logic_in		niveau logic -1.65/+1.65	
53	CMDW_N	Logic_in		niveau logic -1.65/+1.65	
54	CMDW_P	Logic_in		niveau logic -1.65/+1.65	
55	RST_PIPELINE	Logic_in		niveau logic -1.65/+1.65	
56	WVVDD4	Supply	-0,45V		
57	WVVADXL2	Supply	+1,65V		
58	SPARSE2	Output_analog			
59	SPARSE1	Output_analog			
60	ZERO_SPARSE2	Input_analog			
61	ZERO_SPARSE3	Input_analog			
62	DC_SHAPER	Input_analog			
63	SUMSPARSE	Output_analog			
64	V_SPARSEIS	Bias	Current 40uA	Découplage à VSS	-0.810
65	WVVSS4	Supply	-1,65V		
66	OUT_SHAPE3	Output_analog			
67	OUT_SHAPE2	Output_analog			
68	GND1V651	Supply		GND	
69	OUT_SHAPE1	Output_analog			
70	OUT_SHAPE0	Output_analog			
71	OUT_PREAMP	Output_analog			
72	WVVDD5	Supply	-0.45V		
73	V_SPARSEIC	Bias	Current 100uA	**Découplage à VDD**	**-0.2**
74	ZERO_SPARSE0	Input_analog			
75	ZERO_SPARSE1	Input_analog			
76	V_POLE	Bias		Découplage à VSS	1,2
77	V_ZERO	Bias		Découplage à VSS	0,8
78	V_BUF_SHAP	Bias	Current 3.548uA	Découplage à VSS	-1,37
79	V_SHAP	Bias	Current 3.548uA	Découplage à VSS	-1,37
80	V_PREAMP_BUF	Bias	Current 20uA	**Découplage à VDD**	0,8
81	V_PREAMP	Bias	Current 3.548uA	Découplage à VSS	-1,37
82	V_REF	Bias		Découplage à GND	-1,1
83	WVVASXR3	Supply	-1,65V		
84	XL3	Supply	+1,65V		

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