DAQ Status Report

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December 18, 2007

Abstract

The aim of the JRA3 task is to provide infrastructure for the usage of novel readout schemes for a calorimeter detector of experiments at the ILC. The instrumentation and readout should be suitable for operation both in testbeam as well as the final experiment. The current DAQ proposal embodies a system consisting of a Detector Interface close to the actual detector slabs, local Link/Data Aggregators inside the detector volumes and Off-Detector Receivers located in the counting rooms. Software built inside a modular framework controls the DAQ system.

This document contains descriptions of the functionality and current statues of the above items

With the development of individual components under way, the focus of the DAQ working group is on system integration, leading to a full DAQ test. After that, the aim is to read out the EUDET module in a particle beam test.

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1 JRA3 DAQ Task: Introduction and Objectives

The aim of the JRA3 task is to provide infrastructure for the usage of novel readout schemes for a calorimeter detector of experiments at the ILC. The instrumentation and readout should be suitable for operation both in testbeam as well as the final experiment.

1.1 JRA3 DAQ Objectives

The data acquisition system (DAQ) reads out the front-end electronics. The focus lies on constructing a system from commercial off-the-shelf components, using commodity technology where possible.

The design of the DAQ should be scalable. The system should be designed such that upgrading the relatively small system for testbeam use to a full-scale detector DAQ does not introduce bottlenecks.

1.2 A DAQ for EUDET

The first goal for a new DAQ development is the readout of the EUDET module in the beam test scheduled for 2009. In the beamtest, the physics performance of a full stack of the ECAL detector will be assessed, using newly developed front-end readout electronics. The newly developed DAQ will be used for the readout of the module, which comprises a stack of 29 Tungsten slabs, of which 15 have instrumentation fitted on both faces.

Obviously, the requirements of a DAQ for a beam test experiment are quite different compared to those for a DAQ of the final experiment. The design of the DAQ must allow it to operate in both environments. Reading out the modules in the beam test will be a major stepping stone in the development of a DAQ for a detector at the ILC.

2 Calorimeter DAQ Architecture

Ideally, a calorimeter detector consists of dense material with a homogeneous mass distribution. The insertion of layers of detectors and associated readout electronics will worsen the detector performance; therefore the aim is to keep the total thickness of a fully instrumented 21 mm slab under 60 mm.

Because of the dense packing of readout electronics in the detector volume, the power consumption should be constrained to 25 μW per channel. With an average channel size of 5x5 mm, the total dissipation in the calorimeter barrel will be below 2 kW. At this level, the heat buildup in the detector volume is still manageable.

2.1 DAQ Architecture

Very Front-End (VFE) chips are embedded in slabs residing inside the active detector volume. A slab is serviced by a unit sitting at the slab edge, the Detector InterFace board (DIF). The DIFs read VFE data, assert control signals and distribute clock signals and configuration data to the VFE chips.

One DIF services a single detector slab, hosting 130 to 140 VFE chips, depending on the slab length. As the barrel calorimeter counts over 6000 slabs, servicing DIFs individually from the outside of the detector is not feasible. A separate unit is introduced to reduce the link count of the DIF to off-detector DAQ interface.

Links carrying clock, data and controls signals connect the DIFs to the Link/Data Aggregators (LDAs). The data of many DIF links is multiplexed onto a few high-bandwidth links. In the reverse direction, clock signals and control commands are sent to the LDA to be distributed towards the DIFs.
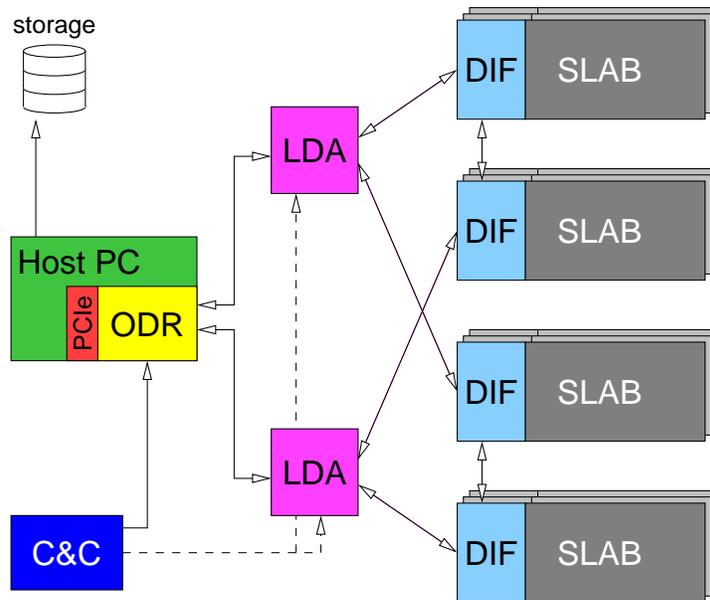

Figure 1: Schematic overview of the DAQ system, see text.

The LDAs are connected to an Off-Detector Receiver (ODR), hosted by a commodity PC. At this stage, data can be stored locally or sent over a high performance switched network.

A separate Clock and Controls (CC) unit deals with the distribution of the collider clock, and is used for the distribution of low-latency detector controls.

A schematic overview of the DAQ system is depicted in Fig. 1.

3

2.2 DAQ Requirements

In the scheme described above, the DIF boards are very much integrated with the de-tector. The LDA, ODR and CC units are transparent with respect to the detector type, readout chips or data format. In principle, they could be used for any type of detector.

To reduce the data volume, aggressive zero-suppression circuitry is integrated in the VFE chips. Input channels are sampled only when a single channel exceeds a preset threshold level, reducing the data volume by a factor $\sim 10^3$. The need for external trigger signals is omitted, except for detector calibration purposes.
The repercussion for the DAQ is that it is waiting for data rather than requesting it: VFE data is 'pushed' through the DAQ system. At the time of the bunch crossings, the back-end of the DAQ is unaware how much data is produced where in the detector.
During calibration, trigger signals are provided to the VFE chips to gather data as quickly as possible and speed up the calibration process.

3 DAQ Components and Interfaces

The boundary between the front-end electronics and the DAQ is defined at the end of the slabs which host the VFE chips and are integrated in the detector. Below, the DAQ components are described in some more detail, and their current status is presented.

3.1 DIF: Detector Interface

As the DIF is directly connected to the end of the detector slab, hence its hardware is very much detector specific. The DIF provides clock and controls signals to the slab, and controls the loading of configuration data into the VFE chips.

DIF - Slab Interface

To ensure a seamless connection between the DAQ and the detector instrumentation, the interface between the detector slab and the DIF needs to be accurately defined and described.

The details on how to operate the VFE chips data readout path, the control signals and the configuration registers are very much determining the interface layout.
Currently, contacts are established by application of conductive glue to facing PCB con-tact pads. Connection densities are capped by the minimum glue drop size, severely limiting the number of connections between the slab and the DIF.

A working group is established to compile a list of signals for the slab-DIF interface. The current list includes redundancy paths for the readout token mechanisms and allows for two separate strings of daisy-chained VFE chips, increasing the slab readout speed.

DIF implementation

The DIF functionality is to be implemented in an FPGA. The larger part of the firmware running on the FPGA is foreseen to be common to all detectors. This includes the interface with the link between the LDA and DIF, the interpretation of the controls and commands, the data transfer and diagnostics functions.

For flexibility, the part of the firmware actually providing specific controls signals can be 'personalised' with respect to the VFE chip and detector type.
A USB port is provided for stand-alone operation of the DIFs, eliminating the need for a DAQ system when performing lab measurements or debugging.

Since the DIF hardware is specific to the detector type, a common hardware solution is probably not feasible. Through the DIF working group, an effort will be made to standardise the hardware requirements, such that compatibility is ensured and DIFs for various detectors benefit from common DIF firmware developments.

DIF-LDA and DIF-DIF Links

At the other end, the DIF is connected to the LDA with a synchronous link, used for shipping data off the detector, and reception of VFE configuration data as well as controls commands.

To protect the DAQ against failure of LDA - DIF links, or an entire LDA, even and odd DIFs are connected to separate LDAs. A DIF is connected to its neighbour, in the case of a LDA (link) failure, the DIF-DIF connection substitutes the lost communications path. Both connection types are indicated by arrows in Fig. 1.

Although the LDA - DIF link bandwidth requirement depends on implementation details of the VFE chips, 50 Mbits/s is established as the minimum requirement, leaving ample headroom for redundancy purposes as discussed above. The link speed can easily be achieved by standard FPGAs on affordable copper media.
Data transfers are to be 8b/10b encoded for maintaining a DC-balanced link. To detect possible errors in the transmitted data, parity checking is foreseen for 2-Byte command transfers, and additional checksumming is to be performed on long data transfers containing configuration data or event data.
Using commercially available developments for the hardware implementation, HDMI cables and connectors are chosen for the DIF links. HDMI components are widely available, and offer excellent specifications at a price point far below custom solutions.

DIF Current Status

For studies of RPC detector performance and data transmission along slab-sized PCB panels, specific FPGA based DIF hardware and firmware has been developed, as pic-
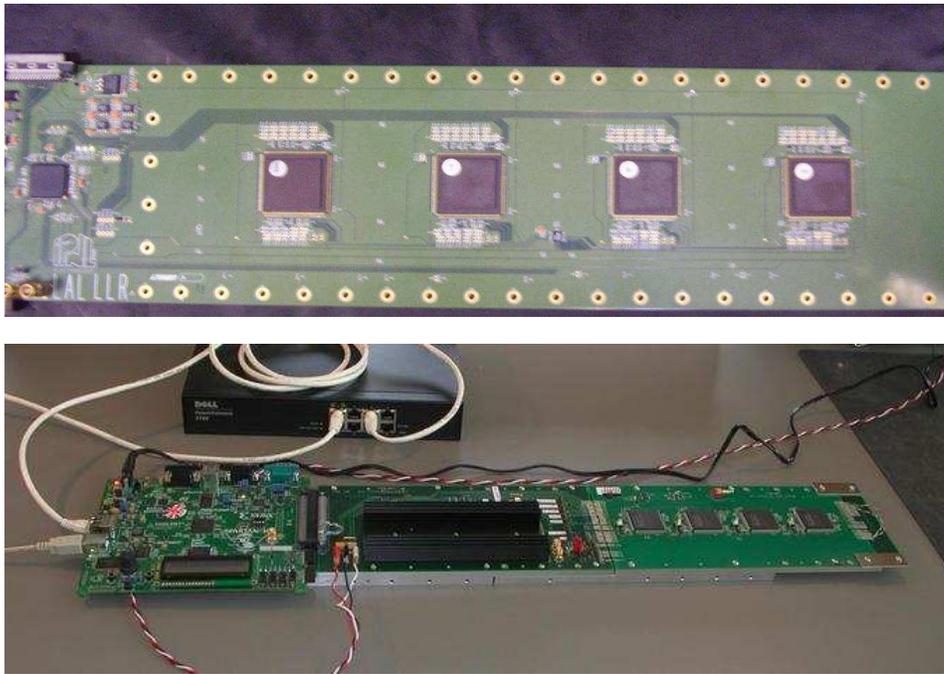
Figure 2: DIF developments for specific tasks: a slab with DIF designed as a part of a RPC detector (top), and a DIF-slab setup for signal integrity and data transport studies (bottom). In both photos, the DIF is located at the left side, servicing chips right of the DIF.

tured in Fig. 2.

Aside from these DIFs, which are intended for very specific use, design effort is ongoing to develop a general-purpose DIF for the readout of the EUDET module.

Probably most of the DIF firmware is associated with the communication between the DIF and the LDA, or between DIFs in case of LDA link failure (see Fig. 1).

Firstly, commands and data transfers coming in from the LDA have to be checked, acknowledged and translated into concrete actions on signal lines running towards the VFE chips. Currently, specifications for the LDA-DIF communications path are being defined.

The second most demanding task is the readout, repackaging and shipping of event data coming off the VFE chips. Both experimental DIFs are capable of reading and buffering VFE data. In the final DIF, multiple strings of daisy chained VFE chips are read out simultaneously, which requires more capacity for data buffering and digestion.

A preliminary DIF functional block diagram for guiding the firmware development has been designed and is continuously being refined. A very coarse representation is included in Fig. 3.
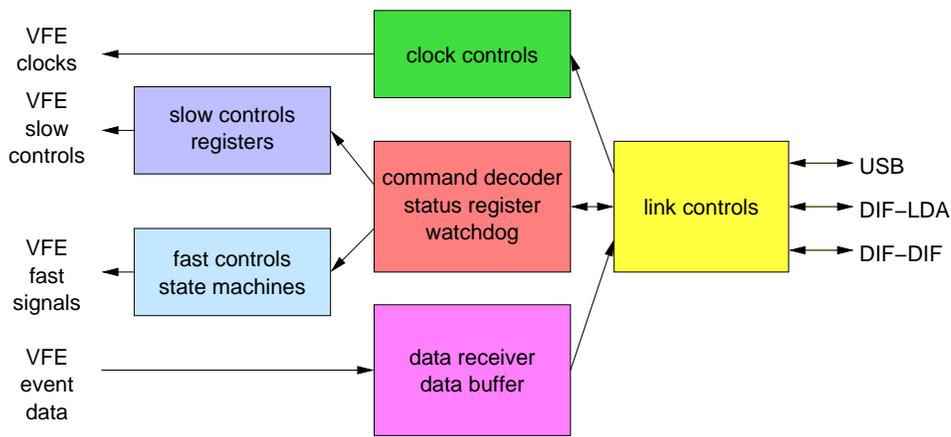
Figure 3: Functional block diagram of the DIF.

3.2 LDA: Link Data Aggregator

To reduce the thousands of DIF output links to a more manageable figure, the LDA multiplexes many DIF links onto a single link with a bandwidth in the 1 Gbits/s range.

Clock and controls signals are to be sent towards the LDAs over the link simultaneously. The LDA decodes and distributes the appropriate signals to the DIFs.
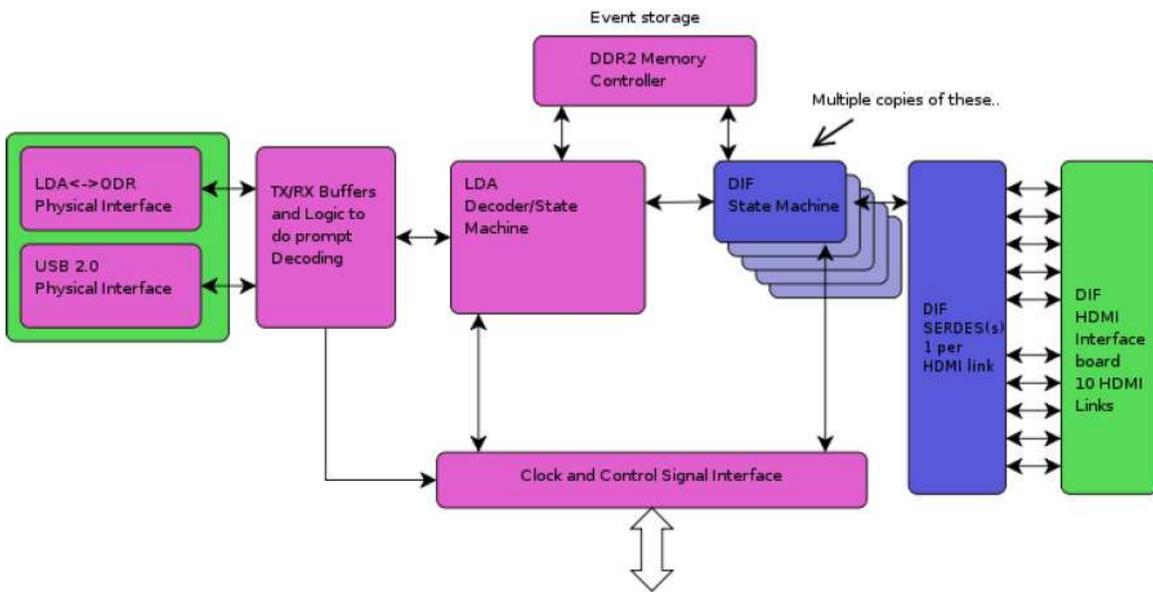

Figure 4: Functional block diagram of the LDA.

To avoid unnecessary complexity in the LDAs, they are designed to forward rather than process commands towards the DIFs, and are repackaging data from the DIF links to-

wards the ODR, unaware of the data content. The LDA is implemented as custom firmware running on commercially available FPGA based hardware.

A functional block diagram of the LDA firmware is depicted in Fig. 4. A commercially available hardware development platform has been targeted (see Fig. 5). The development board offers many I/O connections for custom add-ons. For the serial link towards the ODR, this allows two alternatives to be studied: a Gbit Ethernet, and TLK2501 chipset based implementation.
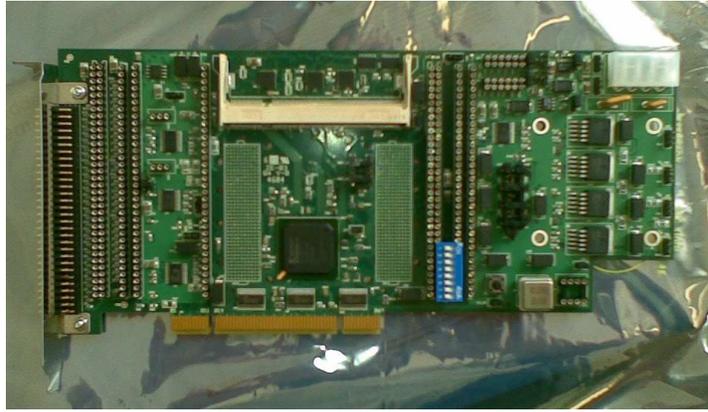

Figure 5: Selected hardware development platform for the LDA prototype.

3.3 C&C: Clock and Controls

For the distribution of the MHz-range ILC bunch-crossing clock and machine related commands, a separate C&C unit is envisaged. The main task is to provide the DAQ with an overall clock signal, even if the primary ILC clock is unavailable.
If necessary, commands requiring a latency less than a ILC clock cycle will be distributed by the C&C directly towards the LDA. It has to be investigated whether the part of the C&C not involved with the provision of the clock can be integrated with the ODR hardware.

3.4 ODR: Off-Detector Receiver and Optical Switching

ODR units connect to the links to/from the LDAs. Once again, commercial hardware and customised firmware is used for the implementation of the ODR prototypes.

ODR Implementation

A development board from PLDA is used for the ODR prototyping. It hosts a large FPGA (Xilinx Virtex4 FX-100), and is intended to be used in a standard PC, using a multi-Gbits/s, multi-lane capable PCI-express bus for communicating with the host

PC. Fig. 6 contains a picture of the board.

Figure 6: The PLDA V4FX100 FPGA hardware development platform for the ODR.

The board features four dedicated I/O sockets for speeds up to 2.5 Gbits/s, intended both for driving optical or copper media. More I/O channels are available through high-speed connectors. Additionally, on-board DDR2-SDRAM can be used for event data buffering.
The firmware is customised for the required functionality, and is largely composed of universal code blocks for addressing the memory, controlling the fast links and PCIe bus.

ODR Performance

The lines in the plot in Fig. 7 represent the data transfer speeds for different functional configurations of the ODR prototype board. In the legend, IDG refers to Internal Data Generation, as opposed to Network Data Generation, NDG. The performance of the Direct Memory Access (DMA) data transfer across the PCIe bus has been plotted separately. 'Net' refers to the situation where the received data is retransmitted onto a fast network. The disk write/no disk indicates whether or not the data is copied onto a five-disk RAID array.

As can be seen from the plot, the DMA transfer is by far the fastest process and acts as a performance maximum. When data is generated externally, the performance is still close to this maximum. However, as soon as the data is generated internally, or has to be written to disk, the data rates suffer a large reduction.
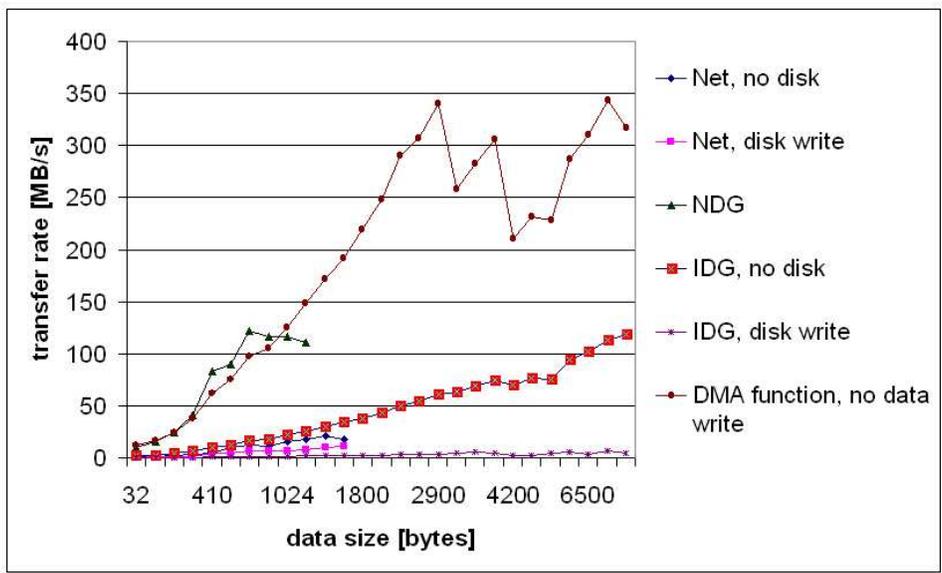
Figure 7: Data transfer rates for various configurations of the ODR board, see text.

The plot implies that the tools for performance assessment are in place; increasing the performance by optimising the firmware is now the first objective.

Optical Switching

Figure 8: Photograph of the optical switch.

Optical switches are a key component in high-performance, fibre-based networks. For performance studies of networks with multiple data sources and destinations, an optical switch, pictured in Fig. 8, has been purchased. Switching times are established at 36 ± 2 ms, with an additional delay of >100 ms for command processing.

3.5 Software

As is the aim with the hardware implementation, the DAQ software effort aims for a modular, easily upgradable system, built from components or using frameworks readily

available in (HEP) research or industry.

After compilation of a list of requirements, three alternatives for the DAQ software implementation emerged: EPICS, ACE and DOOCS. Of these three, DOOCS (Distributed Object Oriented Control System) seems the most appealing. It has been designed for HERA and the Tesla Test Facility. It is written in C++, and based around Object-Oriented APIs, providing interfaces with multiple protocols and applications such as LabView on the client side.

A first objective is to integrate the ODR into the DOOCS software environment. This would facilitate sending commands towards the LDA, and prepares for the reception of event data.

4 JRA3 DAQ: Current Status and Outlook

Within the JRA3 task for the provision of a DAQ system for a calorimeter for experiments at the ILC, work is ongoing in many areas. An overall DAQ architecture is established, and efforts for development of hardware, firmware and software are ongoing. Where possible, commercially available components are used.

Division of Work

Area of work	Participating Institutes
Slab interface	Imperial College London, University of Cambridge
DIF Hardware + Firmware	Cambridge
LDA-DIF link	University of Manchester, Cambridge
LDA Hardware + Firmware	Manchester
LDA-ODR link	Manchester, University College London
ODR Hardware, Firmware	Royal Holloway, UCL
ODR - PC interface	RH
DAQ Software	RH, UCL

Table 1: JRA3 DAQ task division.

Within the JRA3 task, several UK institutes have taken up the responsibility for the DAQ system. In Table 1, participating institutes and their areas of work are listed.

Future Plans and Milestones

With the development of DAQ components under way, the focus for the near future is the DAQ system integration. For 2008, a test aiming at a full DAQ system is foreseen. After that, the next milestone is planned for the second half of 2009, where the EUDET module is planned to be incorporated in a particle beam test, to study its performance, using the newly developed DAQ for the readout

Acknowledgement