JRA-1 Milestone
SDC Prototype 2 ready

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Abstract

SDC Prototype 2[1], the chip featuring the zero suppression logic and the output memories needed for the final pixel sensors equipping the EUDET beam telescope, was designed and fabricated in 2007. Back from foundry last Octobre, it was successfuly characterised in Novembre-Decembre 2007, showing that the expected performances in terms of data flow reduction are within reach.

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[1]alias SUZE-01, acronyme of *SUppression de ZEro No 1.*

1 Introduction

The EUDET beam telescope will be equipped with fast and high resolution pixel sensors allowing to provide high density tracking adapted to intense particle beams. An essential componant of the sensor architecture is a fast zero suppression micro-circuit integrated on the sensor substrate, filtering the pixels having collected a signal charge. SDC-2, the chip prototyping this micro-circuit, also called suze-01, was designed and fabricated in 2007. Its main features are described in this paper, as well as its first test results.

2 Overview of the sensor architecture

2.1 Hit recognition and encoding format

The final sensor on which the zero suppression micro-circuit will be integrated consists of 1088 columns read out in parallel, each composed of 544 pixels. Each column is terminated with a discriminator. The pixels are squares of 18.4 μm width. The corresponding binary single point resolution is expected to be less than 4 μm.

The sensor is read out in a rolling shutter mode, the rows being selected sequentially by activating a multiplexer every 16 clock cycles.
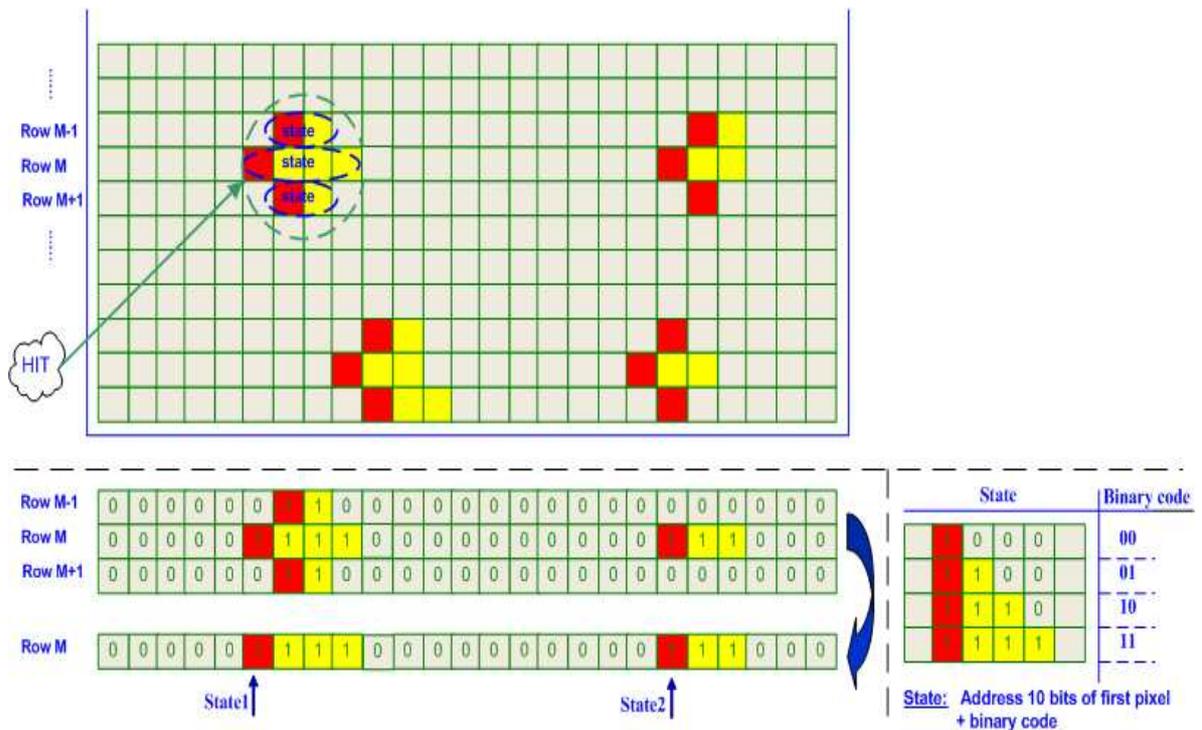

Figure 1: Schematic view illustrating the encoding of the pixels delivering a signal above discriminator threshold.

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Figure 1 shows an example of a digital matrix frame with some hits. A hit manifests itself via a cluster of pixels delivering a signal above the discriminator threshold. The clusters usually spread over several rows. As the matrix is read row by row, a hit will be identified through a couple of contiguous pixels delivering a signal above threshold. Their coding is performed in terms of *states*, each representing such a group of successive pixels in a row. The state format includes the column address of the first hit pixel, followed by 2 bits encoding the number of contiguous pixels in the group delivering a signal above threshold. A maximum number of 4 contiguous pixels is accounted for. The row address is represented by a 10 bit number and is common to all states in a row.

M states by row can be processed. This limit was derived from a statistical study based on the highest occupancy expected in the pixel array.

2.2 Principle of the hit finding algorithm

The zero suppression logic is based on sparse-scan read-out in order to optimize the data bandwidth. A fast priority scan path between the first and last discriminator outputs is implemented to minimize the delay within the critical data path. The 1088 column terminations are distributed over 17 banks (see Figure 2), each bank being connected to 64 columns. The digital architecture allowing to find the '1's in a row of discriminated outputs is based on a "Priority Look Ahead" (PLA) algorithm. It uses a chain of alternated NAND and NOR gates for the priority management during the sparse-scan.
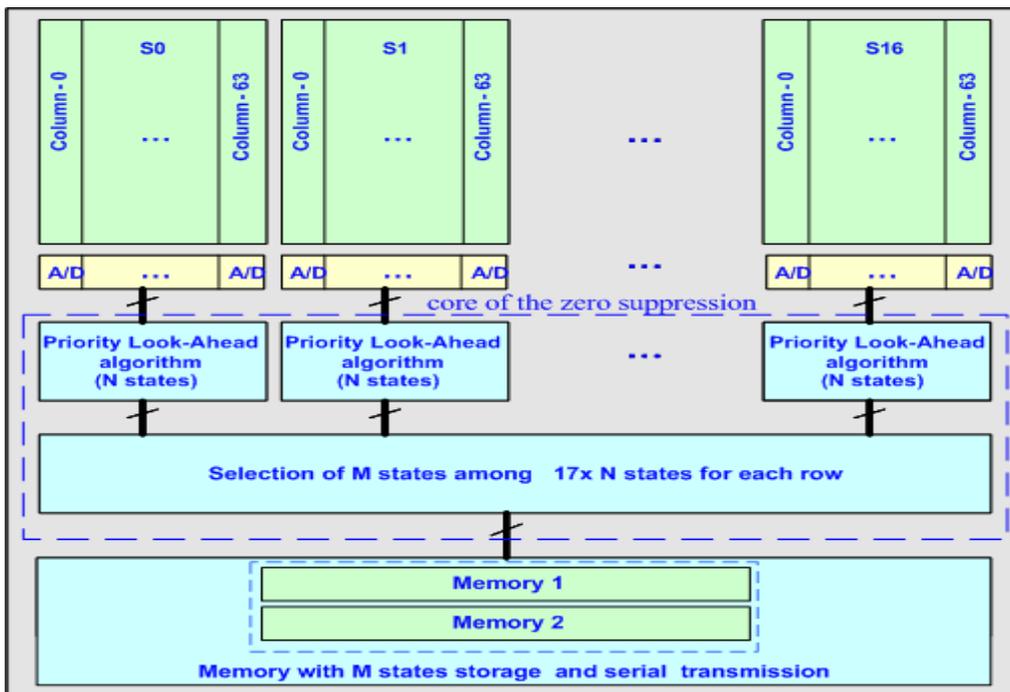

Figure 2: Block diagram of the sensor read-out architecture.

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A specific logic is implemented to deal with the interface between adjacent banks in order to ensure the continuity of the algorithm and the entire row processing.

Figure 2 displays the block diagram of the read-out architecture. The zero suppression algorithm is based on the following main components. Each pixel bank is equipped with its own PLA logic, all banks being active in parallel during the row processing. The outcomes of all banks are combined with a multiplexing logic while the next row is being processed. The outcome of this step is stored in the memory while the subsequent row is still being read out. These operations are repeated continuously.
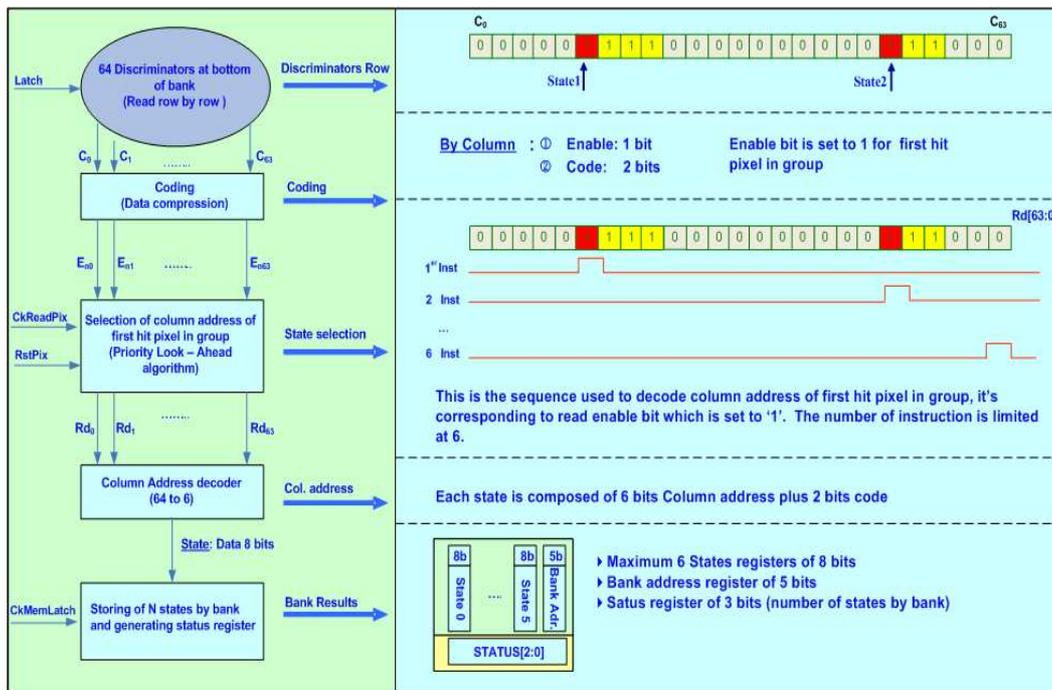

Figure 3: Block diagram of the Priority Look–Ahead algorithm at the bank level.

Figure 3 shows the different steps of the PLA for one bank. The algorithm proceeds through four consecutive steps, summarised below:

- In the first step, the data inputs for the process are extracted from 64 discriminator outputs;

- The second step consists in encoding groups of hit pixels. This logic provides Enable bits and Code bits for each column composing a bank. The Enable bit is set to 1 for the first hit pixel in a group. The number characterising the state corresponds to the number of Enable bits which are set to 1;

- The next step consists in selecting the states; each state is selected successively by a PLA. Several instructions are required to deliver the states. The number of states (N) in a bank is related to M states in a row. The possibility to generate up to 6 (N) instructions or states in a bank has been implemented in the algorithm;

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- After each instruction, the column address of the state is decoded. The last step of the logic consists in storing the N states and in generating a status information which indicates the number of states per bank. Each bank has its own address encoded on 5 bits.

For a row, each bank provides a maximum of N states. Another logic, based on multi-plexers, allows selecting a maximum of M states among 17xN (bank) states. Thus, only up to M states get stored in a memory. In case more than M states get identited, an overflow bit is set to 1. The format of the row states includes the row address, a status register (number of states in the entire row), the states column addresses, and 1 overflow bit.
The states are stored in a dual channel memory. One half of the memory (memory 1) stores the states per row during the current frame read-out, while the second half of the memory (memory 2) stores the states during the subsequent frame read-out. During the writing phase of memory 2, the data of the previous frame contained in memory 1 are transmitted to the data acquisition system.

3 Description and tests of SDC Prototype 2

3.1 General remarks

Prototype SUZE-01 was designed to validate the concept of the Priority Look Ahead algorithm described in the previous section. The chip incorporates all the logic needed to read a pixel matrix made of 544 rows x 1088 columns. For economical reasons, the chip area was restricted to the minimum required, meaning that only 2 rows of 2 blocks of 64 pixels were implemented. A JTAG controller is integrated in the chip, mainly for the communication between the core of the system and an external test structure. The fabrication process is the usal AMS C35B4C3 CMOS 0.35 μm technology in which most MIMOSA pixel sensors are manufactured.

3.2 Chip architecture

The chip is steered with a synchronized external 100 MHz clock, and includes the fol-lowing features:

- Power On Reset interface;

- JTAG interface:
    - Table of configuration registers (write only):
        * for configurable sequencer,
        * for any given pattern of 2 rows (row 0 and row1), or for target result for internal comparison,
    - Table of status registers (read only)

- Sequencer for row, frame and real time recording on memory, configurable by JTAG;

- Look Ahead algorithm and its logic suppression of zero core;

- Main 2 x 6 states to 9 states multiplexer;

- FIFO composed of 4 SRAM 600 x 16 bits and its corresponding management system;

- 1 LVDS loop IN/OUT with a bidirectionnal 9 bit port.

3.3 Chip operation

The internal sequencer emulates a frame made of 2 rows, each composed of 2 blocks of 64 bits. These rows repeated x times will form the frame. This part also generates the synchronization signals for the row, the entire frame and memory signals. The row read-out duration is 160 ns. This configurable frame can include until 1200 rows of the contents of the 2 previously quoted rows repeated x times. It can be divided into 4 zones maximum with 2 empty zones (row with no hits) and 2 full zones (2 x (row0 and row1)).
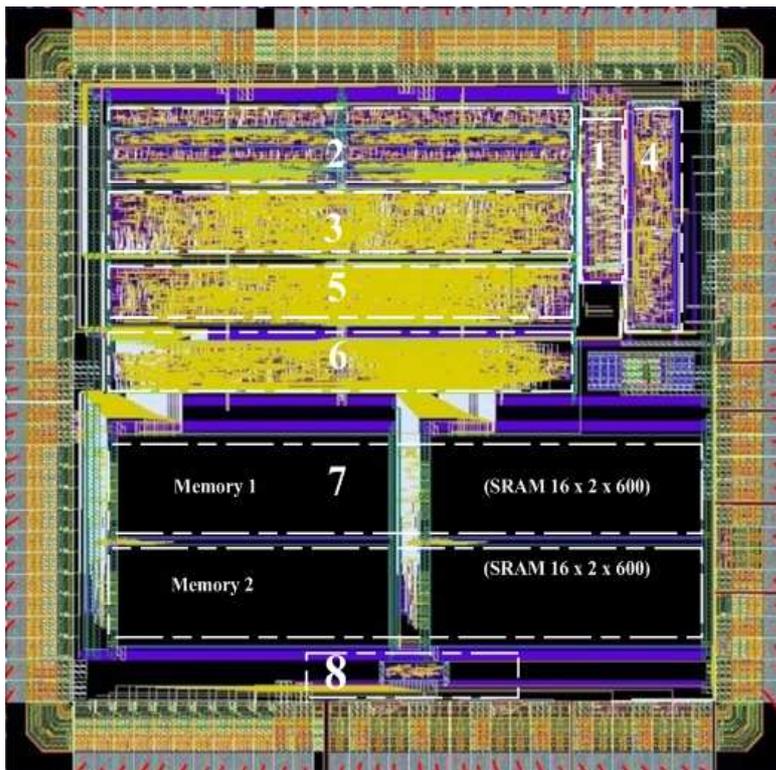
Part 1:
JTAG

Part 2:
Priority Look Ahead algo.

Part 3 & 4:
Sequencer for row, frame & memory synchronisation

Part 5:
Selection of 9 states among 2 x 6 states

Part 6:
Memory management

Part 7: FIFO
2 blocks of memories with M states storage

Part 8:
Serial transmission

Figure 4: Layout of SDC Prototype 2, alias SUZE-01.

The read-out of each row may be done with JTAG at the different levels of the chip. The acquisition of the entire frame is possible for up to 600 states per frame in real

time, using an external logic analyser. Each state requires 10 bits for the row address, 11 bits for the column number and 2 bits for the state coding (up to 4 pixels) in the most extreme case. For each row, its address is sent once to the memory. The content of the memory is read out from the chip; it is made of 16-bit data (states) and a 10-bit address with the control signals.

To reduce the number of pins, we integrated on the chip a multiplexing structure which is configurable by JTAG for pin selection. In the final EUDET sensor, the content of the memory will be multiplexed and read on a serial LVDS flow. Therefore, the maximum speed affordable by the internal LVDS drivers and receivers still compatible with the chip low power consumption requirements had to be assessed in a dedicated structure.

3.4 Specifications

Part	Parameter	Typical Value	Comments
Read-out	RD Frequency	Up to 100 MHz	Readout Clock LVDS signal
	CKRD Duty Cycle	50%	
JTAG	TCK Frequency	10 MHz	Boundary Scan Clock
	TMS Setup/Hold Time	10 ns	Boundary Scan Control Signal
	TDI Setup/Hold Time	10 ns	Boundary Scan Serial Data In
Memory	sampling frequency	100 MHz	Organization 600 x 16 x 4
	size	38400 bits	id.
	frequency max	200 MHz	
	reading speed	100 Mbits/s	
States	max. nb adjacent pix.	4	
	address coding	21 bits	
	coding	2 bits	
Bank	number of pixels	64	
	max. nb of states	6	
Row	number of banks	2	
	max. nb of states	9	
	reading time	160 ns	
Frame	reading time	110 μs	

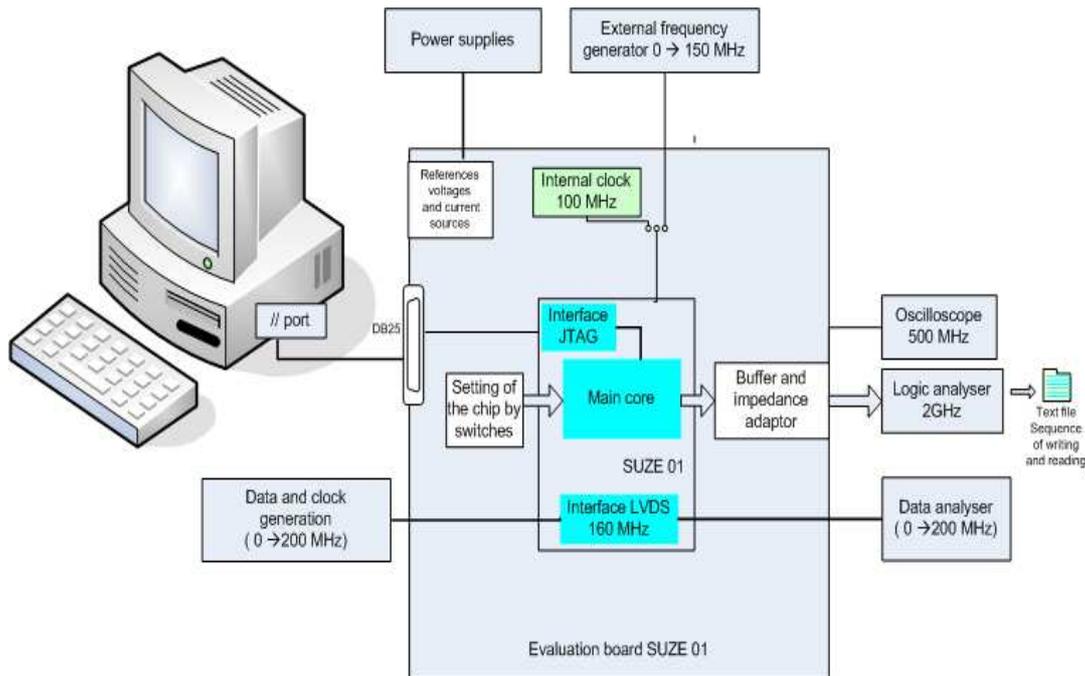Table 1: Technical description of the main SDC Prototype 2 specifications.

Figure 5: Schematic view of the test set-up of SUZE-01.

3.5 Functionnality test set-up

The tests of the chip required designing and fabricating a dedicated evaluation board. The latter interfaces with a PC platform via a standard parallel output. The dedicated communication through the JTAG protocol is initiated by a user interface written in C. This user interface allows to configurate registers in ordre to initiate a sequence. This complex sequence includes the synchronisation of the frame simulation, based on the repetition of the pattern of the two rows equipping the chip a configurable number (x) of times. The result of the frame is written into a memory. The reading of the result of the previous frame is performed in real time on the external plugs connected to a logical analyser.

3.6 Test results

The tests of the chip functionnalities have started in Novembre 2007. They concentrated on the zero suppression functionning, which is the most critical aspect of the prototyping. Read and write operations were performed via the JTAG controller. After loading data patterns of 2 rows into the configuration registers, it was checked that the core of the zero suppression micro-circuits decodes correctly the column addresses of the hit pixels within 160 ns, which is the time of a complete row read-out sequence.
The tests could then be performed extensively. Their main present outcome may be summarised as follows:

- The number of states detected by a bank was checked without spotting any error ($N \leq 6$ states);

- The logic implemented to deal with the interface between banks in order to ensure the continuity of the algorithm and the entire row processing was tested and validated;

- The test of the selection of M states among 2 x N states for each row delivered all results expected. To do this, M was varied from 0 to 9 states;

- All the results above obtained using the JTAG protocol without using the memory. In order to test the dual channel memory, we have performed a built-in self test sequence validating the writing and the reading of the entire space of the memory. This was achieved by writing successively the values "0", "5A" and "A5" in hexadecimal numbers inside all the addresses of the memory, and by checking consecutively that these values were read out properly.

The next steps of the validation address the entire zero suppression concept, based on a large variety of sequences of x frames representing a matrix of pixels, exploring various combinations of row patterns. In order to perform these tests, a text file emulating a matrix of pixels is sent to the logic via JTAG.

The LVDS receiver and driver integrated in SUZE-01 were designed with a strong requirement on the power consumption. Their tests demonstrated that they can be operated within their specifications at 160 MHz (the frequency which will be used later in the EUDET final pixel sensor).

4 Summary

SDC Prototype 2, an essential component of the final telescope sensors, has been designed and fabricated in 2007. Its main purpose is to select those pixels of a frame which have collected a signal charge. The consecutive data flow reduction will allow running the telescope on high intensity particle beams.

The functionnality tests of the prototype are well advanced. They show that the pixel selection and information encoding is fully operationnal and works as expected up to thew highest clock frequency foreseen. An exhaustive program of tests is under way, which will be completed in January 2008. This is well on schedule for the next step, which requires implementing the zero suppression logic on the periphery of the final sensor, to be fabricated in the second half of 2008.

Acknowledgement