Progress on the JRA1 Trigger Logic Unit (TLU)

D. G. Cussans*

December 6, 2007

Abstract

The JRA1 Trigger Logic Unit was designed to ease the task of integrating a "Device Under Test" with the JRA1 beam telescope. Prototype units have been constructed and have been operated in beam-tests. Experience of operating the TLU, current status and future plans are described.

*University of Bristol,United Kingdom

1 Introduction

The TLU is a small, low-cost unit based around a FPGA. It is described elsewhere[1],[2]. TLU has been used in INFN, the University of Bonn, the University of Geneva, ULB, as well as in Bristol. Being used has thrown up some bugs, which is extremely valuable. Some obvious bugs found and fixed.

2 Experience of TLU in use

A number of issues were reported, of varying degrees of severity.

- **Occasional spurious trigger** Probably due to use of unshielded cable for LVDS connection and poor grounding. Suggestions on on grounding and signal integrity were added to documentation[2]
- **Problems with TLU being recognised when connected to USB port** A "fix" for some of these problems was supplied by Bonn group. The issue may also be circumvented by rebuilding firmware to avoid USB re-enumeration[3].
- **Trigger number out of step on different DUT outputs.** This was traced to a bug in the DAQ software rather than a problem with the TLU.

3 Firmware Enhancements

In response to experience operating the TLU a number of firmware enhancements have been implemented, or are planned. These are: a fixed latency trigger, DUT initiated busy, scalers for counting input triggers.

3.1 Fixed Latency Trigger

In the first version of the firmware the incoming triggers were sampled with an internal 48MHz clock at the first stage of trigger logic. The lead to a timing jitter in the latency between input and output triggers of up to one clock cycle. To accommodate the potential needs of devices like the TPC the firmware was modified to give a fixed latency between input and output triggers. In essence the trigger is set asycnronously with respect to the system clock and cleared synchronously.
Figures 1 and 2 show a simplified version of the logic used to set the trigger and the finite-state-machine(FSM)that control it being cleared. Each DUT interface connected to a separate FSM. The trigger output for each DUT is connected to a multiplexer. In IDLE state, asynchronous trigger connected to trigger outputs.

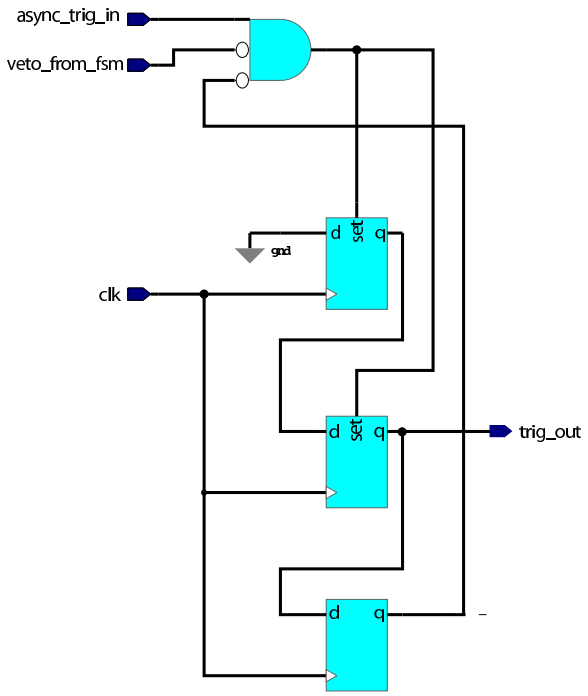

Figure 1: Asynchronous-set/Synchronous-clear Logic

4 Trigger Latency Timing Jitter

The latency between incoming beam trigger and trigger to DUT measured using a Lecroy LT6051 oscilloscope. For fixed height pulses the measured latency was 27.3 ± 3ns. Uncertainty is due to different delay at different DUT outputs and predicted variation due to temperature variations. Approximately 13ns of delay is from FPGA and 14ns from the discriminator. The timing jitter (the fluctuation in the latency on a particular DUT output at a particular temperature) was measured as $24 \pm 5ps$. This is far better than expected, but not totally inexplicable. Since the FPGA is quiet except during readout there is little noise generated that would lead to timing jitter. The TLU currently uses simple threshold discriminators and there would be "timing walk" if the pulse height fluctuates.

4.1 DUT Initiated Busy

The FSM controlling the trigger handshake has been altered to allow the TLU to be put into the BUSY state by raising the BUSY line. Previously the DUT was only permitted to raise the BUSY line in response to a trigger from the TLU. This is convenient, but introduces a race condition where simultaneously a trigger is send by the TLU and a DUT initiated busy is sent by the DUT.

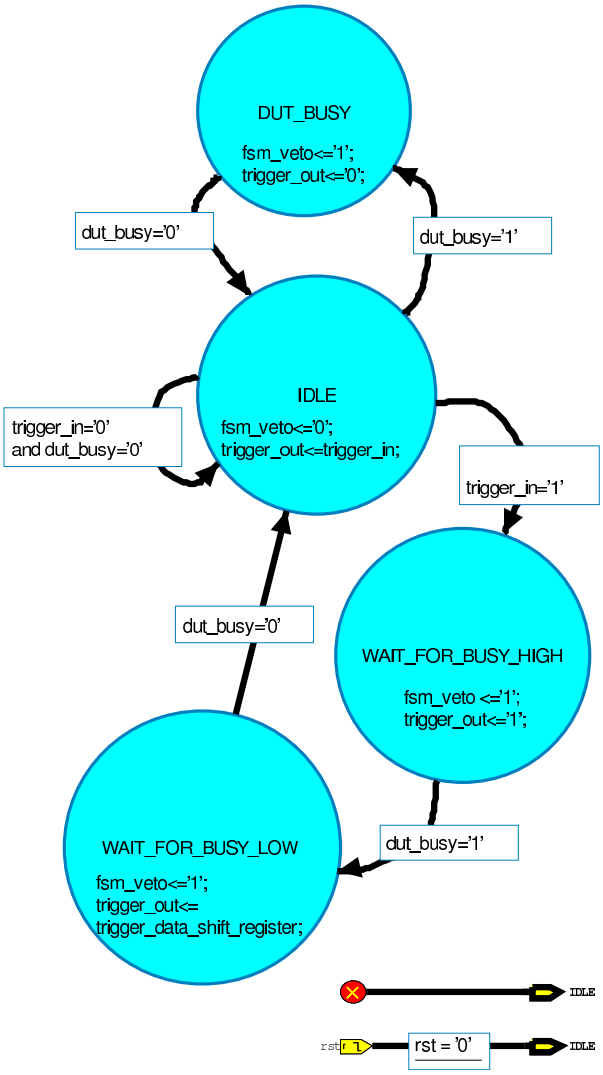

Figure 2: Finite State Machine for TLU Trigger Outputs

4.2 Usability Enhancements

One of the aims of the TLU is to make the use of a NIM crate unnecessary. In pursuing this aim scalers have been added to the beam-trigger inputs (16 bit) and work is in progress to add scalers on pre-veto trigger. This will allow the input trigger rates and the dead-time to be measured. Work is in progress to increase the width of the 16-bit scalers to 32-bits.

5 Plans

- **Firmware Changes**
  - Continue with "usability enhancements"
  - Implement swapping between internal and external clock sources.(Clock input present and tested but needs work since it involves crossing clock domains)
  - Improve time-stamp resolution from 20ns to 2.5ns
- Hardware Changes
  - Provide HDMI connectors as well as RJ45 for interface to DUT. This will allow operation with the Calice readout system. In addition cable shielding much better on HDMI than Ethernet cabling.
  - More inputs and outputs, both trigger interfaces and DUT interfaces.
  - Provide coaxial I/O switchable between NIM and TTL levels.
  - Modify TLU hardware to allow stand-alone operation:
    * Stand-alone configuration of FPGA.
    * Switches to allow control by front panel.
    * Display of trigger counts and TLU status.

6 Conclusion

Work has been done to improve the performance and usability of the JRA1 TLU. Further work is underway.

Acknowledgement

This work is supported by the Commission of the European Communities under the 6^{th} Framework Programme "Structuring the European Research Area", contract number RII3-026126.

References

[1] D. G. Cussans,"A Trigger/Timing Logic Unit for ILC Test-beams", Proceedings of the 1st topical workshop on electronics for particle physics (TWEPP), Prague, Czech Republic. September 3-7, 2007.

[2] D. G. Cussans, "Description of the JRA1 Trigger Logic Unit (TLU)", EUDET-Memo-2007-02

[3] EZ-USB FX2LP(TM) - Low Power (Bus Powered) Programmable MCU for bus power peripherals. Cypress Inc, 198 Champion Ct. San Jose, CA 95134 USA, 2006.