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Front-end electronics and data acquisition for the LCTPC *

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Abstract

A status report is given on the front-end electronics developed to study the performance of the 'large' prototype TPC, built in preparation for the International Linear Collider (ILC). The read-out electronics is based on a system used in the ALICE experiment at the LHC, but with modifications needed to be compatible with new gas amplification systems and small pad sizes foreseen for the final TPC at the ILC. So far the data acquisition is handled by a minimal system, using the hardware and the drivers of the ALICE experiment, but with a software being developed for the new readout system.

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1 Introduction

The detector at the future linear electron-positron collider ILC (International Linear Collider) will include a tracking device, which is able to provide a momentum resolution sufficient to observe a possible Higgs signal from the missing mass spectrum of the Higgs strahlung processes. One option for such a tracking devise is a large TPC using new gas amplification techniques, like GEM's or Micromegas, together with smaller pads compared to previously used. In order to study the performance of such a TPC, a 'large' prototype is being built, offering a certain modularity with respect to investigating various gas amplification systems, pad sizes and geometries as well as different read-out systems.

2 Mechanics for the front-end electronics

The cylindrical field cage will be placed in a solenoid magnet, which provides a nominal field of 1.2 Tesla [1]. The field cage will be moved in axially into a position where the magnetic field is homogeneous within 1% accuracy. The support structure of the magnet should allow movements vertically and horizontally in a plane perpendicular to the incoming test beam, which enables to explore the full TPC detector volume with the test beam. A rotation around the axis of the cylindrical field cage inside the magnet will also be possible in order to study inclined tracks and allow data taking with cosmic muons. These requirements put some constraints on the mechanics of the front-end electronics.

The main read-out system which will be used is based on the read-out electronics developed for the ALICE experiment [2]. Some modifications are necessary in order to adapt it to the expected output signals from the new gas amplification systems, including a new programmable charge amplifier. The schematic layout of the system is shown in Fig. 1. One complication is given by the fact that the effective area occupied by the front-end card (FEC) per channel is significantly larger than the smallest pad size to be investigated, which is 1x4 mm^2. Thus the FEC's can not be attached directly to the pad plane, but have to be connected via kapton cables. In order to prevent the cables to be pulled out by accident as the system is moved in and out of the magnet, the electronics crate needs to be fixed to the field cage so that they can move as one unit. This also allows a common rotation of the electronics with the field cage.

The TPC itself will rest on rails inside the magnet on which it can slide back and forth as well as be rotated. These rails should be extended towards the outside of the magnet such that the field cage and the electronics crate can be positioned well outside the volume of the magnet to provide good access for the attachment of the cables. Although the electronics crate has to be mechnically fixed to the flange of the field cage, it will not be able to take the load of the electronics. Instead the electronics crate, like the chamber itself, has to rest on the rails. This means that the crate needs to have a cylindrical structure of the same radius as the field cage.

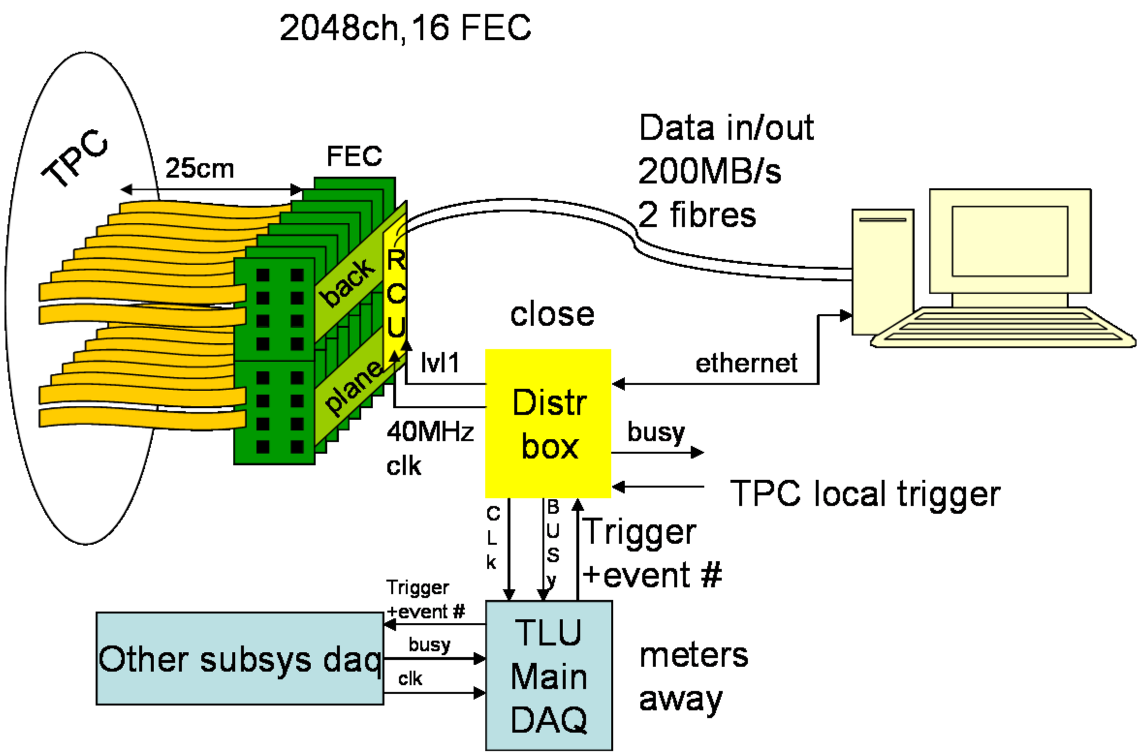

Figure 1: *A schematic view of the front-end electronics and the read-out system.*

3 The end plate and pad modules

The end-plate will contain seven 'windows' into which pad modules can be inserted. These modules are identical and organized in three rows to cover as much as possible of the end plate area. The curvature of the modules are chosen such that it corresponds to a limited part of the full size end-plate of the final TPC. The modules are organized in groups of two, three and two modules, respectively, as illustrated in Fig. 2. The three rows have been staggered with respect to each other so as not to give a continuous gap between them along a straight track. The modules are mounted onto the end plate from the inside, which maximizes the area which is available to cover with pads. However, a 10 mm wide strip along the outer and inner edges of the module are needed for support of a GEM structure. Alternatively, a 2 mm wide strip is required along all four edges for the support of a Micromegas structure. The pad signals have to be distributed to high density connectors on the pad board face opposite to the pads. The connector constitutes the mechanical interface between the TPC end-plate and the read-out electronics. The back side of a pad module has a metal frame along its edges, 14.5 mm wide, which contains precision dowel holes for positioning the modules and threaded holes for their mounting onto the end-plate (see Fig. 3). An o-ring ensures the gas tightness. The frame also provides the necessary stiffness of the pad board. The width of the frame reduces the available area for connectors compared to the pad area.

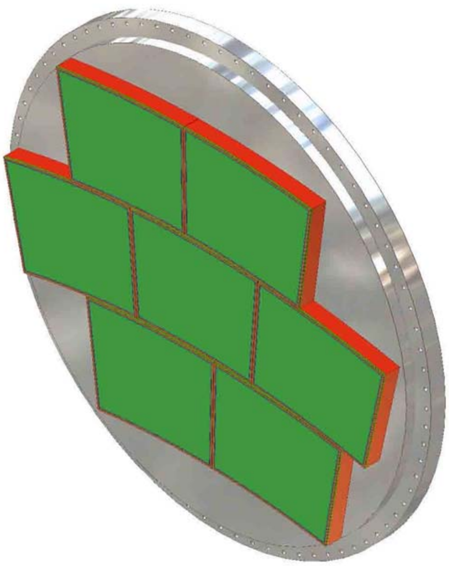

Figure 2: *The end plate with the seven pad modules.*

Assuming a minimum pad size of 1x4 mm^2 and excluding the strips foreseen for the support structure of the GEM system, the pad area can accomodate 36 rows of 4 mm long pads with 0.1 mm spacing. The number of '1 mm' wide pads per row will be the same and with a spacing of 0.1 mm amounts to around 200 resulting in a total number of pads per module of about 7000. In accordance with the shape of the pad module the pads themselves have a trapetsoidal shape which gives somewhat narrower pads at the inner edge compared to those along the outer edge. The exact number of pads thus depends on which row of pads have the pad width exactly 1 mm. A pad width of 1 mm along the innermost edge of the module gives fewer pads per module compared to whether the pad width is chosen to be 1 mm along the outer edge of the module.

4 Pads and connectors

As mentioned above the minimum pad size considered has an area of about 1x4 mm^2 with a separation between the pads of 0.1 mm. The connectors, mounted directly onto the back side of the pad plane, have to be high-density connectors in order to match the area given by the pad. Japan Aviation Electronics offers a connector, which fulfills this requirement. It is a 40 pin connector with 0.5 mm pitch and outer dimensions 13.9 x 4.7 mm^2 for the male connector, which is mounted onto the board. The dimensions of the

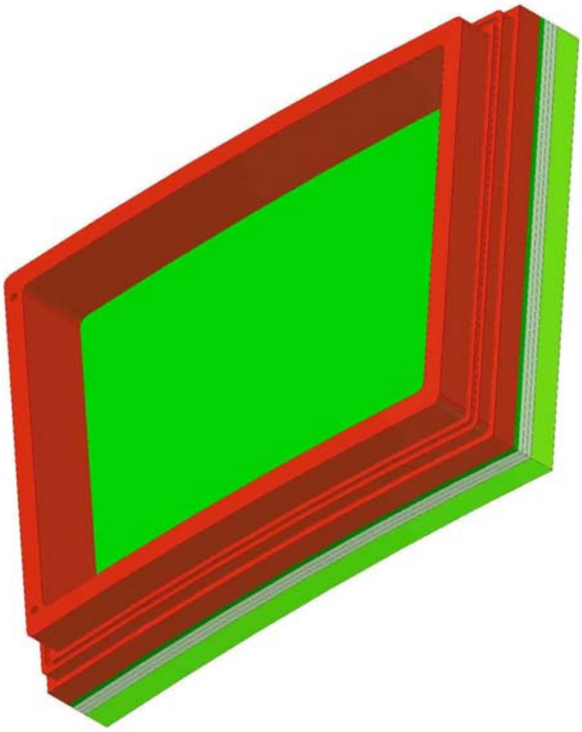

Figure 3: *The back side of a pad module showing the metal frame which surrounds the area available for connectors.*

female connector is somewhat bigger and also needs some space to support the capton cable.

If 32 pins are used for signal read-out, it leaves 8 pins for grounding, which should be sufficient. Subdividing the pad plane in units of 32 channels offers high modularity, which is an advantage in a situation where only a fraction of the pads can be equipped with electronics. Thus, it gives some flexibility in varying the geometry of the pad area, which can be read out. The starting point is that at least 2000 electronics channels are needed. In order to systematically study the performance of the detector system this small number of channels should still be acceptable, since the incoming particles can be directed into the specific detector volume, which is covered with read-out instrumention. With a limited number of electronics channels it must, however, be possible to disconnect the electronics from one pad module and move it to another one or even to install it on a different end-plate. In an extended study the number of read-out channels is planned to be increased to 10000.

The trace routing from the pads on one side of the end-plate board to the connector on the other side has been studied. Since the pads are small, the input capacitance will be small, which is an advantage from a noise point of view. In order to conserve the low input capacitance and keep the cross talk to a minimum, the trace length to the premplifier input has to be as short as possible. The density of the connectors has to be very high in order to accommodate enough connectors to read out the complete number of 1x4 mm^2 pads of a module. The routing between the connectors and the pads constitutes an especially great challenge in the corners of the module where the distances are the longest due to the mounting frame. In the full size TPC the pad modules is likely to be significantly bigger such that the relative difference between the pad and connector areas decreases and consequently the connectors can be distributed more spaciously.

For the prototype TPC, in the initial stage, the routing problem is circumvented by the fact that only a fraction of the total number of pads will be equipped with connectors and electronics. This leaves more room for the connectors available. However, this means that it is necessary to fix the geometry of the pad area which should be read out. It is reasonable to assume that it should be possible to reconstruct a high momentum track through the full diameter of the chamber. Defining a 'road' of 1x4 mm^2 pads through the chamber would in the case of a 2000 channel system give a 19 mm wide 'road' whereas in a 10000 channel system the 'road' would be 92 mm wide. The position of such a 'road' should be such that it covers the gap between some adjacent modules in order to test the effect on the track reconstruction of such gaps. During this stage it should be investigated whether the small pad size of 1x4 mm^2 is needed to obtain the desired momentum resolution or whether a bigger pad size may be used. In a later stage where all pads will have connectors, the geometry of the pad area that is chosen to be read out is only limited by the modularity of the 32 pin connectors. On the other hand the routing problem has to be solved.

Due to the small pitch of the connector pins and the positions of the pads with respect to the connectors, the requirement of the shortest possible routing is not compatible with using a single layer board but a multilayer board is necessary. This also ensure sufficient grounding and blind vias to avoid gas leakage.

5 The front end electronics

The read-out electronics for the large prototype should offer a performance that is better than that of the final TPC, so that the compromises that may become necessary for the multimillion channel final system can be studied and optimized. In order to meet these requirements the front end electronics will contain a programmable charge amplifier ASIC, called PCA16, and digitisation up to 40 MHz sampling rate by a modified ALTRO chip [3] , as developed for the ALICE experiment.

The existing front end card, available from the ALICE experiment, contains 128 channels and have the physical dimensions of 19 cm height and 17 cm depth. The height of the card together with the 4.7 mm width of the connector, correspond to an area of 893 mm^2, which clearly is not compatible with the 128 mm^2, covered by 128 pads of 1 mm width. It is thus clear that the use of these boards will need connection via cables. Since the very small sensor pads together with short input traces give very low input capacitance (≈ few pF), the external conditions for excellent noise performance both for random noise as well as for coherent pick-up noise should be good as long as the cables can be kept sufficiently short. Kapton cables of 25 cm length should be short enough to keep the noise level at an acceptable level. However, the distribution of the signals from the pads to the position of the FEC's sideways reduces the distance between the field cage and the electronics to a few centimeters. With connector receptacles offered in both straight and right angle connectors, easy plug-in of the cables at the pad board and the front-end board is expected, with an arrangement shown in Fig. 4.

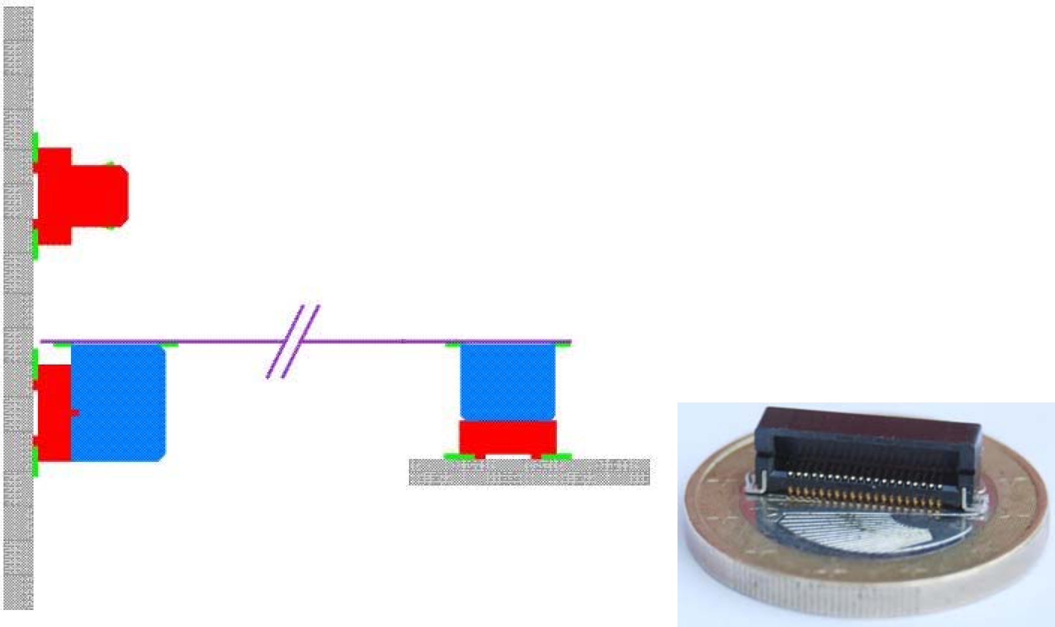

Figure 4: *The connector assembly showing how signals from the vertical pad board are transferred to the horisontal front-end board via capton cables. The size of a female connector is illustrated by placing it on a one Euro coin.*

5.1 The charge preamlifier

The specifications of the newly developed PCA16 programmable charge preamplifier are:

- 1.5 V supply; low power consumption <8mW/ channel.
- 16 channel charge amplifier + anti-aliasing filter.
- single ended preamplifier.
- fully differential output amplifier.
- both signal polarities.
- power down mode with a wake-up time of 1 ms.

- programmable peaking time between 30 and 120 ns.
- programmable gain in four steps between 12 to 27 mV/fC.
- preamp-out mode.
- tunable time constant of the preamplifier.

A first step towards the development of the PCA16 was to produce a non-programmable preamplifier with 12 channels (due to financial reasons) in order to confirm that the desired performance could be met. The 12 channel prototype preamlifier chip, with a fixed rise time of 100 ns, was produced in 130 nm CMOS technology. The test results of the preamplifier are summarized in Table 1.

Parameter	Specification	Simulation	MPR Samples
Noise	$<$ 500e	300e (10 pF)	270e (10 pF)
Conversion gain	10 mV/fC	10 mV/fC	9.5 mV/fC
Peaking time (default)	100 ns	100 ns	100 ns
Non linearity	$<$ 1%	$<$ 0.35 %	$<$ 0.3 %
Cross talk	$<$ 0.3 %	0.4 %	$<$ 0.3 %
Dynamic range	$>$ 2000	3300	4600
Power consumtion / channel	$<$ 20 mW	10 mW	10 mW

Table 1: *Comparison between specifications and results from simulations and tests of the preamplifier-shaper prototype.*

As can be seen from the table, the performance of the chip is up to the specifications or better. Especially one may notice that the noise is much below the specifications and the dynamic range is significantly wider.

The final PCA16 chip has recently been produced. It has a silicon area of 6 mm^2 with 94 pins in total. Out of these there are 16 input pins and 32 output pins for the differential pulses. The remaining pins are for grounding and voltage supply, and 9 pins are used to set the programmable parameters of the chip. The baseline option for control of the PCA16 is to use the the Board Controller (FPGA) to set an octal DAC (Digital to Analogue Converter), which defines the decay time of the pulse. An 8-bit shift register provides the digital input to the PCA16 in order to set the rise time, the gain, the polarity and to bypass the shaping function. In Fig. 5 a schematic diagram of the control system is shown.

A reprogramming of the FPGA is needed to include the additional functions to change the parameters of the PCA16 on-line. The data transfer between the PCA16 and the ALTRO is differential but is internally converted to single-ended analogue signals. A separation between the digital and analogue grounds is provided via the different grounding pins of the ALTRO. The programming of the PCA16 from the FPGA introduces the need for digital grounds. However, the signals from the shift register and the DAC's, used to set the PCA16 parameters, can be considered as D.C. signals and therefore the noise on the PCA16 input pins is expected to be negligible. This will be tested with the prototype board and in case there would be a problem a fall-back solution is foreseen, which allows to set the parameters manually by jumpers/dip-switches. In order

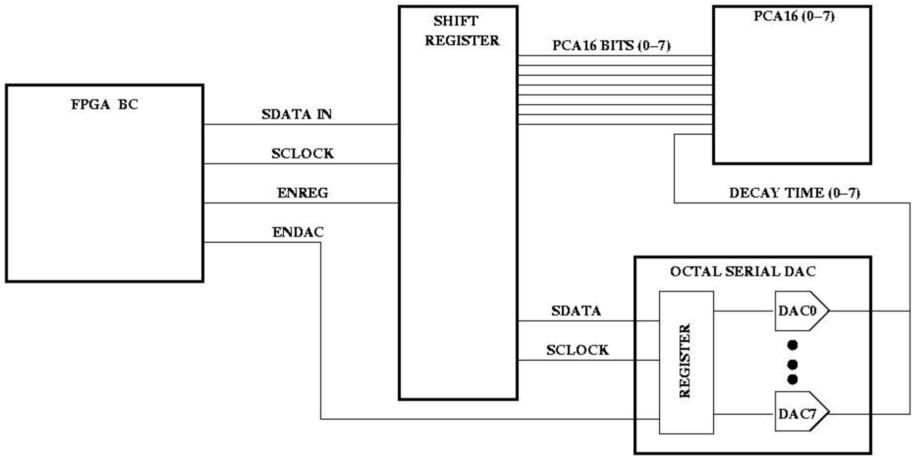

Figure 5: *Schematic diagram of the system to control the parameters of the PCA16*

to change between the options in a fast and simple way a female type connector, of the same kind as those being used for the input signals, has been added to the board. By simply attaching a male type connector the lines between the FPGA and the PCA16 chips are established. If instead a small board with the jumpers/dipswitches is attached the lines between the FPGA and the PCA16 chips are broken and the parameters have to be set manually from jumpers/dipswitches.
In total 1000 PCA16 chips have been produced, of which 200 have been delivered, which satisfies the need for the EUDET project. The remaining ones are reserved for the extended study.

5.2 The digitization

The sampling frequency needed for the digitization depends on the characteristics of the pulse from the gas amplification system. In order to accurately reconstruct the pulse shape to extract the charge deposited on the pad, a few points on the rising edge of the pulse are needed. With a sampling frequency of 40 MHz one would measure rise times down to around 50 ns. The ALTRO chip has been developed for the ALICE TPC to be operated at 10 MHz with 10 bit resolution. It offers a large flexibility and can be used as a general purpose AD-converter for a multi-channel system. If the sampling frequency is increased to 25 MHz the effective number of bits decreases to 9 which would still be sufficient for the expected input pulses. A new round of in total 16489 chips have been produced with an acceptance yield of 86%. After the delivery of 13400 accepted chips to other experiment, 883 chips remained from those which directly passed the performance test. Out of the chips that failed the test it is believed that about 730 can be recuperated, which makes 1600 chips in total available for the LCTPC large prototype. A modified version with 40 MHz sampling rate has been developed, which provides a resolution

corresponding to an effective number of bits equal to 9.5. Presently 125 chips of 40 MHz sampling rate are available, which corresponds to 2000 channels in total. These are intended to be used for the EUDET project.
The data transfer between the PCA16 and the ALTRO is differential, which allows separation of the analogue and digital grounds The ALTRO chip contains a memory of 1024 10-bit words for event storage. This corresponds to a depth of 25 μsec drift time at 40 MHz sampling rate. The maximum drift time in the 60 cm long prototype TPC is 15 μsec if we assume a drift velocity of 4 cm/sec. Thus, the 25 μsec event length foreseen for the ALTRO storage, provides sufficient margin for different gas choices. The ALTRO has a flexible sample by sample subtraction of pedestals accompanied by a powerful suppression of zero data. Thus, it is expected that only valid data will have to be read out from the ALTRO. This will reduce the requirements on the data aquisition (DAQ) system. The ALTRO chip is read out in 40 bit wide words on a customized 40 MHz bus.

6 The data aquisition system

The readout is based on the system used by the ALICE experiment where the FECs are placed on a backplane, which is controlled by a Readout Control Unit (RCU) [4]. Data is sent through a Detector Data optical Link (DDL) to a Detector Read Out Receiver Card (DRORC), which is a PCI card situated in a PC. The low level software consists of drivers and libraries for communicating with the DRORC and the front end through the DDL. ALICE needs a large complex data acquisition system. Trigger and timing control (TTC) in ALICE is done with the standard LHC TTC system and the ALICE Detector Control System (DCS). Fig. 6 shows an overview of the ALICE system. The requirements of the LCTPC project are less demanding than in ALICE. Since the LCTPC system will not be interfaced with the LHC system, we have chosen to develop a special purpose DAQ solution.
A schematic view of the components of the prototype TPC readout system, as described here, is shown in Fig. 7. The DBOX (Distribution BOX) and TLU (Trigger Logic Unit) is the replacement of the ALICE DCS and TTC system. A small modification of the RCU is required due to the fact that it will receive the trigger and clock signals from cables rather than from the LHC TTC system. The TLU is the central trigger unit for all subdetectors in a common test beam setup. The ALICE drivers and libraries for communicating with the readout hardware are used unmodified. In the following sections the software so far developed is described. It consists of the code that provides the configuration of the hardware, the readout, and the local data storage. A simple standalone monitoring and histogram presenter system has been implemented. The run control is done from a graphical user interface. Eventually, it will all be connected to a common beam test data acquisition system. A photo of the test prototype setup including one FEC is shown in Fig. 8.

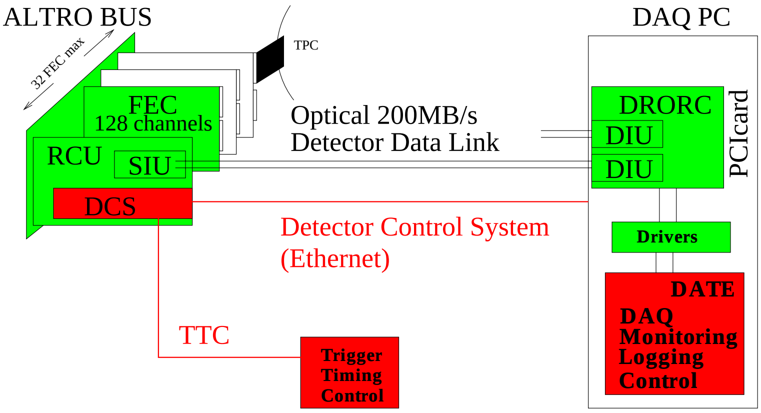

Figure 6: *Overview of the ALICE TPC readout*

6.1 Configuration

For the data acquisition to become active a START DAQ command must be received from the run control. This will initialize the handling of the DRORC, memory buffers in the computer, and the configuration of the front end electronics. There are several settings to be made in the front end electronics, e.g. the run operating conditions of the PCA16, ALTRO, and RCU must be downloaded. These values are stored in configuration files, which are read and downloaded when the START DAQ command is received from the run control. After the initialization the readout is waiting for a START RUN command.

6.2 Trigger and readout

When a START RUN command has been acknowledged, the readout system is ready to receive triggers. On the reception of a trigger from the DBOX the RCU distributes it via the backplane to the FEC's (Fig. 9). The TLU is common to all subdetectors involved in building events from the observation of particles in the test beam. The DBOX either takes the trigger from the TLU or from a local trigger system. The trigger starts the digitization of the analogue information from the PCA16 in the ALTRO chips, and a configurable number of time samples is stored in a memory in the ALTRO. The data is automatically read by the RCU and pushed into the DRORC, which stores the data directly into the physical memory of the readout computer. The readout program is polling the DRORC for new data, and stores the data in a file on a local disk. During the whole readout of an event the trigger system must be blocked from accepting new triggers. In the current test prototype system the DBOX is not yet available. Instead the parallel port of the readout computer is used to enable/reset triggers generated by a pulser. In the final system the DBOX will handle this. The communication between

the DBOX and readout program is done through the network. The readout program is subdivided into two parts, one part that handles the communication with the hardware, and one that acts as an interface to the run control through the network. These parts communicates with each other through TCP/IP sockets and Unix signals.
The synchronization of events between RCUs and other detectors will be done with a time stamp given by the time of the trigger from the DBOX together with the event counters in the DBOX and in each RCU. In a common environment the DBOX gets the event number from the central trigger unit (TLU).

6.3 Run control

The run control is written in Java. It can be run on any computer, and communicates with the readout program through the network. The control panel is shown in Fig. 10. The control has a few commands as described in table 2.
In the current version there is no logging of the run information.

START DAQ	The readout will open devices, setup and configure the readout, and download the configuration to the electronics.
STOP DAQ	Stop data acquisition. The readout will close all devices, and wait for a START DAQ command.
START RUN	Start a run. The readout enables the trigger system, and start polling for data.
STOP RUN	Stop a run. The readout disable the trigger system, and wait for a START RUN or a STOP DAQ command.
STATUS	Get status. Request the status of the system.

Table 2: Run control states

6.4 Monitoring

There is not yet a true real-time online monitoring. What exists is a MONITOR program that reads the data file, decodes the event format, fills histograms, and writes the histograms to a ROOT format file. There is another ROOT based program, PRESENTER, to display the histograms in the histogram file. The histograms in this file can also be viewed with ROOT directly. A true real-time monitoring with its connections will be implemented as indicated by the dashed boxes and broken lines in Fig. 11. The readout stores the events in a shared memory, a MONITOR SERVER sends events from the shared memory to the MONITOR program when it requests an event. This can be done over the network, i.e. the MONITOR can be run on any computer. The MONITOR creates and updates histograms in a shared memory, which is also accessible from the PRESENTER. The monitor server should also be able to playback a data file.

7 Conclusion

A high resolution tracking device is needed to meet the physics requirements at the future ILC. A large TPC with several million read-out channels, using new gas amplification technology, is one of the main options. The performance of such a TPC, with respect to different gas amplification systems, various gas choices and different sizes and geometries of the read-out pads will be investigated using a 'large' prototype chamber. The ALICE front end electronics has been modified to be compatible with the signals expected from the gas amplification. In order to fully exploit the potential of such a TPC system the front-end electronics includes a charge preamplifier, PCA16, that is programmable in terms of rise time, gain, polatity, decay time. The analogue signal from the PCA16 will be digitized by an ALTRO chip, which provides sampling at 40 MHz for 2000 channels and at 25 MHz for about 1600 channels. A prototype TPC data aquisition system is mainly based on ALICE components but with a special Distribution BOX and Trigger Logic Unit to provide the trigger and timing control. Software for the configuration of the hardware, the readout and for the local data storage has been developed.

Acknowledgement

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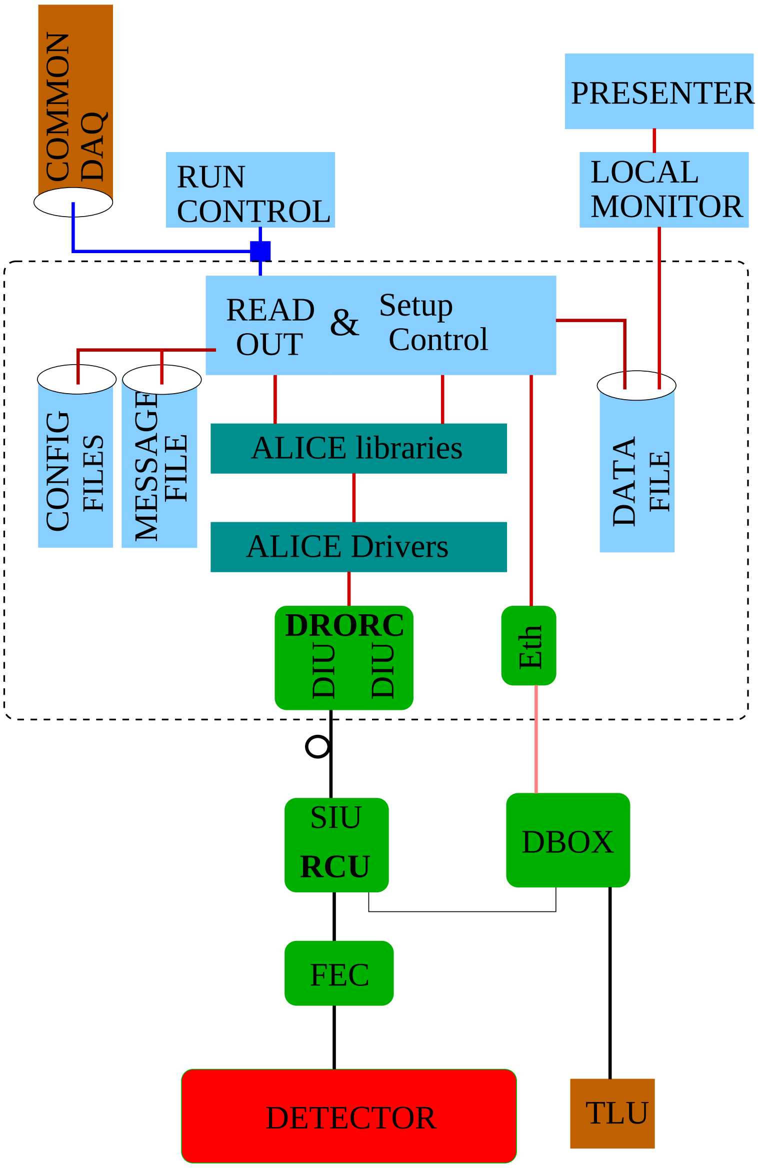

Figure 7: *Overview of the prototype DAQ TPC readout.*

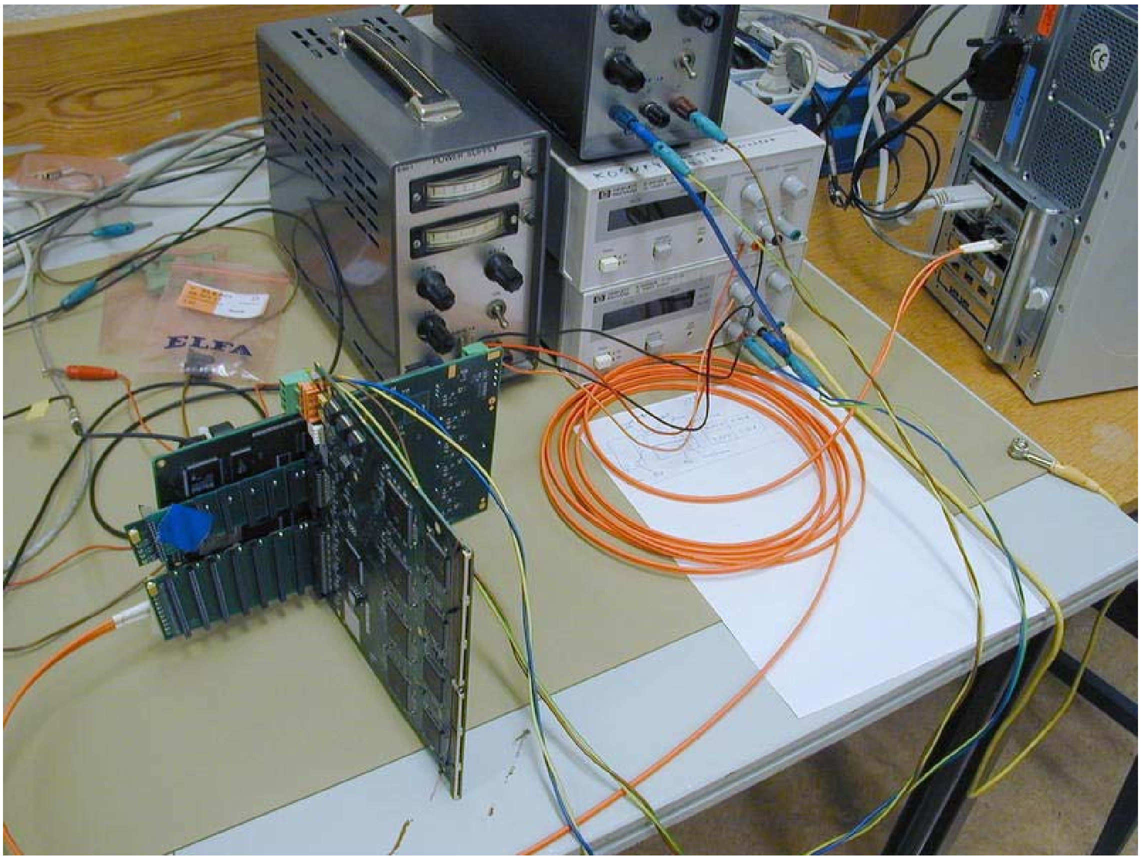

Figure 8: *Picture of the prototype DAQ readout electronics.*

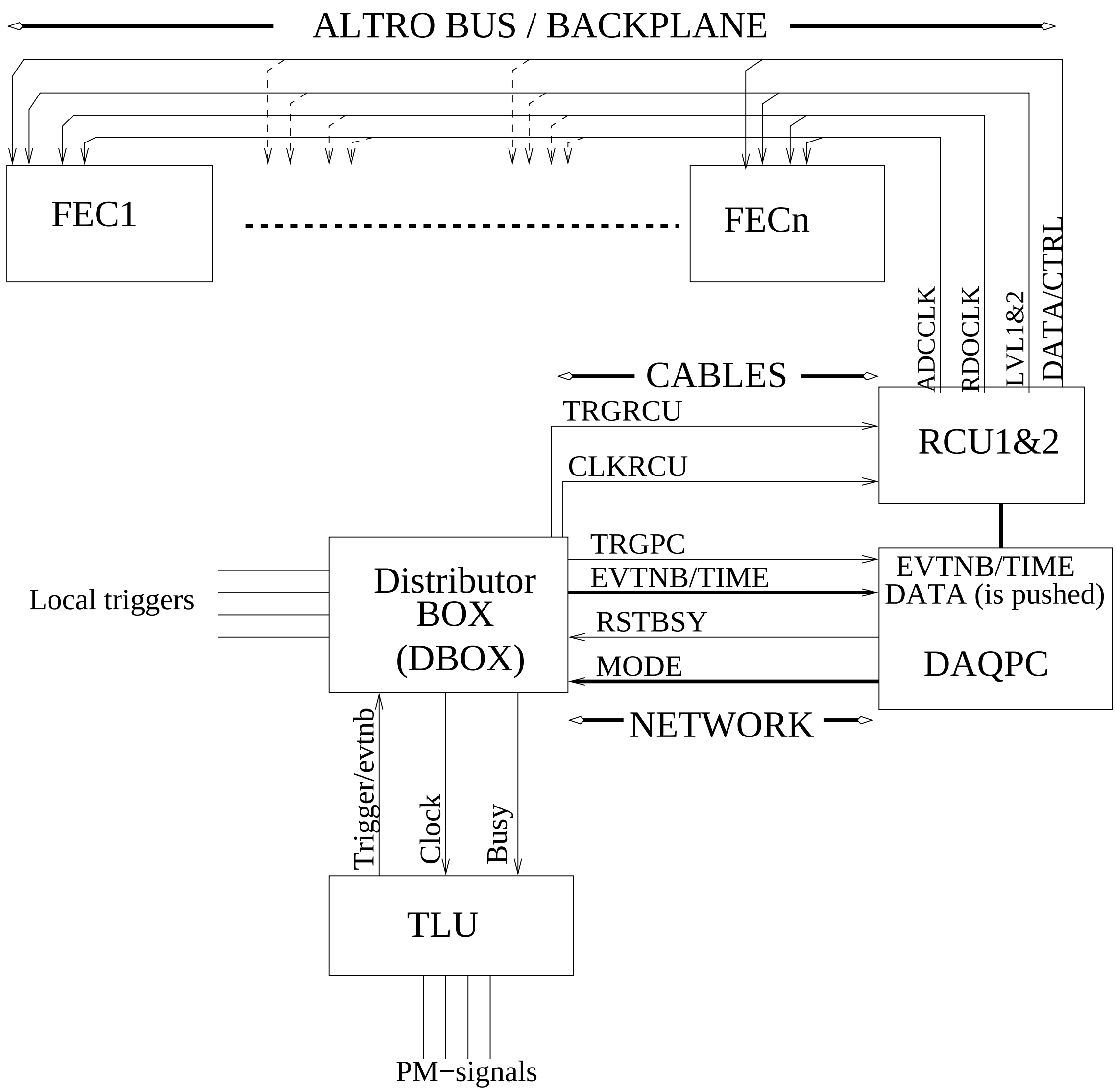

Figure 9: *The trigger and readout.*

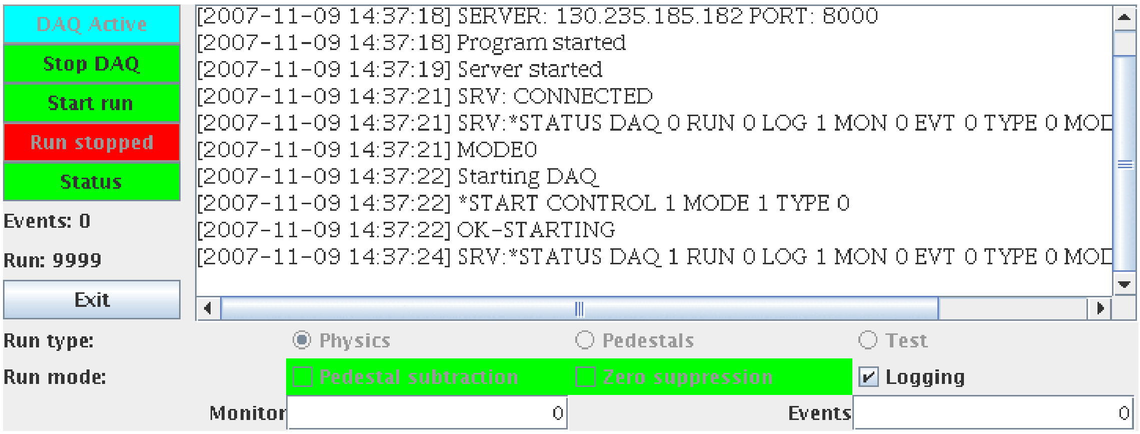

Figure 10: *The run control panel.*

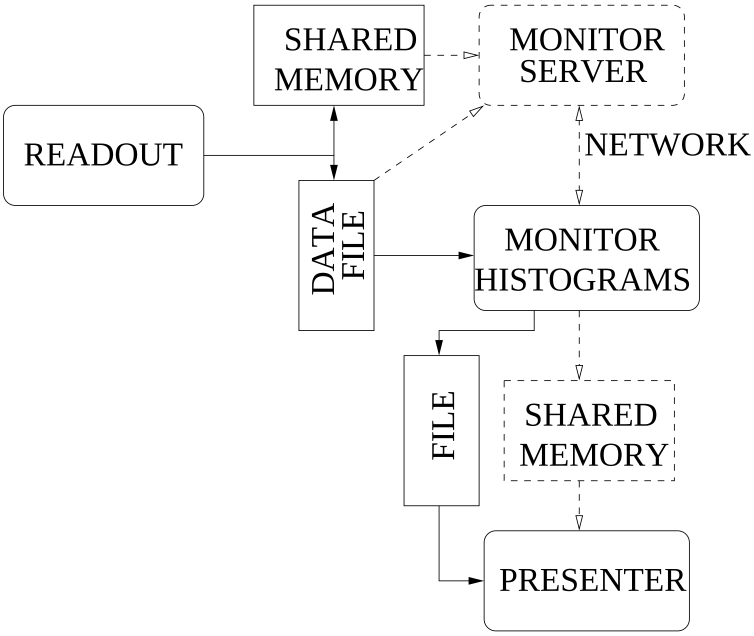

Figure 11: *The current and planned monitoring system. Dashed lines indicates future development.*