Status of the CEA Saclay R&D activities on pixelised readout of TPC

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Abstract

We report on the status of our last R&D activities on a pixelised readout for a TPC using the TimePix chip. We summarize the results of the wafer tests at CERN in which we participated inside the SiTPC collaboration. The yield of good chips reaches 73 %.

Based on Micromegas detector technology we built a small chamber with a 6 cm height field cage using this pixel technology protected by a resistive layer. We present the first X-rays observed in this digital micro-TPC. The design and construction of a deliverable panel made up of a matrix of 2 x 4 TimePix chips are in progress with the aim of being tested in the LC-TPC Large Prototype some time next year within the EUDET facility.

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1 Introduction

To achieve a spatial resolution better than 100 microns as required for the ILC-TPC, one of the solutions is to have a high granularity. This property is given by a pixelised readout CMOS chip called TimePix associated with a Micromegas detector [1,2]. The TimePix chip containing a square matrix of 256 x 256 pixels is described in [3]. Each pixel with dimensions 55 x 55 µm² has a low-noise preamp, discriminator, threshold DAC, 14-bit counter and a synchronization logic which can be set in a specific time mode which has been specifically defined to retrieve the information of the third dimension and single electron detection ability.

2 Results of the TimePix wafer tests at CERN

In collaboration with people from NIKHEF and Freiburg, we participated in the TimePix wafer tests, using the probing station at CERN, from September 2006 to September 2007. We established that the yield of useable chips from the 20 wafers from the first run (see Table 1) was 72.9 %.

		TimePix classification							Total	
Wafer n°	Location	A	B	C	D	E	F	Fnt	Wafer	A+B+C
8_A9FWR6X	CERN	31	27	6	11	12	20	0	107	**64**
9_ACFWR3X	CERN	42	15	13	10	9	17	1	107	**70**
10_A6FWQ5X	CERN	40	27	7	12	11	9	1	107	**74**
11_ATFWTLX	CERN	54	18	7	6	14	8	0	107	**79**
12_ASFWTMX	CERN	45	21	7	2	18	13	1	107	**73**
13_ARFWTNX	CERN	15	18	14	27	17	16	0	107	**47**
14_A5FWQTX	Diced	44	26	3	6	8	20	0	107	**73**
15_AQFWTPX	VTT	55	20	10	6	9	7	0	107	**85**
16_GX11ILX	CERN	44	27	8	10	13	5	0	107	**79**
17_G111GIX	CERN	41	31	8	7	14	6	0	107	**80**
18_GG11G3X	CERN	58	26	5	4	9	5	0	107	**89**
19_GF11G4X	CERN	49	30	9	6	9	4	0	107	**88**
20_GV11INX	CERN	51	23	15	13	3	2	0	107	**89**
21_GV11GPX	CERN	49	27	8	9	9	5	0	107	**84**
22_GZ11H2X	CERN	48	25	9	7	14	4	0	107	**82**
23_GU11H7X	CERN	58	26	2	3	12	6	0	107	**86**
24_GY11IKX	CERN	47	23	8	6	18	5	0	107	**78**
25_GW11H5X	CERN	46	18	8	15	2	18	0	107	**72**
26_GS11H9X	CERN	35	39	7	8	11	7	0	107	**81**
27_GH11G2X	CERN	56	27	5	4	13	2	0	107	**88**
TOTAL		**908**	**494**	**159**	172	225	179	3	**2140**	**1561**
(%)		42.4	23.1	7.4	8.0	10.5	8.4	0.1	100	**72.9**

Table 1 – Results of the tests are summarized in function of the chip quality (A: good, B: one dead column, C: 2 dead columns, D: > 2 dead columns, E & F: bad chip, Fnt: not tested). The yield of useable chips is 72.9 %.

3 Digital diagnostic micro-TPC

3.1 Description

In order to validate the concept we built a small aluminium chamber with a Micromegas mesh placed above the PCB of Medipix2/TimePix readout chip. Figure 1 shows the structure of the

field cage (2 cm × 2 cm × 6 cm) mounted on a frame which holds a Micomegas mesh on top the chip. The field cage is a folded kapton with 15 strips (4 mm pitch and 3 mm width), the connections between each made by 1 MΩ resistors to provide an uniform E-field. We designed also a specific 50 µm gap Micromegas mesh with a hole pitch of 55 µm and a pillar pitch of 19x55 µm to minimize the Moiré effect seen before using standard mesh.
In order to protect the chip against destructive sparks a 20 µm thick high-resistive a-SI:H layer [4] was deposited on top of the chip covering a 2 cm² surface.

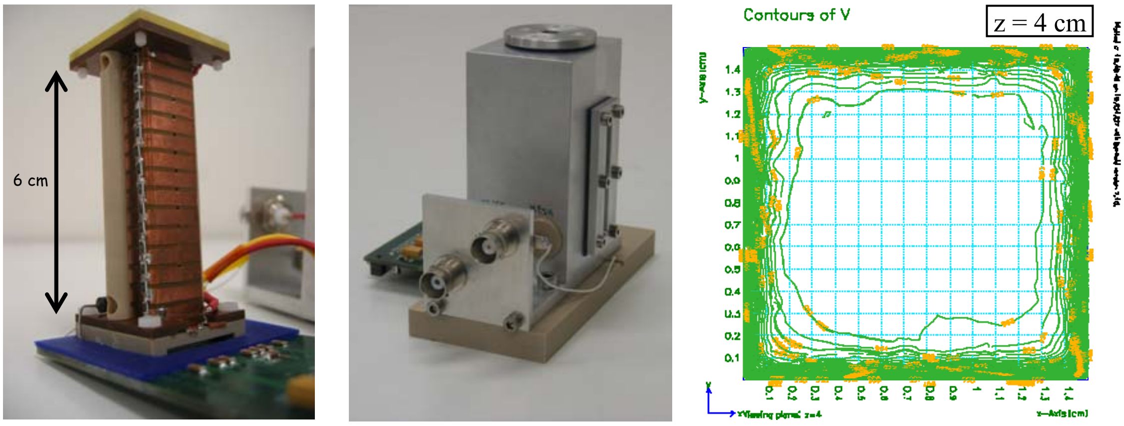

Figure 1 – Field cage (on the left) a 6 cm drift length placed on the TimePix chip inside a small aluminium chamber (on the middle) with two 4 µm thick mylar windows, one on its side and one on its top, transparent to β and X-rays sources. Simulations (on the right) show the homogeneity of field at 1 mm of the border corresponding to the surface limit where the Micromegas mesh is active.

3.2 First lights using X-rays source

We put a ^{55}Fe source on the top window and observed in Time mode the conversion into electrons of the source's 5.9 keV photons in the gas. Figure 2 illustrates our small TPC to be a demonstrator of the use of TimePix chips as digital readout for a TPC. Two photons have lost their energies and liberated about 220 electrons seen in the two clusters shifted in time and z.

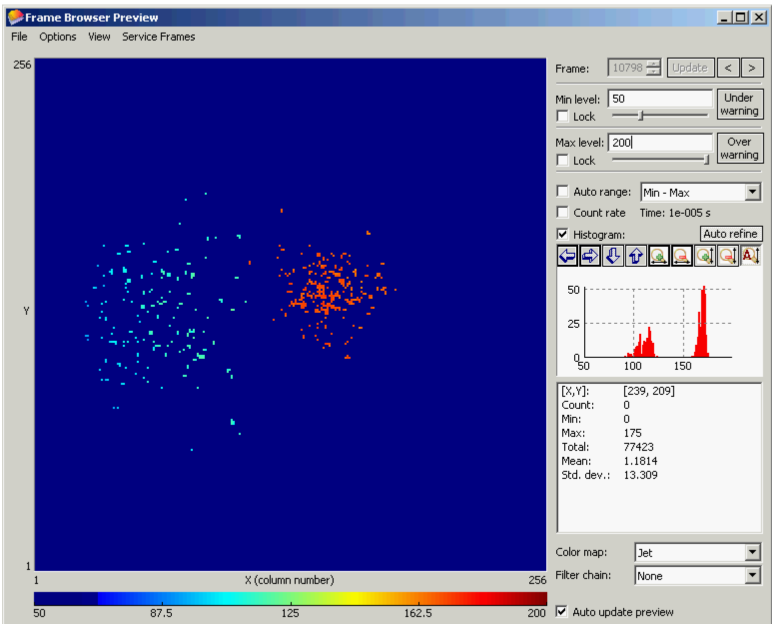

Figure 2 – Picture taken by Pixelman [5] of 2 electrons clusters converted in the gas chamber from 5.9 keV energy photons of an Iron-55 source at z = 6 cm. The colour codes the arrival time on the digital anode. We clearly see the electrons one by one.

4 Deliverable: panel for the ILC Large Prototype

The next stage is to build a 2 x 4 matrix of TimePix chips. We chose the InGrid [6] technology as Micromegas and the resistive layer for protection [4]. This larger pixelised anode, currently in construction, will provide electron by electron tracking and will demonstrate the possibility of integrating it to the ILC Large Prototype.

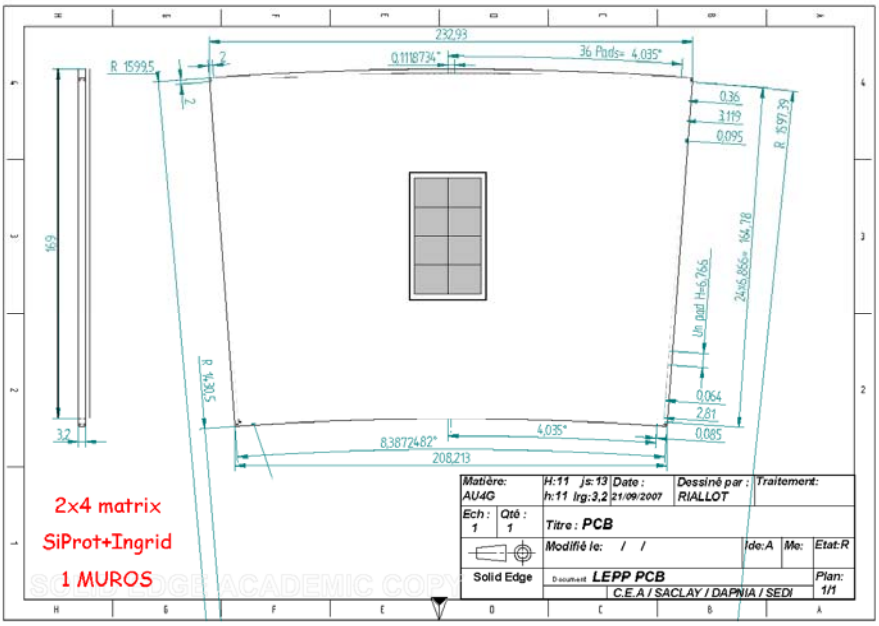

Figure 3 – Sketch of a PCB where is placed a 2 x 4 matrix of TimePix chips.

5 Conclusion

We successfully demonstrated that combining TimePix chips, Micromegas, and resistive layer technologies, for protection, is able to operate as a digital TPC sensitive to single electrons with ultimate spatial resolution. We are now ready to enlarge the surface to ~ 20 cm². We will continue to take data and work further on the analysis.

This small chamber is a fantastic tool to study gas properties. It also could be used for other applications thanks to its ability to give energy and directionality.

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