



## Status Report on TDC-based readout electronics for the LP TPC

A. Kaukher\*, O.Schäfer, H.Schröder, R.Wurth

*Institut für Physik, Universität Rostock, Germany*

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### Abstract

Within the EUDET JRA2 task TPC readout electronics based on time-to-digital converters is being constructed. The new readout electronics will operate with the Large Prototype TPC detector. The current status of the work is described in this note.

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\*Alexander.Kaukher@desy.de

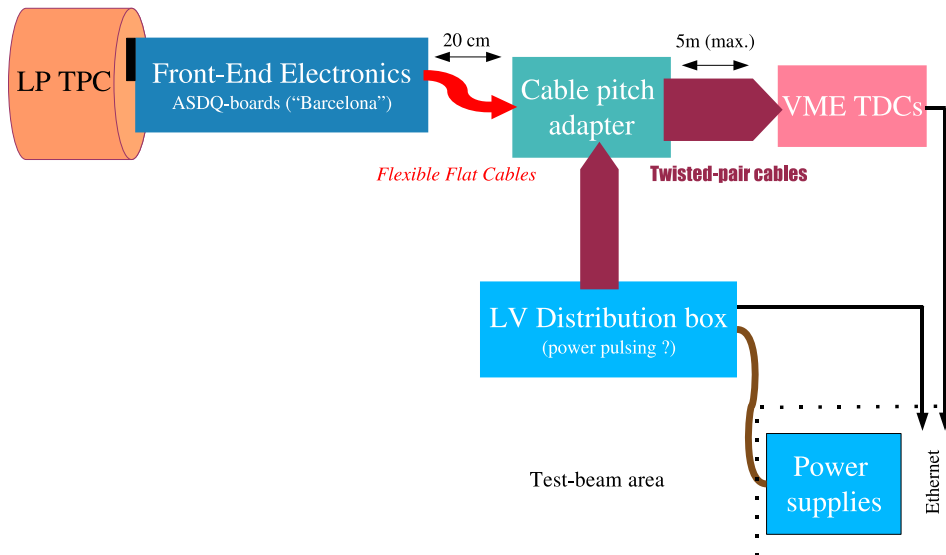


Figure 1: An overview of the readout system based on TDCs for the LP TPC.

## 1 Introduction

The development of the TDC-based readout electronics is carried out in the line of the Electronics Workpackage of the LCTPC Collaboration[1]. Time of arrival and charge of signals from TPC pads are measured with the help of a time-to-digital converter. The charge is measured indirectly, with help of a charge-to-time converter.

Within the EUDET project the readout electronics based on TDC is being build. At this stage readout electronics is being constructed using existing components. It is envisaged to develop a new compact and low power time-to-digital converter chip in the next stage of the project.

Main components of the readout system are the ASDQ chips and VME TDCs (v1190 from CAEN). Due to the cost of the multi-purpose TDC modules the number of channels will be limited to several hundred<sup>1</sup>.

## 2 TDC-based readout electronics: system overview

The overview of the readout system is given on Figure 1. The readout electronics has several components: Front-End Electronics (FEE) boards<sup>2</sup>, flat flexible cables (FFC), Pitch Adapter boards, twisted pair cables and VME TDC modules. The low voltage and control signals for FEE boards are supplied via 7-pair twisted pair cables from a low voltage distribution box and low voltage power supplies.

<sup>1</sup>Currently 5 TDC modules are available, 640 readout channels in total.

<sup>2</sup>Also called "Barcelona" boards.

## 2.1 Front-End Electronics boards

The FEE boards (“Barcelona” boards) will be installed directly on the endplate of the Large Prototype (LP) TPC. The “Barcelona” board is implemented as a thin ( $\sim 1$  mm) multilayer printed circuit board (PCB). The surface mounted components are placed on both sides of the PCB. Four ASDQ chips make up the 32 readout channels of a single board. Thresholds and other control signals are produced by a buffered digital-to-analogue converter, which is controlled remotely.

The width of the board is 30 mm. The final thickness of the assembled board, including PCB and electronic components on both sides, is estimated to be less than 4 mm.

The input connector is WR-40P-HF-HD-A1E from JAE (*Japan Aviation Electronics*). The pinout of the connector is the same as proposed in [3]. The design of the “Barcelona” board and the spacing of the connectors on the LP TPC endplate support the use of a padplane with size of pads as small as  $1 \times 5$  mm<sup>2</sup>. A padplane with smaller pads and a larger number of readout channels can be used as well, however this requires too tight placement of the connectors. Alternatively, a padplane with the same number of readout channels and two different pad sizes can be used: smaller pads in the “region-of-interest” and larger pads around.

The current status of the FEE boards: the design is finished and production details are being negotiated with the manufacturer. Most of the components are purchased, but the delivery of few components (data output connectors and few passive elements) is delayed, due to change of supplier.

## 2.2 Cabling

The FEE boards are connected to the Pitch Adapter with FFC cables. The length of these cables is fixed to 21 cm. The cable length defines the maximal distance between Pitch Adapter and “Barcelona” board.

The Pitch Adapter is a simple PCB board equipped with connectors for FFC cables (0.5 mm pitch) and connectors for twisted pair cables (1.27 mm pitch).

Twisted pair cables of 5 m length are available. The optimal length of the cables has to be found, in order to avoid mutual effects of the magnetic field of the PCMAG[5] and the VME crate with the TDCs. The TDC-side connectors will be installed on the twisted pair cables as soon as details of the TPC support structure are known.

Status of the cabling: complete set of data cables is available.

## 2.3 VME crate and DAQ system

A standard VME crate hosts the TDC modules. Regarding stray magnetic field of the PCMAG, the twisted pair cable length and the required degrees of freedom of the PCMAG and the LP TPC movement, the VME crate will be placed in the vicinity of the LP TPC.

The data transmission from the TDCs is performed with the help of the integrated VME controller of the VME CPU. The raw data will be transmitted over the Ethernet network to a DAQ PC, which will format data into LCIO files. The prototype of the data acquisition software (only VME-side) has been tested.

Status of the DAQ: a VME crate and 5 TDCs are available. The VME-side DAQ software is in prototyping stage.

## **2.4 Low voltage subsystem**

Low Voltage (LV) power and control signals are distributed with a printed circuit board – the LV distribution board. Each FEE board is connected individually to this board. The LV distribution board carries a FOX-controller – a single board Linux system. The FOX-controller is used to distribute required (digital) control signals. Finally, all required parameters of the FEE boards can be controlled over the Ethernet network with help of the FOX-board. Voltages on the LV distribution board will be monitored as well.

During the operation of the LP TPC[2] in the testbeam in August 2008, it is foreseen to install LV power supplies outside of the testbeam area.

Status of the LV distribution subsystem: FOX-board, LV power supplies and cables are available, the LV distribution board is in development stage.

## **3 Test equipment**

### **3.1 Chip tester**

A specially designed Chip Tester board will be used to select ASDQ chips before installing them on the FEE boards. The design of the Chip tester includes several design features of the “Barcelona” board. Individual channels of the chips can be tested and ASDQ chips with similar threshold uniformity will be grouped for installation on a single “Barcelona” board.

Status: The Chip tester is in assembly process.

### **3.2 UNIMOCS detector**

UNIMOCS[4] - a simple triple GEM setup, with a drift length of 3 cm. The setup can be considered as a tiny TPC without a field cage. The purpose of the setup is to test readout electronics with GEM signals and in this case the drift field homogeneity is of no concern. The main goal – evaluate the noise performance of the multi-channel readout electronics.

The detector has been tested with previously developed readout electronics (“Athena” boards) based on the ASDQ chip. The padplane of the UNIMOCS currently has 112 pads (in 7 rows) with sizes of  $2.54 \times 14 \text{ mm}^2$ . The pad size is due to the size of the “Athena” boards.

The stable operation of the chamber and good data quality during the operation with a (usual) cosmic ray setup allowed to perform various tests with TDC-based readout electronics. In the data driven mode<sup>3</sup> of the TDC operation, a coincidence signal from the scintillator counters is not required for the acquisition of data, but still was recorded by the TDC simultaneously with the signals from “Athena” boards. Tracks from cosmic particles with zenith angles beyond the acceptance of the scintillator counters were recorded. As a result - some inefficiency of the scintillator counters was observed.

Owing to modular design of the UNIMOCS, a new padplane can be easily integrated. One such padplane is ready to operate with four “Barcelona” boards. In order to be able to compare the results with previous measurements with “Athena” boards, the padplane has been designed with 6 rows of pads of the size  $2.54 \times 14 \text{ mm}^2$  and one row with pads of size  $1.27 \times 14 \text{ mm}^2$ .

Status: the UNIMOCS test chamber is ready and operational.

## 4 Integration of the Readout Electronics with the LP TPC

In order to complete integration of the readout electronics and the LP TPC, their mechanical and electrical interfaces have to be considered

The FEE boards to be supported with a light-weight support structure, the design of which is being elaborated. The weight of a single assembled “Barcelona” board is estimated to be less than 30 g.

The twisted pair cables are very heavy, and have to be supported together with the Pitch Adapter boards with the help of an external support structure, detached from the LP TPC. In this way no excessive additional load is applied to the LP TPC. The only possibility to reduce total weight of the twisted pair cables is to shorten them.

The choice of the high density connections[3] has established the interface between a padplane of the LP TPC and the FEE boards. Electrical connections in the overall system (readout electronics, LP TPC HV system, PCMAG, Motorised support structure, Laser system(?),...) are of high priority and shall be understood as soon as possible, in order to ensure good data quality and safe operation.

The power dissipation of the readout electronics is estimated to be 25 W for 640 readout channels. In order to remove most of this heat from the LP TPC endplate, air cooling

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<sup>3</sup>also “continuous operation”, or triggerless mode.

is foreseen.

During the operation of the LP TPC in the cosmic ray setup (Spring 2008), a simple trigger signal will be available for the TDC-based readout electronics. Testbeam operation of the LP TPC with other detectors ([7],[8]) will require the use of a Trigger Logic Unit (TLU)[6]. The electrical interface and the communication protocol are prescribed and development of an interfacing hardware component to be considered.

The output data format of the DAQ software of the TPC readout electronics is defined by the LCIO format. It is considered to use one of the already existing DAQ systems and one of the candidates is DOOCS (Distributed Object Oriented Control System)[9]. This control system is used in the FLASH Facility at DESY and is being considered by JRA3[10] for use with calorimeter detectors.

## 5 Summary

TPC readout electronics with several hundred readout channels is being constructed. At this stage only already existing components are used. Most of the hardware components are available, except the FEE boards, the Pitch Adapter boards and the LV distribution box. The VME-side DAQ software is in prototyping stage. Few components are missing and expected to arrive at the end of February 2008. The complete readout electronics is expected to be ready by February/March 2008. One of the crucial issues to be defined is the support structure of the FEE boards and cables.

## Acknowledgement

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