JRA3 DAQ Status - Munich

M. Warren[1], on behalf of EUDET-JRA3-DAQ groups:
Cambridge University
Imperial College London
University of Manchester
Royal Holloway, University of London
University College London

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Abstract

Status of the emerging EUDET JRA3 DAQ is presented. Current thinking in terms of overall design and connection topology using commercial off the shelf (COTS) components is detailed. Latest development in the off-detector receiver (ODR) is detailed.

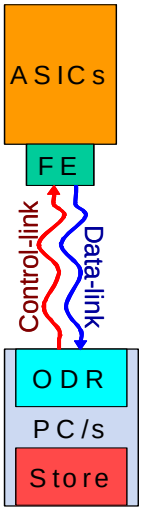
[1] University College London

Introduction

Although JRA3 DAQ is in its infancy, it builds upon a well established DAQ used by the CALICE collaboration. Much of our effort involves using commercial equipment where bespoke hardware was used before. It follows, therefore, that the central component of this package is the development of detector readout hardware and interfaces.
We have specified and purchased a prototyping card that will facilitate the development of both ends of the detector to PC link, as well as later work on transferring clock and control signals in the opposite direction.

The conceptual DAQ can be divided into 6 parts;

1. Front-End interface to sub-detector (FE)
2. Data-link (FE to Off-Detector Receiver)
3. Off-Detector Receiver (ODR) card
4. Control data-link (Clock, Control to FE)
5. Data Store
6. Software



The commercial hardware constraint allows for a simplified design process. Although much of the design detailed here is no more than a block diagram, the use of real-world components will hopefully allow development of the first system prototype to proceed efficiently.

DAQ Goals

- Use commercial components where possible:
  - Readout links use standard connectors and protocols
  - Fibre-optic links
  - PCI-Express readout board hosted in a standard PCs
- Modular, general purpose design:
  - Generic readout board for all users
  - Detector specific interfaces as plug-in modules
  - Other ‘bespoke’ functionality in firmware
- Front end ‘Control-link’ attempts to use commercial hardware too
  - Extract ‘fast’ signals from commercial signalling
  - Reconfigure FE firmware using control-link
- Software general purpose for possible EUDET wide use
  - Use plug-ins for specific detectors and environments
- Failure protection (fail-over)
  - PCs not reliable – reroute signals on-the-fly

Component Detail

1.1 Front End (FE) Interface

The FE is tasked with interfacing directly with sub-detector ASICs. It is assumed to be an FPGA for maximum flexibility. Data is collected (or accepted) from the ASICs by the FE, buffered (if needed) and packaged and transmitted off-detector. The FE will be responsible for formatting it in the desired data link protocol (S-Link, Ethernet, raw etc.)
The FE also receives configuration signals from off-detector, and packages and distributes them as needed to the ASICs.

As the detector slabs will be constructed from shorter sections, the FE assumes to connect at the end of the slab. Work is already underway at Cambridge[i] to mimic the digital operation of the ECAL FE ASICs. This will provide a first attempt at defining and ASIC/FE interface.

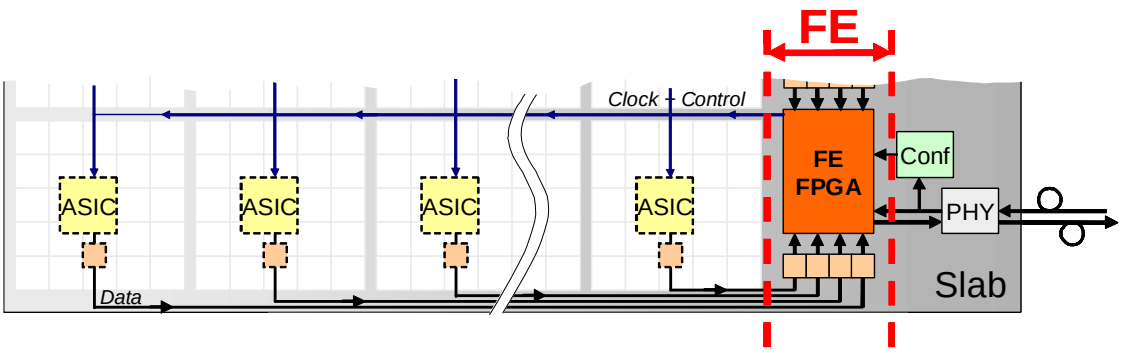


Figure 1. FE in context of an ECAL 'slab'

1.2 Data-link

The data-link represents the physical link (regardless of protocol) from FE to off-detector, covering the path of data from the FE FPGA to a off-detector FPGA. It is presumed to be fibre-optic, and makes use of commercial interfaces and protocols; e.g. HSSDC2, SFP (see Figure 2) using Ethernet or S-Link protocols. They are expected to operate above 1Gbit.
Using FPGA's with manufacturer provided firmware for their gigabit transceivers allows for the whole link to be built using standard components. It can also be modelled and tested the off detector receiver.

HSSDC2 SFP

Figure 2. Giga-bit connecter formats: HSSCD2 for (mainly) copper, SFP for fibre-optic

1.3 Off-Detector Receiver (ODR)

Data from the FE is collected by the Off-Detector Receiver cards. These cards are hosted by a PC with PCI-Express bus. The goal is to keep the hardware as generic as possible, allowing for use on multiple (sub-)detectors. Conceptually each card consists of a large FPGA (with embedded CPUs, if needed), some buffer RAM and sites for attaching data and control link hardware as needed by those interfaces. It is envisaged that cards could host FE firmware (and similar link hardware) to facilitate testing without real FE's (FE emulation).
Provision is also made for interfacing with fast-control (clock and trigger) sources, as well as transmitting these signals to the FE. The ODR concept is shown in Figure 3.

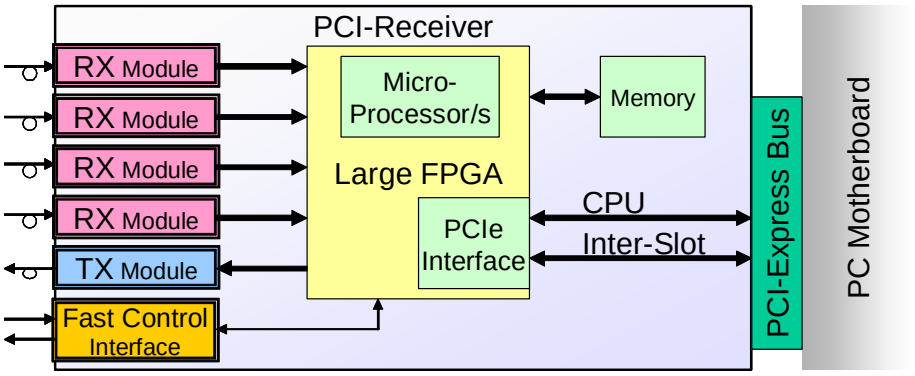


Figure 3. Conceptual design of the Off-Detector Receiver

We have found a development board that suits our requirements extremely well: the *PLDA XpressFX100* [ii] (shown in Figure 4). It is supplied with a PCI-Express firmware core, that has allowed us to side-step that development work.

The board is based on a Xilinx Virtex 4 FX100 FPGA, which has extensive logic resources as well as a pair of 400MHz CPUs. Two pairs of gigabit interfaces are already fitted, with room to add four more via plug-in modules. It supports 8x PCI-Express (a bandwidth of 10Gbit), and has 128Mbyte of DDR2 RAM onboard. All round this seems a very powerful and versatile board, suitable for test-beam use.

It is envisaged that the firmware developed for this board will be portable enough to be used on custom boards if needed.

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Figure 4. XpressFX prototyping and development board.

The ODR is a central component of the DAQ the focus of our activity at present. Cambridge, Manchester, RHUL, UCL have a board each, along with a hardware development PC. A basic Linux driver has been written for SLC4 and we can communicate with the board (e.g PCI-Express core is working).

Separately an Ethernet interface is working, with the only outstanding code for a first-order receiver being a DDR2 memory controller, which is under active development. We expect to complete a test data transfer system by end of year.

1.4 Control-Link (Clock and Control)

The control-link transports configuration data to the FE, as well as clock and timing synchronisation signals. For data it uses exactly the same hardware as the data-link but in the opposite direction. Timing synchronisation poses some additional challenges; we will attempt to recover a machine clock and synchronising signals from the link electronics, but this might be difficult on the test-beam schedule. As a fall-back, discrete interfaces for clock, trigger and possibly power-pulsing will be provided. Figure 5 shows the concept.

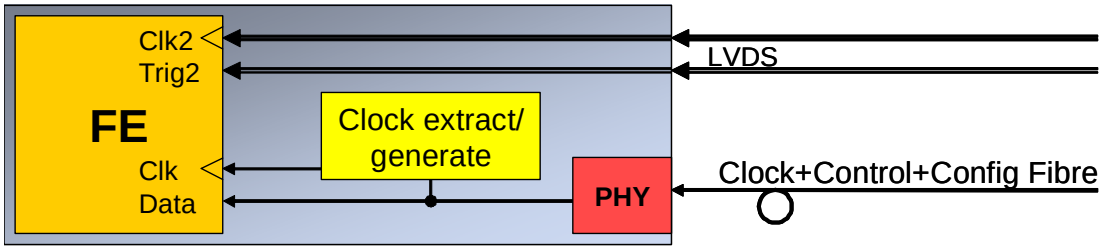

Figure 5. Control link concept.

1.5 Datastore and Software

Data needs to be stored for processing. It is unlikely that the volume will exceed bandwidth and storage limits at this stage, so the first-order prototype will write it directly to disc. The data will then be available to higher level DAQ software via e.g. NFS. If data volume increases it could be zipped in firmware.

Higher level software is in the very early design phase and will likely be derived from the existing CALICE structure where possible, although detector configuration and usage models need to be finalised before work begins.

Conclusion

Work has started on the DAQ, with the primary being focus on the read-out hardware, which is progressing well. As detector specifics and areas of use stabilise development will expand to incorporate these.

Acknowledgement

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References

[i] Study of data paths on ECAL Slab
http://ilcagenda.cern.ch/materialDisplay.py?contribId=71&sessionId=4&materialId=slides&confId=737

[ii] PLDA PCI Express XpressFX Development Board
http://www.plda.com/products/board_pcie_fx.php