EUDET-Memo-2006-02

Status of the R&D Program for a Read-Out System based on Time to Digital Converters for the LP-TPC within EUDET

A. Kaukher, O. Schäfer, H. Schröder, R. Wurth*

December 4, 2006

Abstract

The status of the R&D work for the TDC based read-out system for EUDET's Large Prototype TPC is presented. Problems arising from the choice of the pad size are shown and alternative solutions are discussed.

*University of Rostock, Germany

1 Introduction

The quantities read out from a Time Projection Chamber (TPC) comprise the spacial information of an incoming charge cloud (one of them, the z-coordinate, encoded in the drift time) and the charge itself. It is the task of the read-out system to extract these quantities from the TPC.
In the read-out method proposed by the University of Rostock group for the Large Prototype TPC (LP-TPC; [1]) the charge is first measured in an analogue step and encoded into an intermediate (rectangular) pulse of a length corresponding to the charge. This intermediate signal is afterwards digitized by a Time to Digital Converter – TDC. The Rostock group examines this aproach using TDCs with existing technology.
In order to develop a read-out system for the LP-TPC the mechanical design of the electronics has to be considered, which is essentialy driven by the dimensions given of the pad plane and pads. For the LP-TPC the pad size was set to 1 mm × 4 mm. A typical readout- or preamplifier board of e. g. 32 channels must therefore not exceed 32 mm in width and 4 mm in thickness respectively. A suitable interface for these conditions using WR-40S connectors was proposed by the University of Lund (Fig. 1). However, within these rather small dimensions a proper mechanical support for the boards and the attached cables has to be realized, as well as electrical shielding and cooling.

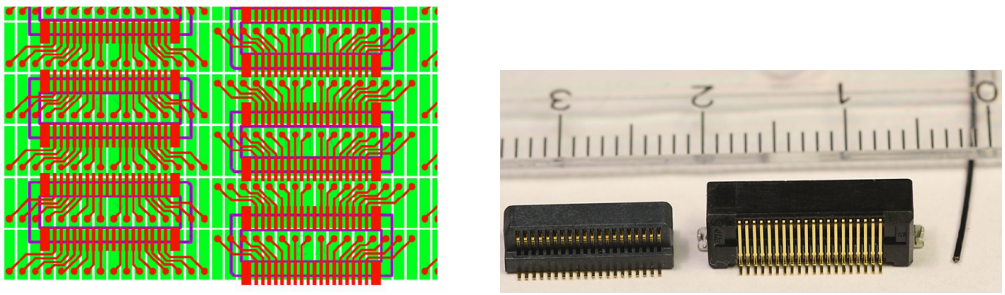
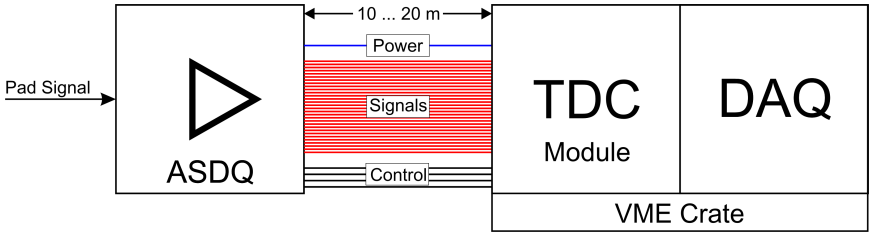


Figure 1: Interface to the padplane and WR-40S connectors (L. Jönsson, University of Lund). In green, pads of 1 mm × 4 mm, violet frames show the outline of the connectors and red the conductor paths.

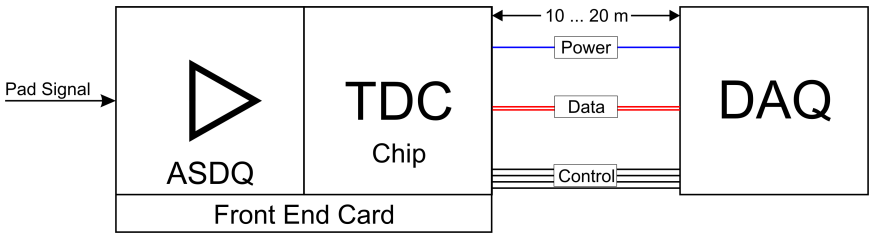
2 Planned Setup

The TDC based read-out system proposed for EUDETs LP-TPC originates from earlier research work described in [2]. That setup consisted of preamplifier boards carrying two ASDQ chips (Amplifier, Shaper, Discriminator, Q = Charge measurement; for detailed information see [3]) being plugged directly onto the backside of the padplane. From there the intermediate signals generated by the ASDQs were sent via cable (16 pairs) and a signal conversion step to a VME TDC-module[1] for digitization. They were then converted to the final read-out data format by the DAQ system.

[1] CAEN, Model V767, 128 Channel Multihit TDC



(a) Coventional Setup with CAENTDC Modules



(b) Compact Setup with TDC Chip on Front End Card (FEC)

Figure 2: Tests

The original idea was to simply scale this setup to the larger number (several hundred) of channels (Fig. 2a). However, new problems arise for this *conventional setup*, e. g. cabling the pads being increased both in number and density. Solutions to this problem are being investigated.
An alternative idea forsees to place the ASDQ chips and a TDC chip on the very same board (Front End Card – FEC). From here only a serial data connection (2 pairs), a few control lines and a power line are needed to connect with the DAQ system (Fig. 2b). The TDC chips have the additional advantage of much lower cost per channel compared to the conventional setup and thus many more channels could be equipped. On the other hand additional hardware and software development has to be done for this *compact setup*. Several new problems are adressed by following this concept like the operability of analogue and digital circuitry if installed on the very same board. The development of a DAQ system for this setup is another one. These are currently being studied. For this reason the safer, conventional setup is followed as a backup – all the more since newer TDC modules[2] don't require the signal conversion step any longer.

2.1 ASDQs

A central part of the Rostock setups is the ASDQ chip. As stated above, this chip comprises a preamplifier, a shaper, a discriminator and a charge to time convertion as a feature of the discriminator. The chip is capable of measuring charges within 0.34 … 120 fC at a precision of about 10 %. It encodes the charge of the signal into a digital pulse of corresponding length. The pulse is provided as a differential signal (LVDS) at the output.

[2] CAEN, Model V1190A, 128 Channel Multihit TDC

One ASDQ chip unites eight channels on a 5.4 mm × 3.9 mm chip surface inside a TQFP package of 12 mm × 12 mm (including pins). The power dissipation is 40 mW/channel. In total 200 ASDQ chips have been obtained from the University of Pennsylvania.

2.2 TDCs

Having the charge measured and encoded into the intermediate pulse, the next step is to measure the start time and length of the pulse and digitize these measurements with a Time to Digital Converter.
As indicated above there are commercial TDC modules available, as is the TDC chip being used in the CAEN V1190 A module. This High Performance TDC (HPTDC; [4]), which is produced at CERN, is a multi purpose TDC with selectable time binning within a range of 24 ps ... 781 ps. For all the Rostock setups the slowest time binning of 781 ps is sufficient, as is the resulting maximum measuring range of 105 μs. This corresponds to about 4.20 m drift lenght at 4 $\frac{\text{cm}}{\mu\text{s}}$ drift speed (compared to 60 cm length of the LP-TPC).
Up to now, one V767 and two V1190A modules from CAEN, as well as five HPTDC samples have been procured.

2.3 DAQ System

The DAQ system for the *conventional setup* is merely a program running on the VME CPU. As a single TDC module provides a data output where every read-out channel has an unique number, the DAQ software has to provide channel remapping in order to efficiently build an event from multiple TDCs. Two possible remapping solutions are under investigation. Firstly an additional TDC VME module ID can be encoded into the TDC number. This scheme extends the usable number of channels from 512 to 4096. Secondly an additional TDC module header could be inserted into the data stream, thus extending the usable number of TDC modules from 4 to 2^{12}. The latter method is more complicated and only necessary if the read-out electronics has to be scaled to more than 4096 channels.
The data is stored on a local VME disk. In order to increase the CPU data throughput, the data stored locally has a proprietary format without conversion into the LCIO format. Optionally data can be sent over the network for online monitoring or to remote storage where additional format conversion can take place.
The DAQ system for the *compact setup* includes hardware and software parts. A commercially available solution can be used, for example Ben-One$^{\text{TM}}$ – a PCI FPGA computing card from Nallatech. The data from the HPTDC chip is transfered via twisted pair cable to the board. Only two LVDS links are necessary to communicate with a single HPTDC chip. The software part is to be programmed in the FPGA core and performs the same task as for the conventional setup.

3 Test Equipment

In order to study signal integrity of the ASDQ and the HPTDC an *evaluation board* will be designed. For testing the interplay of the electronics with a chamber, the construction of a small test chamber has been started as well.

3.1 Evaluation Board

The board will carry four ASDQ chips and one HPTDC. The design rules of the evaluation board will be the same as for the final (compact) setup, but without its strong requirements on the size of the board. The evaluation board will be used not only to study the mutual performance of the analogue and digital components on the board, but also as a development platform for the compact DAQ system.

3.2 Test Chamber

For the stand alone testing of the read-out system separated from the LP-TPC a small test chamber is currently being designed. It will provide a triple GEM amplification structure and exchangeable padplanes. The test chamber is based on a modular concept. It was found by electrostatic simulation that for small drift distances the drift field is sufficiently homogeneous. By providing an individual barrel section each for the cathode, drift region and read-out structure, all parts can be easily accessed and possible future changes don't neccessarily affect the whole chamber. All voltages can be connected on the outside, thus the design of the power supply can be realized independently from the chamber. The chamber is designed for maximum potentials of 6 kV to 10 kV – depending on the gas and pressure.

4 Conclusion

Main components of the two setups have already been purchased: 200 ASDQs, 5 HPTDC-Samples, 1 Model V767, and 2 Model V1190A CAEN Multihit TDC Modules. Currently the test chamber is being designed to the manufacturing level, as is the preamplifier board (redesign for new pad geometry). Both are expected to be available by April 2007. The cabling for the conventional setup is under investigation and for the integrated solution the problem of the DAQ system is under study.
In general a first TDC based read-out system for the LP-TPC, as described in the EUDET proposal ([5]), is from the current point of view most likely to be ready by the end of 2007. For further information please contact O. Schäfer, e-mail address: oliver.schaefer@desy.de.

Acknowledgement

This work is supported by the Commission of the European Communities under the 6th Framework Programme "Structuring the European Research Area", contract number RII3-026126.

References

[1] Information about ongoing LP-TPC R&D can be found at:
`http://alephwww.mppmu.mpg.de/~settles/tpc/lp/lp.html`

[2] A.Kaukher, "A study of read-out electronics based on TDC for the international linear collider TPC detector", IEEE Trans. Nucl. Sci. 53 (2006) 749.

[3] "The ASDQ ASIC for the Front End Electronics of the COT", W. Bokhari et al.
http://penn01.fnal.gov/~cot/

[4] HPTDC Documentation can be found at:
http://tdc.web.cern.ch/tdc/hptdc/hptdc.htm

[5] EUDET Proposal "Detector R&D towards the International Linear Collider" at:
http://www.eudet.org