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GOSSIPO 3 - A front-end pixel chip prototype for readout of MPGDs

C. Brezina*, K. Desch*, H. van der Graaf†, V. Gromov†, R. Kluit†, A. Kruth*, F. Zappon†

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Abstract

NIKHEF (Amsterdam) and the University of Bonn made a joint effort to develop a front-end pixel chip prototype, named GOSSIPO-3, in IBM 130 nm standard CMOS technology for the readout of Micro Pattern Gas Detectors (MPGDs).

GOSSIPO-3 targets future highly granulated (60x60 µm^2 per pixel) readout chips. The prototype consists of the analogue readout chain and the logic needed in a TPC application. This includes a high precision time to digital converter (TDC) with a sampling resolution of 1.7 ns and a dynamic range of 102 µs.

The charge deposited in each pixel is measured using the time over threshold (ToT) technique in the dynamic range from 400 e^- to 28000 e^- with a standard deviation of 200 e^-.

The circuitry is optimized for a low power consumption of roughly 100 $\frac{\mathrm{mW}}{\mathrm{cm}^2}$.

*University Bonn, Germany
†NIKHEF, Amsterdam, Netherlands

1 Introduction

Due to many favorable properties it is very attractive to make use of MPGDs in particle physics. Especially, the high spatial resolution, the radiation hardness and the inherent low material budget are desirable.
Currently, NIKHEF and the University of Bonn are exploring the capabilities of the Timepix chip [1] in MPGDs (e.g. [2]). Although the prospects opened by the Timepix IC are outstanding it has been found that the time measurement still offers room for improvement. Also the need to choose one out of the four possible operating modes (timing, ToT, single hit, Medipix mode) limits usability.
The development of the GOSSIPO-2 chip [3] in 2007 at NIKHEF gave first insights to the design of high resolution TDCs incorporated into every pixel. The main goal of the recent GOSSIPO-3 prototype is to optimize the design of the building blocks for a future IC dedicated to the readout of MPGDs.

2 The Pixel

As figure 1 shows the pixel in GOSSIPO-3 contains a charge sensitive preamplifier (CSA) with a discriminator connected to its output. This generates the logical hit signal when the threshold level has been reached. The pixel logic includes a local fast oscillator, a fast, a slow and a ToT counter (4 bits, 12 bits and 8 bits respectively).
In the time measuring mode, depicted in figure 2, the hit signal starts the local fast oscillator and the fast counting, as well as the ToT counter. The fast counting and the local oscillator are stopped by the first rising edge of the chip-wide slow clock (40 MHz). This triggers also the start of the slow counter. The slow counter then runs until the trigger signal occurs. The trigger has to be synchronized to the 40 MHz clock. The time between the hit and the trigger signal may be calculated from the number of fast clock cycles and the number of slow clock cycles: $t = N_{\text{fast}} \cdot f_{\text{fast}} + N_{\text{slow}} \cdot f_{\text{slow}}$.

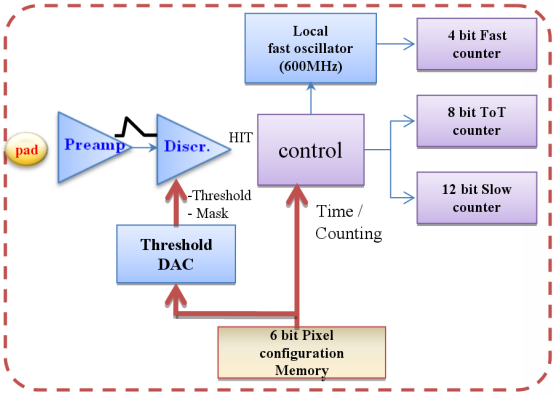

Figure 1: Block diagram of one pixel.

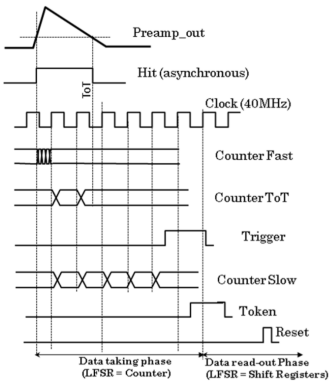

Figure 2: Timing diagram of operation in time mode

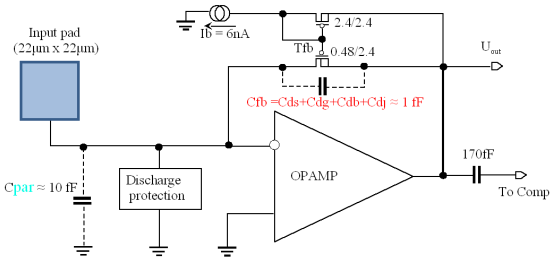

Figure 3: Front-end circuit

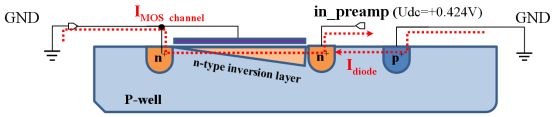

Figure 4: Layout of the discharge protection device

The precision of the time measurement is given by the fast oscillator frequency of 580 MHz (T = 1.7 ns). If the stability and synchronicity of the trigger and the slow clock are not guaranteed this may degrade the accuracy. The dynamic range is determined by the counter depth of the slow counter. At 40 MHz 12 bits correspond to 102 µs.
The ToT counter determines the time the hit signal is high by counting the number of elapsed full slow clock cycles. This value depends linearly on the charge deposited on the CSA input. The linearity holds up to 28000 e^- at the CSA input. The accuracy of this measurement is limited by the noise-related time jitter on the falling edge on the signal of the CSA's output. It is simulated to be roughly 200 e^-.
In an alternative counting mode all counters are combined to one 24 bit counter. This mode allows the determination of the number of hits on the pixel between reset and the trigger signal.
For the readout of the stored values the flip flops of the counters are reconfigured to a 24 bit shift register by the token signal. The data is then shifted out of the chip using the slow clock. After readout the counters are reset.

3 The Front-end

Since the circuits on GOSSIPO-3 are designed for readout of MPGDs there is no need for a leakage current compensation. The input circuitry shown in figure 3 is optimized for operation with a very low input capacitance of 10 fF as common in gaseous detectors. In order to achieve high charge conversion gains ($\propto \frac{1}{C_{\mathrm{fb}}}$) it is necessary to keep the feedback capacitance as small as possible. Therefore the feedback capacitance is not implemented as a standard capacitor but as the parasitic capacitance of the constant current feedback transistor. The chosen feedback transistor introduces a capacitance of 1 fF and has a resistance of 30 MΩ if no signal is present.
Simulations predict a low noise of $\sigma = 70\ e^-$ while only a few µW are consumed. An on-pixel DAC reduces the channel to channel threshold spread down to $\sigma = 5\ e^-$
The input of the CSA is protected from high-voltage breakdowns of the gas amplification stage by a protection device consisting of a n-channel transistor (see figure 4). The inversion layer below the gate and the diode in the substrate form two channels, which are draining the discharge current.

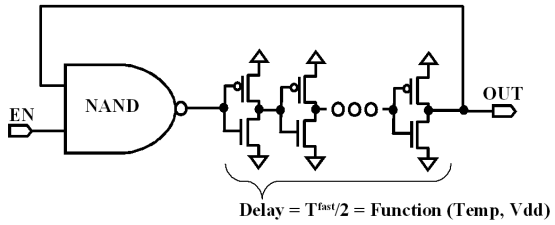

Figure 5: The local fast oscillator circuit

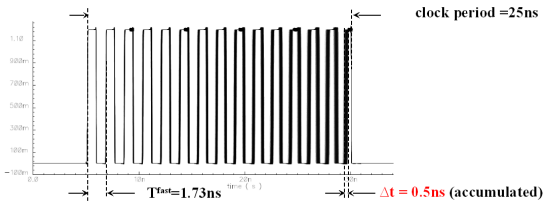

Figure 6: Pixel to pixel mismatch on one die (Monte Carlo simulation)

4 Local Fast Oscillator circuit

The central building block of the high precision TDC is the local fast oscillator (LFO) in each pixel. This LFO consist of a NAND gate and several daisy-chained logic inverters as shown in figure 5. The NAND gate allows en-/disabling of the circuit.
The oscillation frequency is determined by the delay through the daisy chain. Based on simulation the LFO is designed to run at a frequency of 580 MHz, this means that the leading edge of the slow clock (40 MHz) can be determined with an precision of 1.7 ns. The fast clock signal is generated locally and only for a short time period when the pixel is hit. Therefore there is no need to distribute the fast clock in the pixel array. This strongly reduces power consumption and crosstalk.
As expected the frequency of the LFO is a function of temperature ($0.2\frac{\%}{\mathrm{K}}$) and supply voltage ($-0.12\frac{\%}{\mathrm{mV}}$). Additionally the LFO frequency of different pixels will depend on process variations. Monte Carlo simulations showed that the frequency mismatch between the pixels on one die will be well below one TDC bin, even if the LFOs are active for a complete slow clock cycle (see figure 6). Hence, this mismatch can be negelected. Nevertheless the frequency spread between different dies is much larger. The wafer to wafer mismatch is compensated using the linear dependency between supply voltage and oscillation frequency by varying the LFO supply voltage on each chip. This allows to tune different chips to run on the same LFO frequency.
Supply voltage regulation is done by an on-chip low drop out regulator (LDO). The output voltage can be chosen between 0.6 V and 1.1 V by adjusting the reference voltage. This is sufficient to adjust the LFO's frequency to compensate all possible process variations. The LDO is designed to deliver up to 40 mA within a response time of one TDC bin. Although the LDO features a low equivalent serial resistance (less than 1 Ω) an off chip capacitor with a low equivalent series resistance needed to keep the output voltage stable on fast load changes.

5 Conclusion

GOSSIPO-3 is a prototype of building blocks to be used in a future front-end pixel chip for readout of MPGDs.
A TDC architecture is developed which allows time measurements with a precision of 1.7 ns over a dynamic range of 100 µs. Besides time mode the chip will feature a hit counting mode. The front-end circuitry in each pixel, featuring low noise and low power, is optimized for operation in MPGDs with low input capacitance. A compact device protects the input circuit from discharges.
To achieve frequency uniformity over different chips the local fast oscillators are frequency tuned via their supply voltage with a low drop out regulator.
The prototype chip was submitted to IBM for fabrication in December 2009, first measured results are expected in spring 2010.

Acknowledgment

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References

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