Beam tests of the FORTIS 4T pixel detector

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On behalf of the SPiDeR collaboration

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Abstract

In summer 2009 a beam test of the FORTIS four-transistor prototype pixel sensors was performed using the EUDET telescope. The status and first results are presented here.

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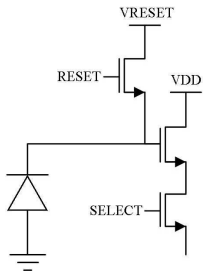

Figure 1: 3T CMOS pixel architecture

1 Scientific Background

1.1 Introduction

FORTIS (4T Test Image Sensor) is a prototype sensor containing up to thirteen variants on a 4T (four transistor) pixel architecture. There have been two iterations of the sensor; FORTIS 1.0 and FORTIS 1.1, where the latter contains an optimized process for low noise, and was also fabricated with and without a special deep p-well layer and on both standard and high resistivity substrates.

1.2 The 4T Pixel Architecture

The simplest pixel architecture present in CMOS image sensors is that of the 3T (three transistor) structure as shown in Figure 1. This pixel architecture consists of a diode, a reset transistor, a source follower transistor, and a row select transistor. The operation is as follows; first the diode is reset via the reset transistor, and then charge is collected. After a set "integration" time, the row select transistor is turned on and the signal from the pixel is read out via external readout circuitry. In this particular pixel, the diode is both the charge collection area and the node from which the signal is read within the pixel.

The 4T (four transistor) pixel architecture [1] is shown in Figure 2. The architecture contains three special elements compared to the 3T architecture; the transfer gate (TX) the floating diffusion node (FD), and a pinned photodiode. When the pinned photodiode is held at a certain voltage called the pinning voltage, the diode becomes fully depleted, allowing for a noiseless transfer. Charge will be collected by the pinned photodiode as long as the transfer gate is closed. When readout is ready to occur, the floating diffusion node is first reset to a value above the pinning voltage, and then the transfer gate is opened, which transfers all of the charge from the pinned photodiode and resets it simultaneously. Charge is therefore collected on the pinned photodiode, but transferred to and read out from the floating diffusion node, leading to separate nodes for these two functions.

There are two key benefits to the 4T pixel architecture due to the separated charge collection and readout nodes. The first is that low noise operation is obtainable via

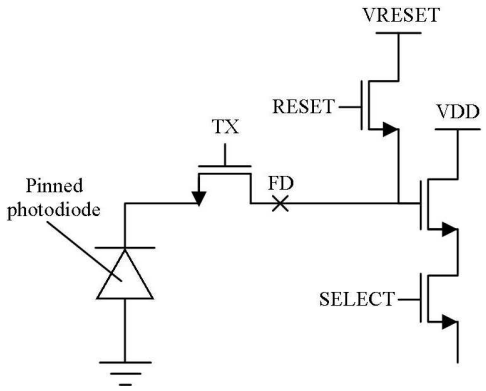

Figure 2: Advanced 4T CMOS pixel architecture

correlated double sampling. If a sample is done before and after the transfer gate is opened, the kTC noise, which is the main source of noise within a pixel, can be removed as it is correlated.
The second benefit of the 4T pixel architecture is that a high conversion gain can be obtained, which increases the sensitivity of the pixel to small amounts of charge. The conversion gain is given by $V = q/C$. If charge is transferred from the large diode capacitance (with a low conversion gain) to the smaller floating diffusion capacitance (with a higher conversion gain), then the sensitivity to small amounts of charge is increased.

1.3 The Sensors

FORTIS (4T Test Image Sensor) is a prototype sensor containing up to thirteen different variants on a 4T pixel architecture. There have been two iterations of this sensor; FORTIS 1.0, and FORTIS 1.1, where the latter explored the variants chosen for FORTIS 1.0 further via fabrication with and without the deep p-well layer, and on both standard and high resistivity substrates. FORTIS 1.1 also contains an optimized processing step to reduce the noise associated with the source follower.
FORTIS 1.0 and FORTIS 1.1 are shown in Figures 3 and 4.
Both sensors consist of the same simple readout architecture, with decoders for row and column access to focus on one pixel variant array at a time, and a simple analog output stage with sampling capacitors for storage of the reset and signal samples for correlated double sampling. In FORTIS 1.0, there were twelve different pixel variants, consisting of the original designs plus several geometric variations, such as variations in the size of the source follower transistor, the diode size, and the pixel pitch (6 μm, 15 μm, 30 μm and 45 μm). FORTIS 1.1 contains an extra pixel variant where four diodes have been combined at the floating diffusion node to investigate the effects of charge binning.

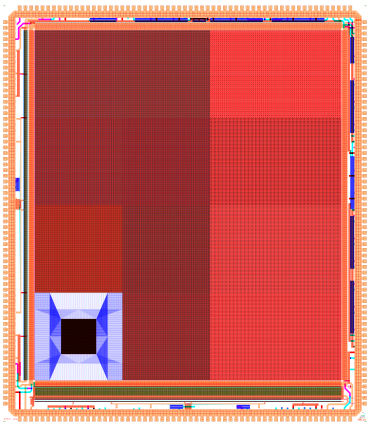

Figure 3: FORTIS 1.0

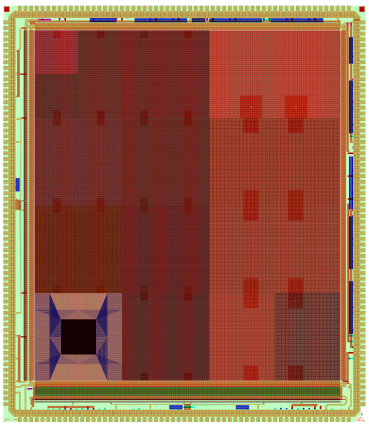

Figure 4: FORTIS 1.1

2 Test Results

The sensors have been extensively tested. The gain and noise were measured using the Photon Transfer Curve (PTC) technique, a laser scan was performed to measure the charge sharing between the pixels and finally the sensors were placed in a testbeam.

2.1 Gain and Noise measurements

For the characterization of the FORTIS sensor we first used the Photon Transfer Curve (PTC) technique. A Photon Transfer Curve is a plot of the dark corrected signal obtained from an image sensor against the noise for that signal. It is obtained via one of two methods; an intensity sweep, where the integration time is fixed and the light level/temperature is varied, or via an integration sweep, where the light level/temperature is fixed and the integration time is varied. At least two identical images are required for each step to obtain the PTC, and the mean signal and variance are taken from these two frames. The subtraction of the two frames to calculate the variance removes fixed pattern noise, leaving only read noise (which is the noise of interest for an image sensor) and shot noise. Shot noise scales with the square root of the signal, giving a characteristic 0.5 gradient when plotted on a log-log plot, and is the basis of the photon transfer curve [2].
Many parameters can be drawn from a photon transfer curve to give the basic characteristics of an image sensor. The noise is taken from the y-intercept of the graph (i.e. the noise for 0 signal). The gain is taken from the x-intercept of the best fit line taken from the plot, which if plotted on a log-log scale, should give the characteristic gradient of 0.5. The linear full well capacity is taken from the peak in the photon transfer curve. This is where the noise begins to reduce as the variation in signal is dampened as no more signal can be collected. The maximum full well capacity is taken as the maximum signal level which is plotted on the graph. If an integration sweep was performed, the dark current can be obtained from the gradient of the dark signal level plotted against the integration time. A result[3] from the best pixel variant from FORTIS 1.0 is shown

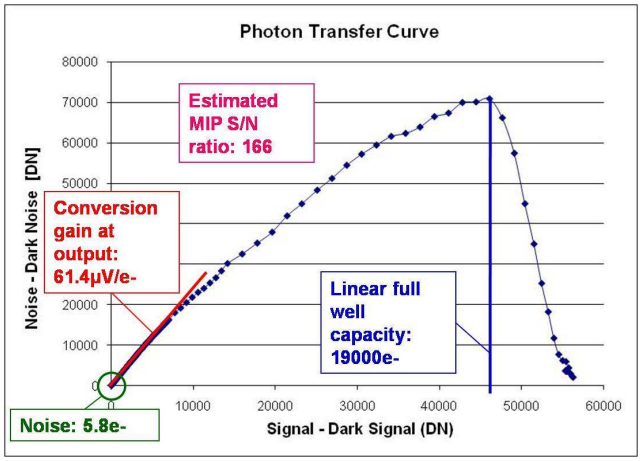

Figure 5: Results from the best pixel of FORTIS 1.0

in Figure 5. This pixel had a very low noise of 5.8 e^-, and a high conversion gain of 61.4μV/e^-, demonstrating the benefits of the 4T pixel architecture.

2.2 Radiation hardness

Three FORTIS 1.0 sensors were irradiated up to 1MRad in steps of 10kRad, 20kRad, 50kRad, 100kRad, 200kRad, 500kRad and 1MRad using 50kVp x-rays from an x-ray tube. In-between the irradiations, when not being tested, the chips were stored at -25^o C. At each radiation step the noise of the best pixel variant was measured using the PTC technique. In Figure 6 the noise distribution for one chip are shown measured before irradiation and after 500 kRad. In Figure 7 the average noise for each of the three sensors is shown as a function of dose[3]. Clearly, the sensor is still working well up till 500 kRad. A logarithmic increase with respect to irradiation level was found between 0-500 kRad from 6-9e^- rms, and the noise distribution clearly spreads out, suggesting that random telegraph signal noise and 1/f noise has increased, which are both associated with charge trapping in the source follower transistor gate oxide and the corresponding silicon-silicon dioxide interface[4].
It was found that the noise significantly increased beyond 500kRad to a point where the signal-to-noise ratio decreased substantially and a MIP would not be reliably detected, therefore the suggested radiation tolerance for FORTIS 1.0 is between 500 kRad-1MRad.

2.3 Laser scan

When electron-hole pairs are generated by a MIP, the electrons will typically diffuse through the epitaxial layer, and if they are sufficiently close to the depletion region of the diode, they will be collected. In the ideal situation, the entire epitaxial layer underneath the diode would be completely depleted, changing the main charge transport mechanism from diffusion to drift, where the increased electric fields from the larger

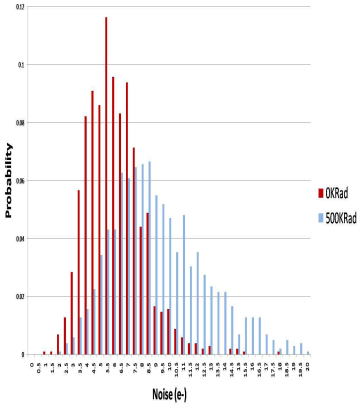

Figure 6: Noise distributions measured before irradiation and after 500 kRad.

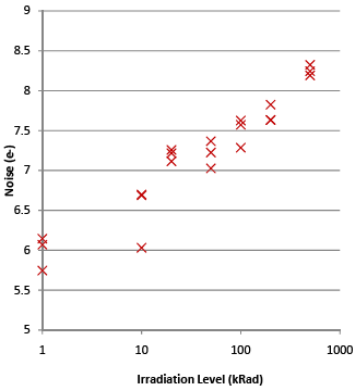

Figure 7: Average noise as a function of radiation dose.

depletion region attract more charge than in the case of a smaller depletion region. As the depletion region width increases with increasing resistivity of the epitaxial layer, one way to extend the depletion region further into the epitaxial layer and improve the charge collection efficiency is to use an epitaxial layer with a high resistivity[5, 6]. The use of a high resistivity epitaxial layer should also reduce the cluster size as less charge will be diffusion to and get collected by the neighboring pixels, improving the hit finding efficiency.

FORTIS 1.1 has been fabricated with both a standard (10-100 Ωcm) and a high resistivity epitaxial layer (1-10kΩcm). To test the difference in charge collection, a white light source was focused down to a 2 μm$\times$2 μm^2 spot size and then horizontally scanned across the centre of the diodes of three adjacent pixels. The results are shown in Figure 8 and 9. The peaks and troughs represent the diode and metal within the pixel respectively, and the secondary peaks are due to charge being collected by the neighbors. Clearly, the charge collected by the neighbors is a lot lower when using a high resistivity epitaxial layer. The effects on hit finding and position reconstruction are still under investigation.

2.4 Beam test

This summer the FORTIS sensors were tested in a beam test at the SPS using a 120 GeV pion beam. Both standard and high resistivity epitaxial layer chips were tested, as well as chips with and without deep p-well. The results are currently being analysed. In Figure 10 an event display obtained with a high resistivity FORTIS 1.1 sensor is shown. The plot shows the first detection of MIPs with a 4T architecture. In Figure 11 the pedestal corrected signal for each pixel in each event is shown for a short pedestal run and a larger beam run. This result also demonstrates that we clearly see particles. In Figure 12 and 13 the cluster signal distribution and the pixel noise distribution are shown. As can be seen there are just a few pixels with very low noise. This particular

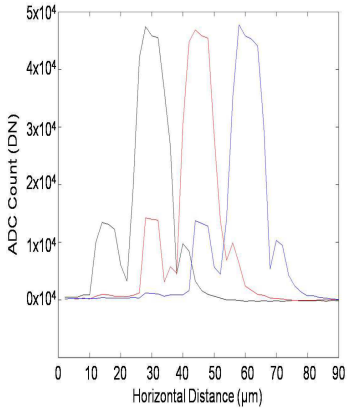

Figure 8: Laser scan using a FORTIS 1.1. with a standard resistivity epitaxial layer

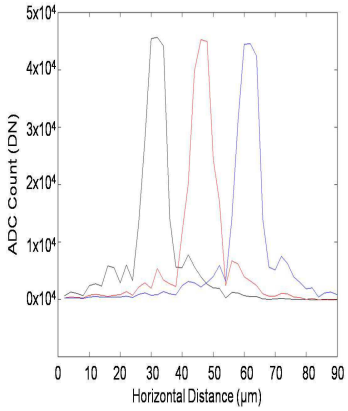

Figure 9: Laser scan using a FORTIS 1.1. with a high resistivity epitaxial layer

substructure[1] displays a signal-to-noise ratio of ∼50. Currently, work is going on on the sensor alignment.

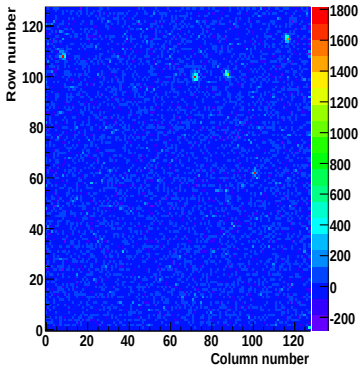

Figure 10: Event display taken with a high resistivity FORTIS 1.1. Five hits can clearly be seen.

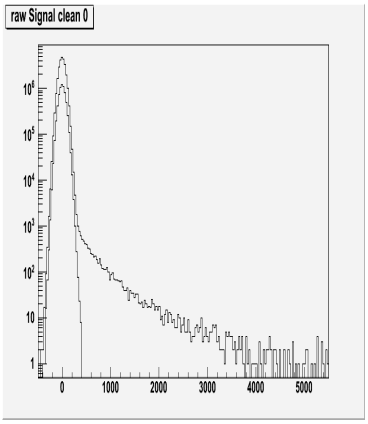

Figure 11: Pedestal corrected signal for each pixel in each event with and without beam.

3 Summary

We have performed a beam test of the FORTIS sensor. We are still working on the analysis. We have tracks in the EUDET telescope and the data from the FORTIS sensor is in the same data file as the EUDET telescope.
We would like to express our thanks to the EUDET collaboration for our their help during the data taking.

[1]This is not the substructure with a noise of 5.8 e^-.

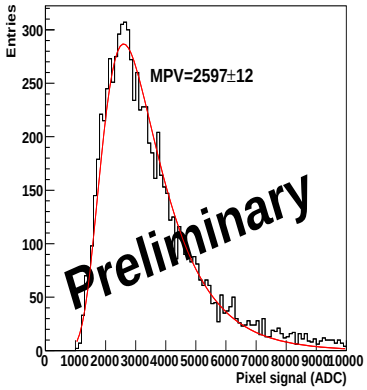

Figure 12: Cluster signal distribution for the high resistivity FORTIS 1.1.

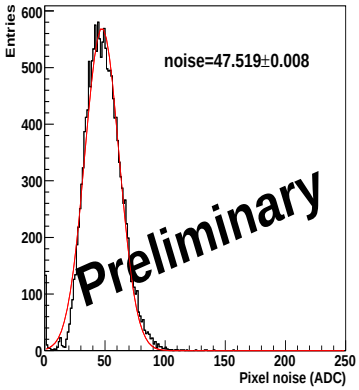

Figure 13: Pixel noise distribution for the high resistivity FORTIS 1.1.

References

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