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# Status of TPC-electronics with Time-to-Digit Converters

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**Abstract**

Two components of the last EUDET milestone of our group are presented: a Data Readout Module and a PCA16 test board. These were designed and manufactured in 2009.

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# 1 Introduction

Within EUDET JRA2, TPC readout electronics based on a new principle of data acquisition is being developed. In this approach, time of arrival and charge of signals from TPC pads are measured with the help of a time-to-digital converter. The charge is measured indirectly, with help of a charge-to-time converter. This technique is currently implemented using ASDQ ASICs.
Next step in the development of TPC readout electronics requires optimization of parameters of the signal readout chain. To study signals from a TPC detector, test boards based on PCA16 chip have been produced. Data Readout Module focuses on TDC' digital interface and concentration of data from several TDCs. PCA16 test boards and Data Redout Modules comprise the last EUDET milestone of our group.

# 2 640 channel Front-End Electronics based on TDC

Front-End Electronics based on Time-to-Digit Converters[1] has been fully assembled. During first tests with a GEM module no optimal signal-to-noise ratio was found. Optimization of shielding has decreased pick-up noise of the system, what resulted in a signal threshold of 0.15 V. For comparison, typical threshold in the setup with a test chamber (3 GEM foils, gas gain $\sim$ 10000) is 0.25 V. The main reason for suboptimal signal-to-noise ratio is insufficient gas gain ($\sim$ 3000) of the used GEM module.
Presence of magnetic field in the TPC effectively reduces transverse diffusion of electrons in the gas, therefore electrons arrive onto less number of pads, possibly only one. Larger number of electrons projected onto a pad means larger signal, but also degradation of spatial resolution. At this stage of readout electronics development, signal efficiency is of more importance than precision of the coordinate measurement.
Based on this, a test with a GEM module on LPTPC with PCMAG[2] has been prepared. During ramp up of the magnetic field, stray field of the PCMAG moved some conducting parts inside of VME power supply, damaging it. The test had to be cancelled. Before such test, optimal position of a new VME crate with respect to the PCMAG need to be found.
An alternative for a GEM module is a readout system based on Micromegas. Existing Micromegas modules, can reach gas gains of the order of 20000. If used with a resistive layer on the pads, a Micromegas readout system broadens signals, both in space and time. First tests with a Micromegas module (with resistive ink) demonstrated, that the width of a signal even for short drift distance ($\mathcal{O}$ 1 cm) can be as large as 400 ns. With the short shaping time of the ASDQ of 28 ns, only little amount of charge can be collected. For comparison, a Micromegas system without resistive layer, features signal width of 50-100 ns, which increases efficiency of signal registration. Since input connectors of Barcelona boards [1] have been chosen to fit onto GEM modules, adapter boards for a Micromegas module have been developed and manufactured. Yet, no tests of the readout electronics with a Micromegas module have been performed.

# 3 PCA16 Test board

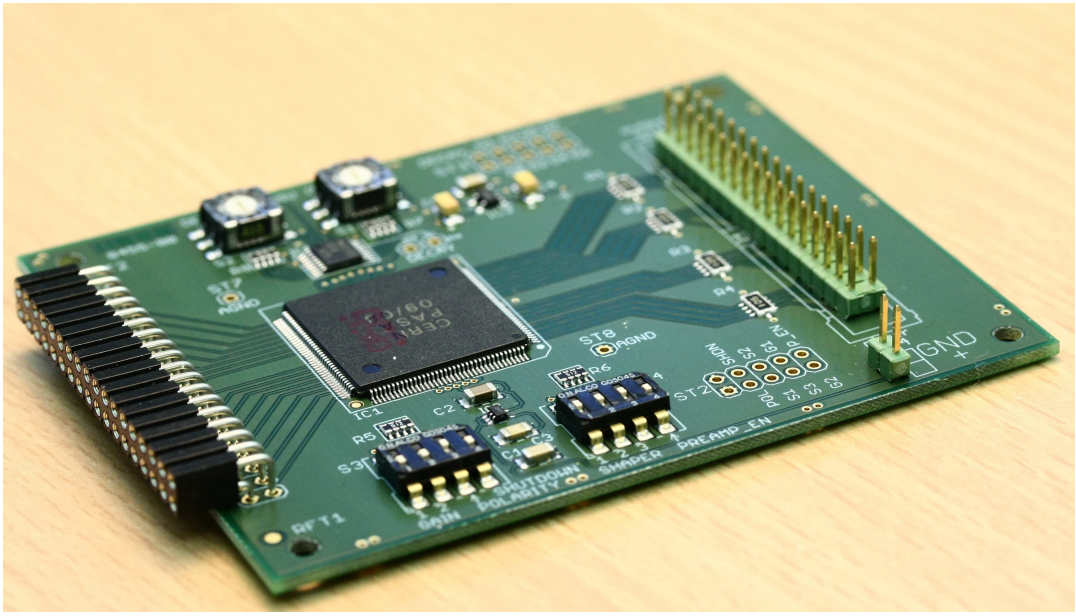


Figure 1: A photograph of a PCA16 test board.

A PCA16 test board, Figure 1, is based on one PCA16 chip developed at CERN[3]. The main purpose of the board is to study signals from a GEM detector, in order to optimize a future amplifier and charge-to-time converter.
The PCA16 test board has size of 72 mm × 90 mm. Gain, shaping time, polarity and preamplifier mode of the PCA16 chip can be varied with the help of DIP switches on the board, as well as, externally by logic potentials (maximum level: 1.5 V). Particularly interesting is the variable shaping time (30 ns, 60 ns, 90 ns and 120 ns) of the PCA16 chip. This allows to study effect of shaping time on timing and charge measurement performance.
In the "preamplifier enabled" mode shaper is bypassed and the decay time can be varied with the help of two rotary switches. These switches set 8-bit code for a DAC, which supplies a potential to the "decay"-pin of the PCA16 chip.
Two voltage regulators provide power on a PCA16 test board: 2.7 V for DAC and 1.5 V for PCA16 chip and DAC reference input. The voltage range on the power connector is 2.7–6 V.
In order to simplify connection of a PCA16 test board to an oscilloscope a supplementary board "PCA16 line driver" has been developed. On the board are four high bandwidth operational amplifiers which work as a 50 Ohm line drivers.

One PCA16 test board has been tested with a small TPC prototype detector[4]. Charge clusters in the detector were produced with a $Fe^{55}$ radioactive source. The (single) pad

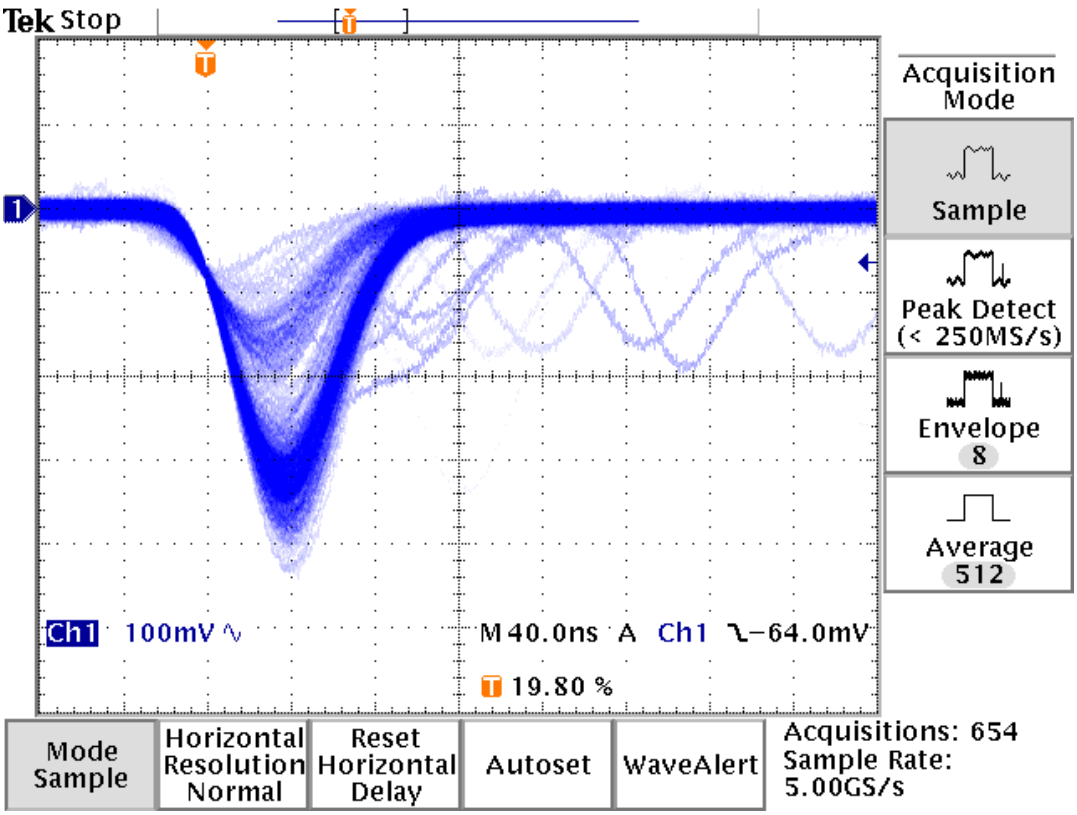


Figure 2: Signals from a GEM detector obtained with a PCA16 test board.

has been connected to one channel of the PCA16 board. Signals from the output of the board were observed, with a *Digital Phosphor Oscilloscope*, Figure 2. Several signal acquisitions are overlayed on the screen and the intensity of the waveforms represents the rate of the signals.
One clearly distinguishes two main groups of waveforms: signals with highest rate and the largest amplitudes of 300-400 mV (PCA16 output is AC-coupled in this test) and signals with lower rate and smaller amplitudes of 150-200 mV. Those two groups of signals correspond to 5.9 keV photons from the $Fe^{55}$ source and the Argon escape peak.

# 4 Data Readout Module

A modular ILC TPC endplate will have around 100 readout modules, each with several hundreds readout chips (amplifiers and digitizers). A Data Readout Module (DRM) represents only digital part and addresses the data concentration from multiple readout chips.

A DRM, Figure 3, consists of two components: an FPGA-module and a microcontroller evaluation board. Size of a Data Readout Module is 120 mm × 160 mm. The power to

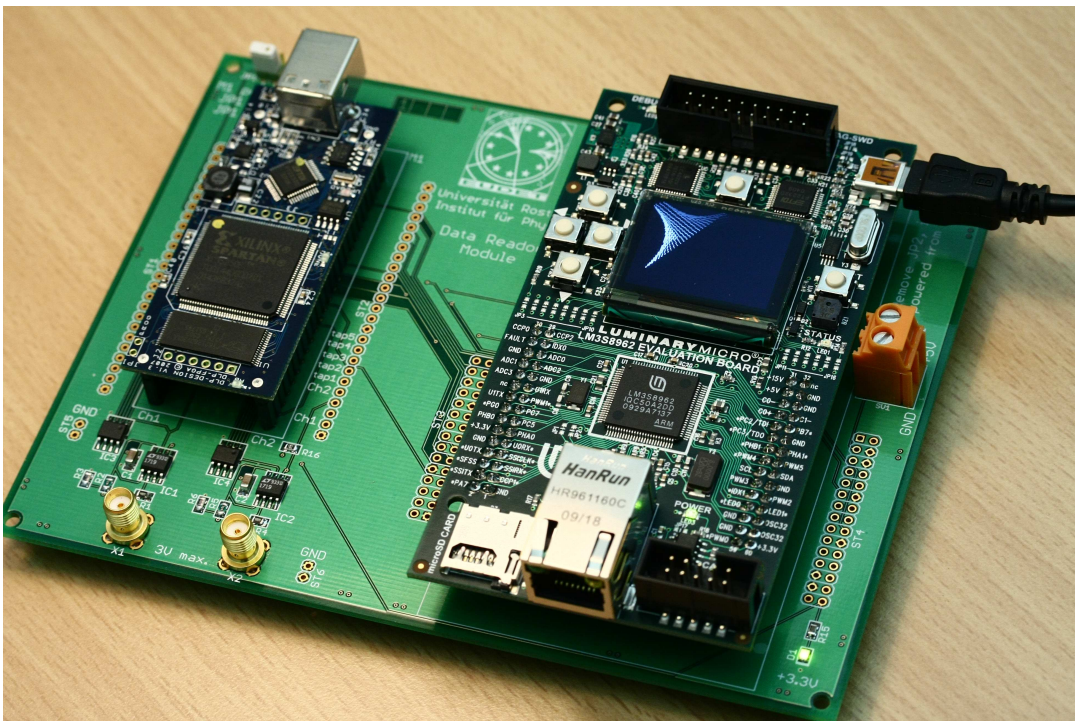


Figure 3: Photo of a Data Readout Module.

a DRM is provided via USB connector of the FPGA module. Additionally, it can be powered from an external +5 V source. The microcontroller evaluation board can be also powered separately from its own USB connector.
Data to the DRM can be provided from a pattern generator (via two SMA connectors) or generated directly in the FPGA. Signal from an SMA connector (LVTTL, 3 V maximum) is delayed with multi-tap silicon delay line, so that delayed copies (5 ns, 10 ns, 15 ns, 20 ns and 25 ns) of the signal are provided to the FPGA. These six signals simplify programming of the FPGA time measurement circuit. Since high precision time measurement is not addressed here, single TDC channel can be realized as a simple binary counter.
Due to its simplicity, multiple TDC channels (it is assumed to be a 64 channel TDC) can be programmed in the FPGA module. In this case data to be generated in the FPGA. Since signals on ILC TPC pads originate, most of the time, from the beam-background, an estimate can be obtained from simulation. Analysis of pad occupancy for LDC TPC[5] yields $< 15$ hits $>$ per TDC chip[1]. Taking this into account, corresponding amount of data will need to be generated on the output of the TDC.
Due to limited pin budged, the FPGA connected via 8-bit bus to an Ethernet-capable microcontroller. The Ethernet standard appears to be a good candidate for efficient data acquisition. The measures of efficiency here are the electric power and material budged,

[1] Analysis of beam-background in ILD TPC gives $< 7$ hits $>$(SB2009 machine parameters, 50 BX).

availability in future, price and speed. This, however, by no means excludes any other data links.

It is assumed that the amplifiers, TDCs and a data concentrator are all positioned on a module of ILC TPC. Each TDC sends data over a serial line, for example, using LVDS signaling, to the data concentrator. In the ILC TPC, the role of the data concentrator can be taken by a large (radiation hard) FPGA. In the DRM the FPGA plays role of the TDC and the microcontroller considered to be the data concentrator.

Two Data Readout Modules are provided. The modules to be connected to a Gigabit Ethernet switch, which acts as a Back-End of the ILC TPC data acquisition system. Different TDC data interfaces and data concentration methods can be studied.

# 5 Summary

First tests of TDC-based readout electronics with GEM-modules have been performed. A higher gas gain of an amplification system is necessary. Optimal position of the VME crate, with respect to the PCMAG need to be found. Two Data Readout Modules and three PCA16 test board are provided.

Last EUDET milestone of our group has been reached in December 2009.

# Acknowledgement

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# References

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