Status of VFCAL

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Abstract

The effort within VFCAL was focused in 2007 on the design of the front-end electronics. A first version of the design has been developed, prototypes have been produced and performance studies are under way. In addition, the laboratory infrastructure has been upgraded, the equipment for tests of the radiation hardness of sensors in a beam has been completed and the equipment for sensor tests in the EUDET telescope has been partly developed. Progress has also been made in the design and construction of a laser position monitor system with μm accuracy.

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1 Introduction

Two calorimeters in the very forward region are planned for the ILC detector to extend the coverage to small polar angles, to measure precisely the luminosity and to assist beam tuning to optimize the luminosity. The calorimeters must be fine-grained and compact. The innermost calorimeter has to withstand harsh radiation conditions and must be read out bunch-by-bunch. At larger polar angles LumiCal must be positioned extremely precisely and the inner acceptance radius must be controlled on μm level. Due to the high occupancy, fast front-end (FE) electronics is also needed.
The goal of the VFCAL project is to develop the infrastructure for tests of all sub-components of these special calorimeters. This includes infrastructure to develop position monitoring on μm level and to investigate radiation hard sensors. In addition, the design and test of ultra-thin sensor planes and fast FE electronics will be done to support tests in particle beams.

2 FE Electronics Design Considerations

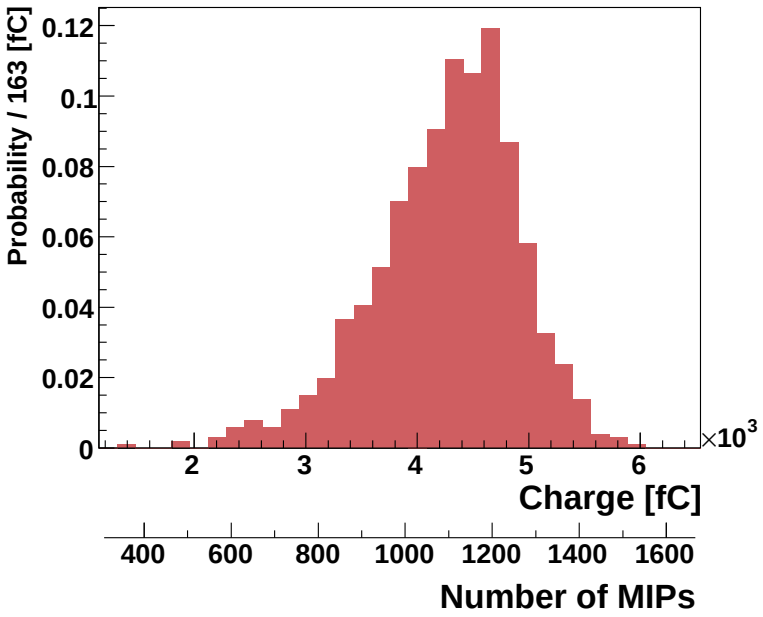

Figure 1: The distribution of the charges on the pads for an electromagnetic shower of 250 GeV energy.

In the current design, LumiCal consists of 30 layers of 300 μm thick DC-coupled silicon sensors. Each layer is divided into azimuthal sectors and each sector is segmented into radial strips with a constant radial pitch. Such design results in pads on the sensors

with input capacitances to the front-end preamplifier between 10 and 100 pF. The FE

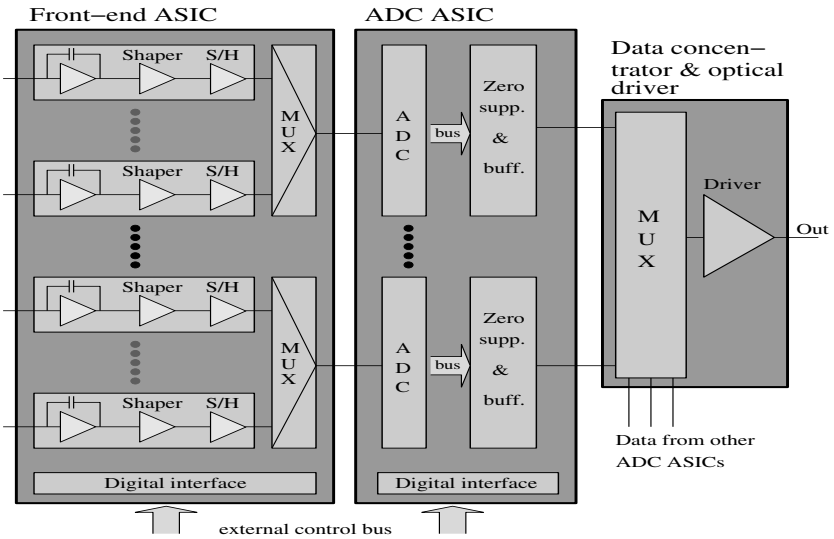

Figure 2: Block diagram of the FCAL readout electronics.

preamplifier is foreseen to be operated in two modes - the physics mode and the calibration mode. In the physics mode, the depositions from electromagnetic showers of high energy have to be read out. From Monte Carlo simulations the charges collected on the pads are estimated to reach values up to 7 pC, as can be seen from Figure 1 [1].
In calibration mode, the signals from relativistic muons, i.e. minimum ionising particles, MIPs, should be detected.
Because of the very high occupancy expected, the front-end electronics must resolve signals from particles in subsequent beam bunches, i.e., in a time scale of 100 ns. The power dissipation must be kept small to avoid cooling pipes and thermal tensions. This will be ensured by switching off the power in the periods between the bunch trains. The requirements on the BeamCal FE electronics are very similar.
The general concept of the FE electronics, matching all the requirements listed, is outlined in Figure 2.
The main blocks in the signal flow are:

- The front-end electronics.
- The A/D conversion plus zero suppression.
- The data concentrator with the optical driver.

The first two blocks of Figure 2 need to be designed as dedicated multichannel ASICs [2]. In the following the design of these blocks is discussed and simulation results are presented. The prototype design is done using the AMS 0.35μm technology. The data concentrator and optical driver block will be studied in a later development stage.
The low noise requirements are driven by the calibration mode operation where a S/N ratio of about 10 should be sustained even for the largest sensor pad capacitance. At

the present stage, the power dissipation per channel is constrained to 10 mW. In order to fulfill the requirements concerning low noise operation and wide range of input capacitance, a charge sensitive preamplifier configuration was chosen. Two architectures are currently under study: one with continuous pulse shaping and one based on a Switched-Reset scheme. For both architectures, simulation results are discussed below.

2.1 Front-End with Continuous Pulse Shaping

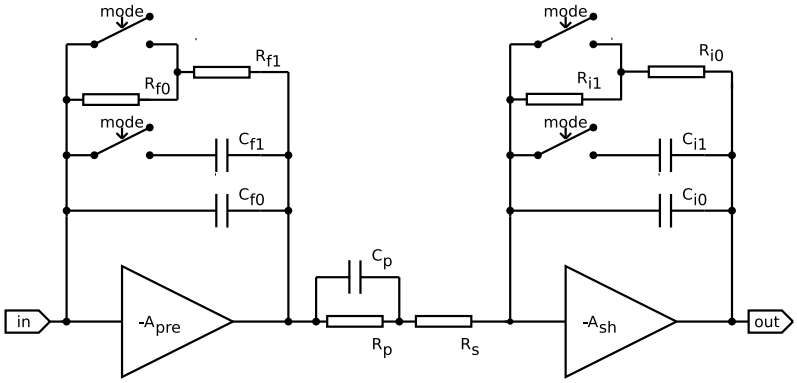

Figure 3: Scheme of the preamplifier, the PZC and the shaper. The switches are set to the calibration mode.

Each FE channel is built of a preamplifier, a pole-zero cancellation circuit (PZC) and a shaper, as shown in Figure 3. The preamplifier integrates the signal from a sensor on the feedback capacitance. The PZC circuit is used to shorten the slow tail of the preamplifier response and such to improve high input rate performance. To optimize the signal to noise ratio and high speed performance, the preamplifier and PZC is followed by a pseudo-Gaussian shaper with a peaking time of about 70 ns. In order to cover the amplitude range of input signals, from MIPs in the calibration mode to about 8 pC in the physics mode, a variable gain scheme is implemented. The change of the gain is realized by the switches in the preamplifier and shaper feedback. The transfer function of the circuit in Figure 3 is equivalent to a standard CR-RC first-order shaping. Both the preamplifier and shaper circuits are designed as folded cascodes with active loads, which are followed by buffers.
The front-end electronics is designed as a multichannel ASIC. In order to match the sensor segmentation, single ASICs containing 32, 48 or 64 channels are considered for the final version.
Simulations of the FE circuits were done using the Cadence package with Hspice and Spectre simulators. The typical simulated responses for sensor capacitances in the range from 10 to 100 pF are shown in Figure 4 for the calibration mode (mode0) and for the physics mode (mode1). One can see that in the calibration mode the amplitude and peaking time depend on the input capacitance. This happens because in the calibration

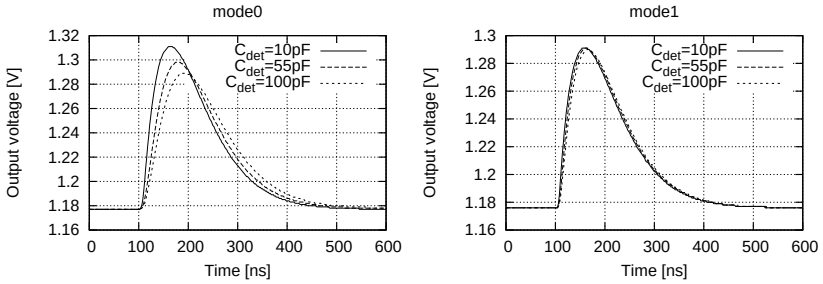

Figure 4: Example of shaper output in calibration mode for 10 fC input charge (left,mode0) and in physics mode for 1 pC input charge (right, mode1).

mode, where the preamplifier's feedback capacitance C_f is small ($\sim 400fF$), the ratio of the sensor capacitance C_{det} to the effective input capacitance $C_{eff} \simeq A_{pre} \cdot C_f$ is not negligible since the preamplifier gain A_{pre} is below 1000 while the sensor capacitance reaches 100 pF. In such a case, part of the input charge is lost due to the sensor capacitance and the preamplifier can not be considered as purely charge sensitive. On the contrary, in the physics mode where the feedback capacitance is large ($\sim 10\ pF$), the aforementioned ratio may be neglected and the preamplifier behaves as purely charge sensitive. This is seen in Figure 4 (mode1) where the dependence on input capacitance is hardly noticeable. The simulations were done for a wide range of input charges. The circuit is linear below 10 pC and saturates above 15 pC. In all simulated cases the S/N ratio stays above 10.

2.2 Switched-Reset Front-End

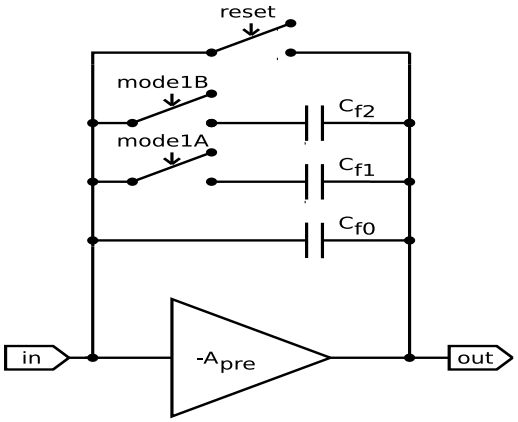

Figure 5: Scheme of switched-reset preamplifier.

A preamplifier with a feedback reset instead of a feedback resistance could be a very attractive configuration because such a solution does not need a shaper and has a large output dynamic range. For this reason a charge sensitive configuration equipped with a

reset switch as shown in Figure 5 is investigated. The preamplifier is designed as a folded cascode. To allow variable gain operation, different values of feedback capacitances are implemented. The calibration mode configuration is obtained using the smallest capacitance C_{f0}. Simulations of this configuration were performed for a wide range of input capacitances and input charges. In all cases, the signal rise-time is below 300 ns. Since the simulated reset-time of the preamplifier never exceeds 40 ns, the full cycle of pulse response and the reset can be kept between two bunches. In the calibration mode, the circuit is linear up to about 300 fC and saturates for higher input charges. In the physics mode, the linearity region can be extended to tens of pC by increasing the feedback capacitance. The circuit noise performance is currently under study.

3 Front-End Electronics Measurements

A prototype 12 channels ASIC was designed and produced in 0.35 μm CMOS technology. Three prototype ASICs were bonded to a dedicated PCBs to test the front-end functionality and to measure their electrical parameters. First the continuous pulse shaping front-end functionality was measured by injecting a charge into the preamplifier input and observing the output signal. In Figure 6, pulse shapes measured in physics (right)

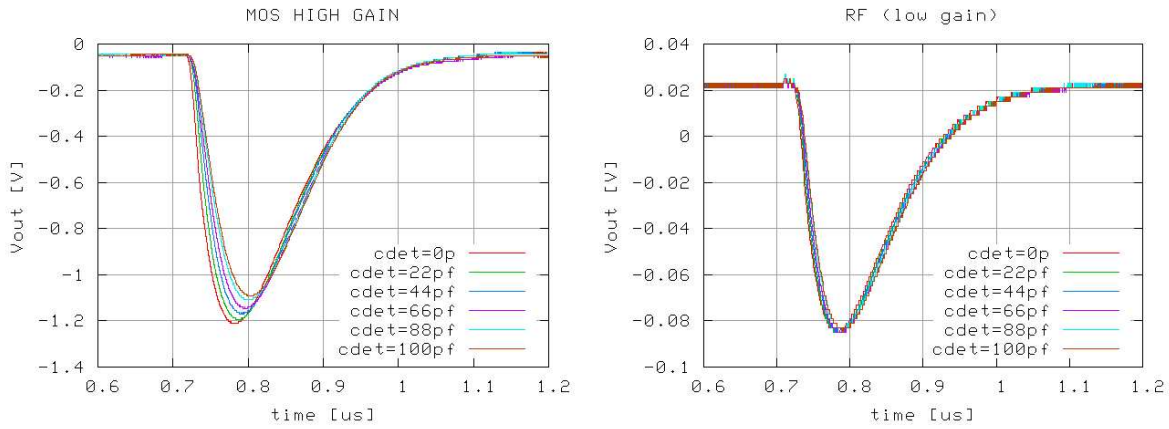

Figure 6: Measured pulses in the calibration (left) and physics (right) modes.

and calibration mode (left) are shown. One can see that in the calibration mode the amplitude and peaking time depend slightly on the input capacitance. In the physics mode, when the feedback capacitance is large ($\sim 10\ pF$), both the amplitude and peaking time are not sensitive to the value of input capacitance. The measurements presented above are in good agreement with Hspice simulations performed for both gain modes shown in Figure 5. The gain was measured over the full input signal dynamic range for a few channels. In Figure 7, preliminary results obtained for the physics mode are shown. The measurements were done for injected charges up to 17 pC, as seen in Figure 7. The amplification is linear up to about 10 pC and starts to saturate for higher input charges. As expected, the channel response is not sensitive to the input capacitance.

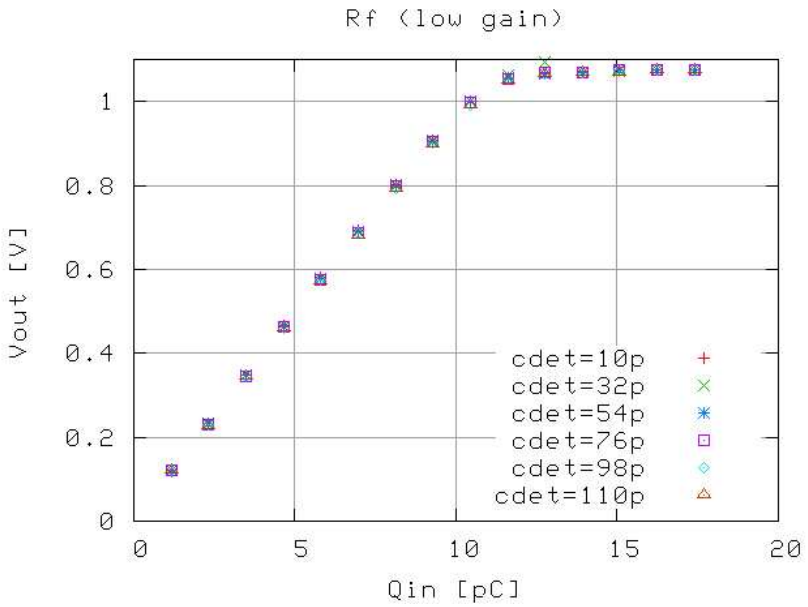

Figure 7: The amplitude at the preamplifier output as a function of the injected charge in physics mode.

4 Analog to Digital Conversion

From simulations it is estimated that an ADC with 10 bit resolution matches the performance requirements of the calorimeter. Considering the number of detector channels needed and the limitations on space and power, the best choice for the analog to digital conversion seems to be a dedicated multichannel ADC. To save area, a reasonable solution for LumiCal would be to foresee one fast ADC for 8 channels of the front-end electronics. Since the LumiCal detector requires a sampling rate of about 3 MHz per channel, an ADC should sample the data with at least 24 MHz rate. On the other hand a single 3 MHz ADC per each channel would be the simplest solution from the designer point of view. The latter solution would also match the needs of BeamCal. Both solutions are still under consideration.
One of the most efficient architectures assuring a good compromise between the speed, area and power consumption is a pipeline ADC, hence this option was chosen.

4.1 ADC Architecture

A pipeline ADC is built of several serially connected stages as shown in Figure 8. In the proposed solution a *1.5 bit stage* architecture was chosen because of its simplicity and immunity to offsets in the comparator and amplifier circuits. Since a single stage generates only three different values coded on 2 bits it is called *1.5 bit stage*. Each stage from Figure 8 generates 2 bits which are sent to a digital correction block. In the correction block, 18 output bits from 9 stages are combined together resulting in 10 bits

of ADC output.

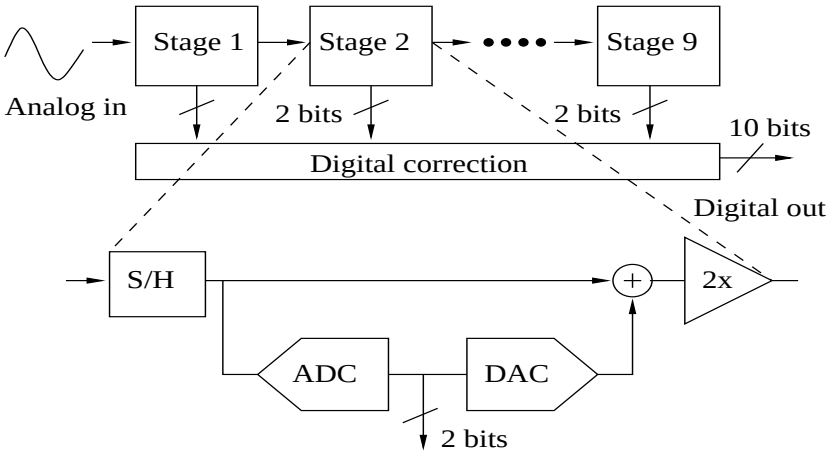

Figure 8: Pipeline ADC architecture.

The block diagram of a single stage is shown in Figure 9. Each *1.5 bit stage* consists of two comparators, two pairs of capacitors C_s and C_f, an operational transconductance amplifier, several switches and a small digital logic circuit. To improve the ADC immunity e.g. against digital cross-talks, a fully differential architecture is used. The operation of the stage is performed in two phases. In phase φ_1, capacitors C_s and C_f connected to ground through S_1 are charged to voltages $V_{i\pm}$. In phase φ_2, the switches S_2 and S_3 change positions and S_1 is open. The C_f are now in the amplifier feedback while the C_s are connected to the DAC reference voltages. In the *1.5 bit stage* architecture $C_f = C_s$ is chosen to obtain a gain of two in the transfer function.

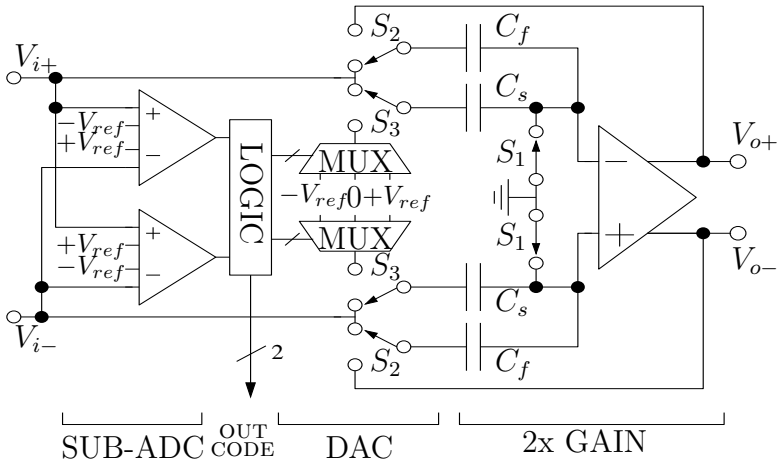

Figure 9: Simplified schematics of a 1.5 bit stage. Switches are set to φ_1 phase.

A telescopic cascode amplifier configuration is used here since it represents the most efficient solution with respect to speed versus power. In order to obtain the necessary gain of about 80 dB, required for 10 bit resolution, gain boosting amplifiers are used

in both upper and lower cascode branches. Since the *1.5 bit stage* architecture leaves very relaxed requirements on the comparators (∼100mV threshold precision), a simple dynamic latch architecture was chosen.

4.2 ADC Measurements

The prototype ASIC with 8 pipeline ADC stages was designed and produced in 0.35 μm CMOS technology. Two ASICs were bonded to a dedicated PCB board to test the front-end functionality and measure its electrical parameters. A preliminary measurement of the digital output after 8 stages versus the input signal amplitude is shown in Figure 10. One can see that the analog to digital conversion is performed properly.

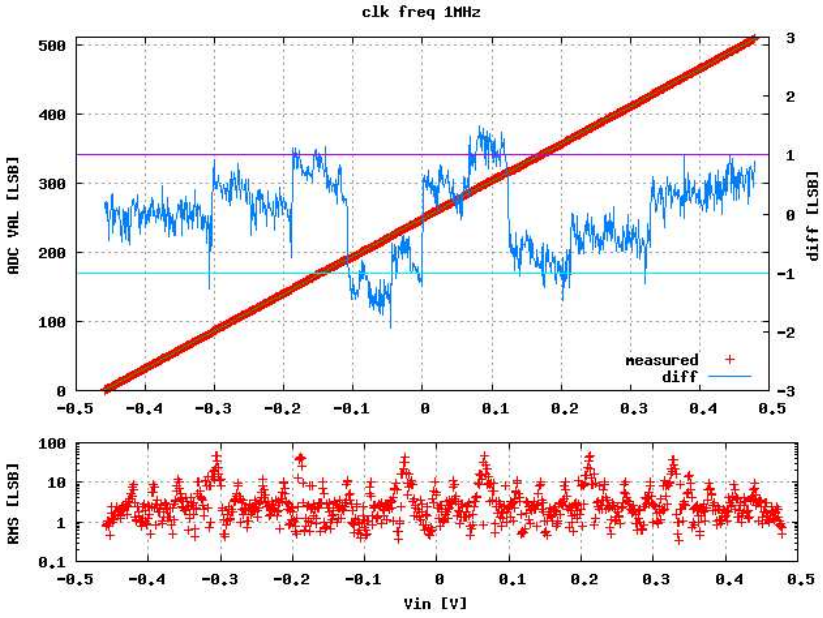

Figure 10: The ADC output as a function of the input signal amplitude.

5 FE Electronics Test-Stand

Firmware was developed to use a versatile VME module as pattern generator for testing newly developed different front-end chips. The setup is shown in Figure 11. For samples of an 18-channel preamplifier chip with analog multiplexing, developed by LAL Orsay, a testing printed circuit board has been developed and built. Parameters of these chips, such as linearity over channel number and charge decay versus readout speed, have been measured. This test facility will be used in future to test the FE ASICS produced by the AGH University Cracow.

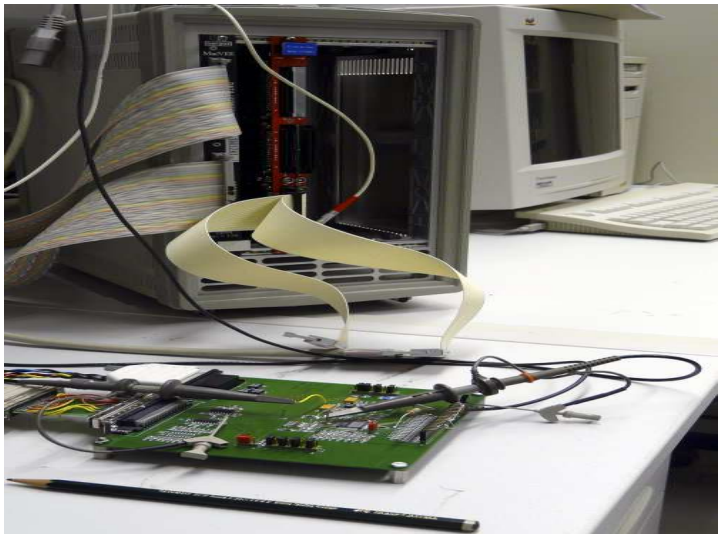

Figure 11: The test-stand for FE electronics based on a CAEN V1495 sequencer module.

6 Measurements Using Particle Beams

The test-beam equipment for sensor tests in low-energy electron beams has been completed in 2007. It has been used for irradiation tests at the S-DALINAC accelerator at the Technical University of Darmstadt. A beam of 10 MeV electrons is directed to the sensor. A brass collimator limits the cross section of the spread beam and measures the electron current dumped onto it. The sensor is positioned inside the PCB box with applied bias voltage. A brass Faraday cap collects all electrons traversing the sensor. Measuring the current, the dose rate can be determined. After a certain integrated dose is collected, the signal of a ^{90}Sr source β beam is measured in a spectroscopic setup. Its peak position is determined, denoted hereafter as reference signal, and monitored as a function of the absorbed dose.
The performance of mCz-silicon, GaAs, polycrystalline and single crystal diamond sensors has been studied as a function of the absorbed dose. As an example, in Figure 12 the reference signal sizes of two GaAs pad sensors are shown as a function of the absorbed dose [3]. The signal decreases continuously with the absorbed dose, approaching at 1 MGy about 10% of the signal of a non-irradiated sensor. The behavior of the two sensors is very similar.
The results obtained for all sensor types were presented at the IEEE conference in October 2007 [4]. They constitute the basis for the forthcoming discussions with the sensor producers to understand the damage mechanisms and to further improve the radiation hardness of the sensors.
In order to clarify for diamond sensors the relation between energy loss by ionisation and the amount of created free charge carriers, we studied the signal of a single crystal diamond sensor for electrons of 3, 4 and 5 GeV energy in the DESY test-beam using the EUDET pixel telescope. A picture of the setup is shown in Figure 13. The data taken are under study now. Depending on the results, we will decide about additional

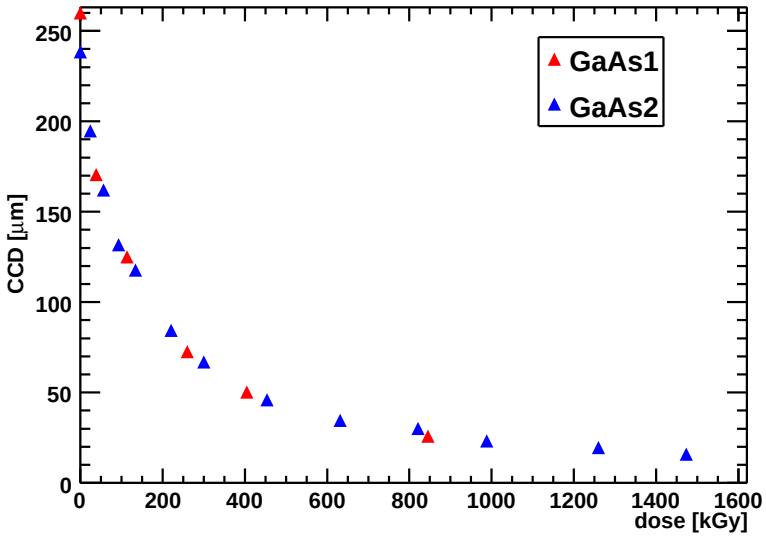

Figure 12: The signal size (expressed in charge collection distance, CCD) as a function of the absorbed dose, for two GaAs pad sensors.

test-beam campaigns.

7 Laser Alignment Studies

The laser positioning system is planned to monitor the position of the LumiCal with respect to the beam-pipe and the distance between the two calorimeters, and the position of at least a few sensor planes inside the calorimeter. Laser beams, mirrors and CCD sensors will be used to ensure the position control on the μm level.
In the test-bench developed by INPPAS Cracow, shown in Figure 14, two narrow laser beams are directed to a CCD sensor. One beam is perpendicular to the plane of the CCD sensor and the other shines onto the sensor with an angle of 45°. Using the two laser spots on the CCD, shown in Figure 15, the spot position of the perpendicular beam monitors movements in the (x-y) plane. The distance between the two spots measures the displacement in the z direction. The system is now installed in a temperature stabilized box and studies of the temperature dependence of the distance measurement with respect to a mechanical reference measurement and of the long term stability are done [5]. As an example, the result of the measured position over a time interval of about a week is shown in Figure 16. As can be seen, the drift of the measured position is below 1 μm.
In the ILC detector the laser system has to control not only the position of each of the calorimeters with respect e.g. the beam-pipe but also the distance of a few meters between them. Therefore an optomechanical concept for such a facility, as illustrated in

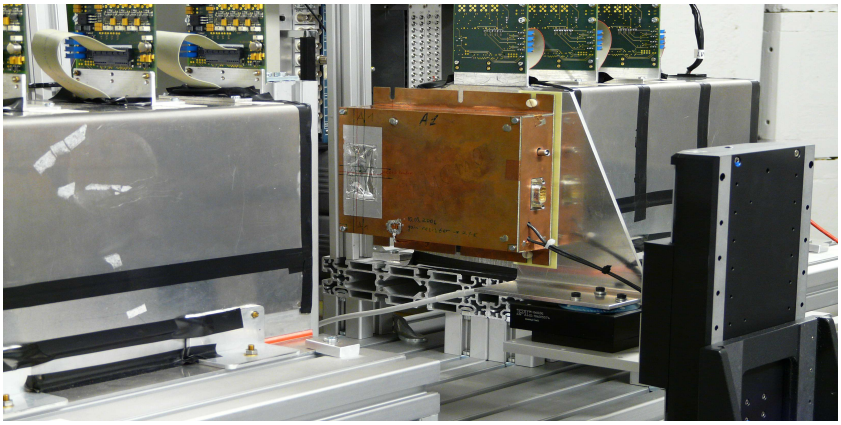

Figure 13: The test-beam setup for studies of a single crystal diamond. The sensor under test including the preamplifier is housed in the copper covered PCB box. Up- and downstream of this box the pixel sensors of the EUDET telescope are installed.

Figure 17 is under development.

8 Sensor Diagnostics and Development of Sensor Planes

The Tel Aviv group is completing a test lab for silicon sensors. Most components of a computer controlled probe station were purchased and a Labview based software for the measurement of the current and capacitance as a function of the voltage is developed. First measurements are under way to debug the software of the system. Also the possibilities of sensor production in Israel are investigated.
The upgrade of the silicon lab in DESY Zeuthen is finished and used for electrical tests of all kind of sensors.
The sensor planes of LumiCal are designed as sketched in Figure 18 by INPPAS Cracow [6]. Negotiations are ongoing with Hamamatsu Corp. about the production of a first batch of sensors.
On a fully assembled sensor plane the signal pads must be connected with the FE ASICs placed at the outer radius of the plane. One option is the use of a flexible PCB with copper traces bonded on one side to the sensor pads and connected on the other side to the FE ASIC. A prototype of a flexible PCB prepared for the signal transmission tests is shown in Figure 19. These segments will be investigated in detail in 2008.

9 Summary

The FE readout electronics design has been completed in a first version, the main readout circuits i.e. the prototype front-end channels and main ADC blocks have been simulated and first prototypes were produced. First test have shown proper functionality of both

Figure 14: The test bench of the laser position monitoring system using two laser beams directed to a CCD sensor.

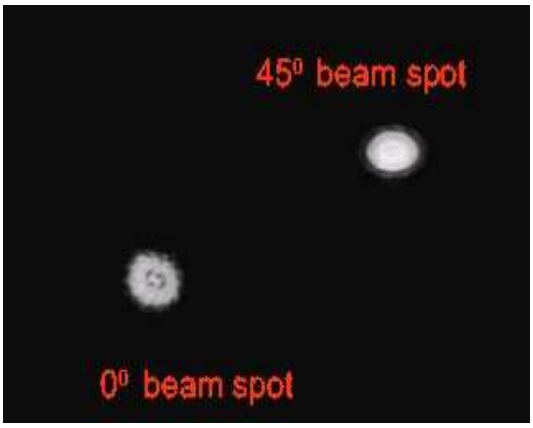

Figure 15: The spots on the CCD from two laser beams with angles of zero and 45°.

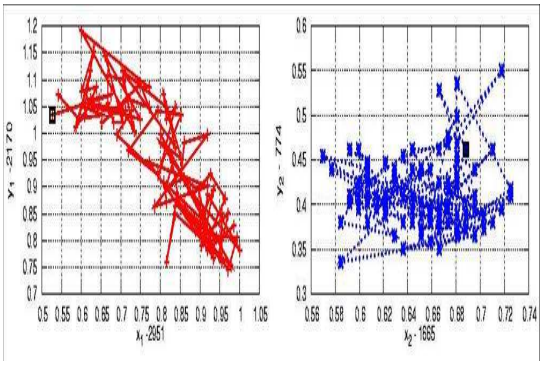

Figure 16: The position, measured with the laser system in x-y coordinates, as a function of time over a week.

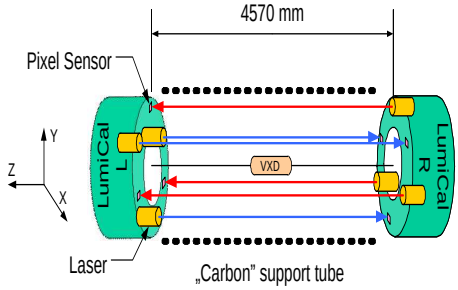

Figure 17: A scheme for a laser based system to control the distance between two calorimeters.

circuits. The detailed measurements are ongoing. In the next evaluation stage, the sub-circuits not yet designed, like sample and hold (S/H) or multiplexer (MUX), will be integrated and prototyped as well. Then the integration of multichannel ASICs with all channels and full functionality comprising all necessary controls, DACs, zero suppression etc. will be added. In parallel, a facility for realistic tests of the FE ASICS has been designed, built, and brought to operation.

The test-beam equipment for irradiation tests has been completed and used for irradiation studies of several sensor types. For the first time, the performance of a single crystal CVD diamond sensor was measured using the EUDET pixel telescope.

The laboratory equipment in Tel Aviv and the silicon lab in DESY have been upgraded. The laser position control system was further developed. A major step was the temperature stabilisation. Long term stability tests have been done and have shown that the stability of a small-size system is on the level of 1 μm.

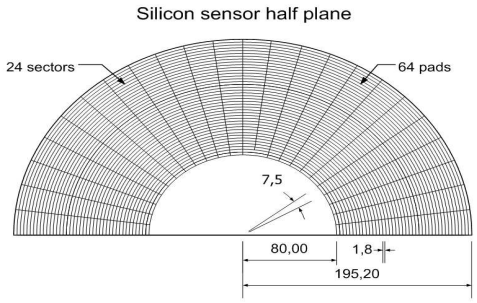

Figure 18: The structure of a LumiCal silicon sensor plane.

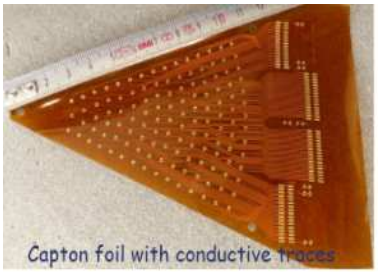

Figure 19: The prototype of a flexible PCB with traces for the signal transport.

Effort is ongoing to assembly full sensor planes. The prototype of a silcon sensor plane for LumiCal is designed and negotiations with companies for the production started.

Acknowledgement

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References

[1] H.Abramowicz, R.Ingbir, S.Kananov, A.Levy, I.Sadeh, "GEANT4 Simulation of the Electronic Readout Constraints for the Luminosity Detector of the ILC", EUDET-Memo-2007-12 and EUDET-Memo-2007-17.

[2] M. Idzik, K. Swientek, Sz. Kulis, J. Gajewski, L. Suszycki, "Readout Electronics for VFCAL", EUDET report, 2007,in preparation.

[3] K. Afanaciev et al., "Investigation of the Radiation Hardness of GaAs Sensors", EUDET report, in preparation.

[4] Ch. Grah et al., "Radiation Hard Sensors for the Beam Calorimeter of the ILC", submitted to the Proceedings of the IEEE Conference, Hawaii, USA 2007.

[5] J. Blocki, W. Daniluk, M. Gil, E. Kielar, J. Kotula, A. Moszczyski, K. Oliwa, B. Pawlik, M. Stypua, W. Wierba, L. Zawiejski, W. Slominski, L. Suszycki, M. Idzik, K. Swientek, "Status report: Laser Alignment System for LumiCal", EUDET-Memo-2007-39.

[6] J.Blocki, W.Daniluk, W. Dabrowski, M.Gil, M.Idzik, E.Kielar, J.Kotula, A.Moszczynski, K.Oliwa, B.Pawlik, L.Suszycki, K.Wientek, W. Wierba, L.Zawiejski, "Silicon sensors for the LumiCal prototype design", EUDET-Memo-2007-47.