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JRA-1 Milestone
IDC Prototype ready

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Abstract

The IDC Prototype[1], is the medium size sensor featuring the fast read-out architecture with digitised outputs needed for the final pixel sensors equipping the EUDET beam telescope. It was designed and fabricated in 2007, and came back from foundry in January 2008. It was successfuly characterised at IPHC/IReS and IRFU/DAPNIA, showing that the expected performances in terms of electronic noise, charge collection efficiency, charge-to-voltage conversion factor and read-out speed have been met.

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[1]alias MIMOSA-22, which stands for *Minimum Ionising MOS Active pixel sensor*, serial number 22.

1 Introduction

The EUDET beam telescope will be equipped with fast and high resolution pixel sensors allowing to provide high density particle tracking adapted to intense particle beams [1]. IDC, also called *MIMOSA-22*, is the final prototype of the part of the sensor architecture which includes charge sensing, average noise removal and analogue-to-digital conversion. It was designed and fabricated in 2007. Its main features are described in this paper, as well as the test results validating its functionnalities.
The architecture of IDC is based on the *MIMOSA-16* sensor [2], which is a fast binary readout Monolithic Active Pixel Sensor (MAPS) [3]. The sensor was designed in the AMSC35B4O1 CMOS-Opto 0.35 μm technology [4]. This technology has 4 metal layers and 2 poly layers. It relies on wafers featuring a $14\mu m$ thick epitaxial layer. The chip dimensions are 12.0 x 3.7 mm^2, including a charge sensitive area of 10.6 x 2.5 mm^2.

2 Description of the IDC sensor

IDC features a charge sensitive array of 136 columns and 576 rows of pixels. The latter have a pitch of 18.4 μm. 128 columns are ended with a discriminator featuring a common adjustable threshold for analogue-to-digital conversion. The remaining 8 columns have direct analogue outputs for functionnality tests and pixel characterization purposes. The outputs of the 128 column level discriminators are multiplexed by a serializer block onto 16 binary output pads. The pixel array is designed to be read out on a column parallel basis and row by row (i.e. rolling shutter mode) with a frequency of 6.25 MHz. The corresponding integration time is less than 100 μs.
In order to realise the final sensor with optimised performances, different diode dimensions, with and without radiation hard structures, have been implemented in the chip to find the best signal detection conditions, essentially governed by the signal-to-noise ratio (SNR). Moreover, three types of pixel architectures are implemented: one with a reset diode with common source amplifier, one with a self-biased feedback diode with common source amplifier, and one with feedback reset diode with common source amplifier. All of these pixels use the same clamping technique to achieve Correlated Double Sampling (CDS). The next section describes these different pixel architectures implemented in the chip.
Different functionnal modes of the chip, controlled by the digital sequencer and the circuit bias can be set and removed via a JTAG [5] controller [6]. The values of the discriminator threshold voltages can be set both via the JTAG controller and dedicated input pads.
Figure 1 represents a photograph of the chip.
Figure 2 shows the IDC functionnal view. It differs slightly from the final floor-plan, in which both the core and the pad ring were slightly modified in order to accommodate constraints emerging in the ultimate steps of the design.

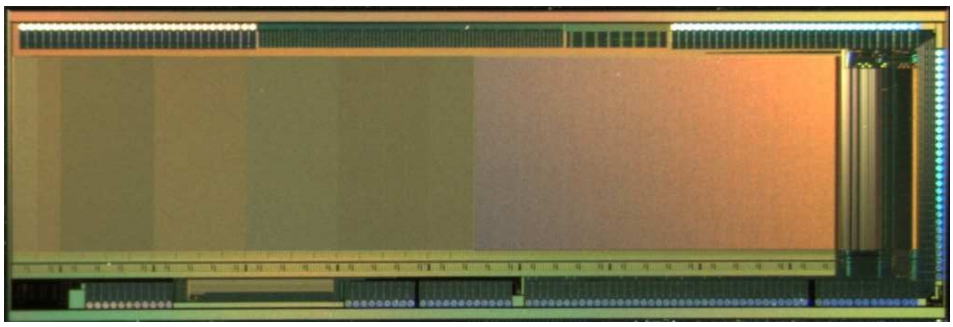

Figure 1: Photograph of the IDC sensor.

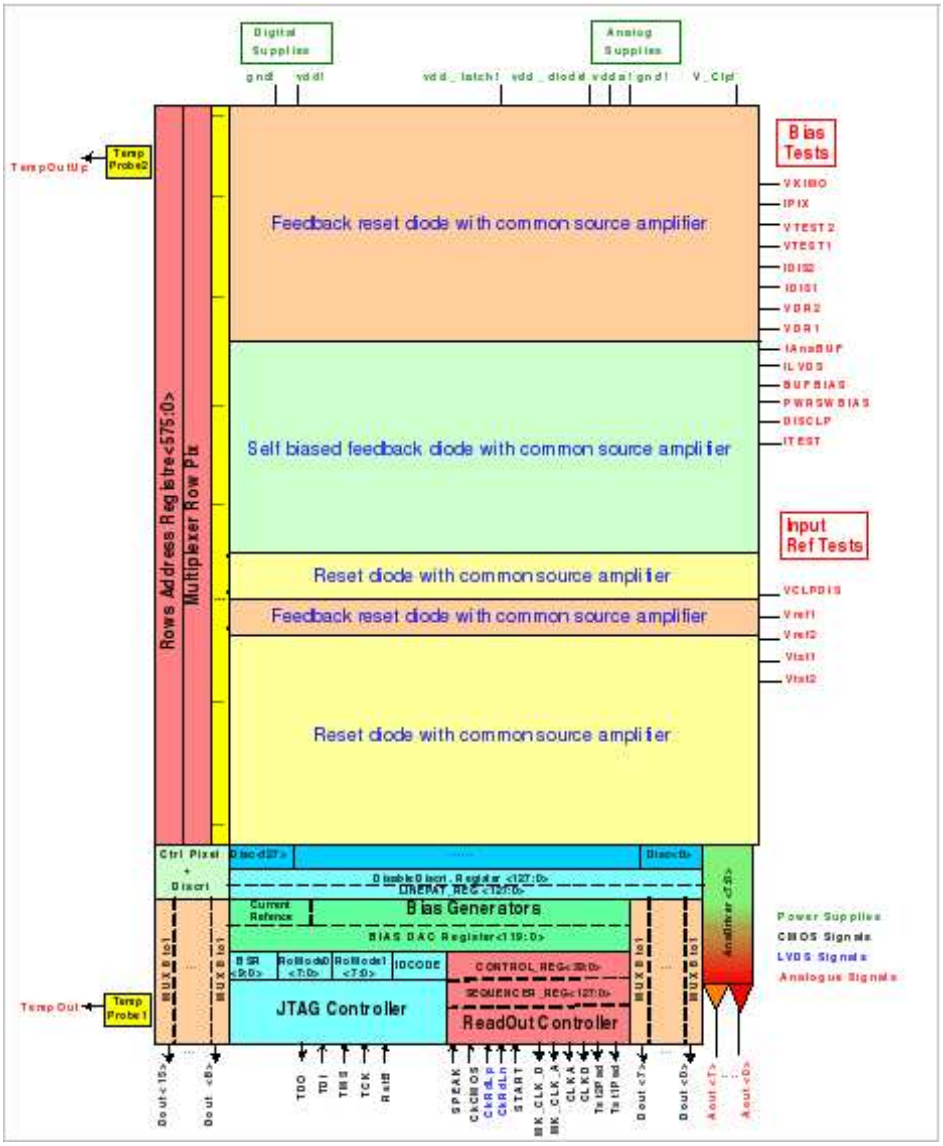

Figure 2: IDC functionnal view.

3 Description of the pixel architectures

3.1 Reset diode with common source amplifier

The pixel architecture is illustrated in Figure 3.

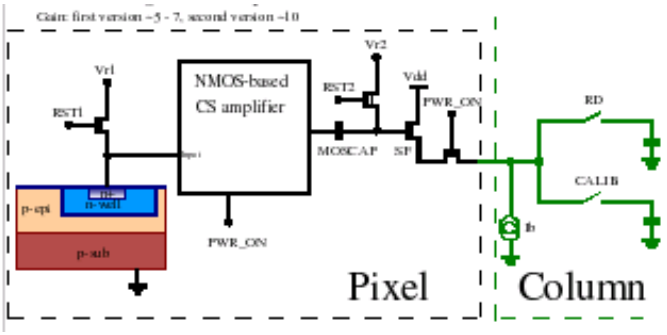

Figure 3: Main features of the pixel architecture with reset diode.

A CS (Common Source) pre-amplifying stage is located very close to the charge detection diode. Two versions of common source amplifier are implemented. The first version is a common source NMOS transistor with connected NMOS transistor load, both saturated in strong inversion. The second version has a common source NMOS transistor with improved load [7] composed of two NMOS transistors. The voltage gain of the first version is the ratio of the transconductances of the common source and load transistors. The transconductance of the improved load used in the second version of the amplifier is about twice larger, translating into a higher voltage gain. The DC current bias of the amplifier is determined by the voltage across the charge collecting diode, which is close to Vr1.
A double sampling circuitry is made up of this CS preamplifier, a serially connected capacitor (MOSCAP) and two reset switches. The first switch (RST1) is used to reset the sensing diode and the second one (RST2) is used to memorize on the capacitor the offset of the preamplifier and the reset level of the diode.
A SF (Source Follower) and a row select switch are used to output the signal on the common data bus. RD and CALIB are column level commands and are used to memorize the output signal level and the reference level of the pixel output stage, respectively.

3.2 Self-biased feedback diode with common source amplifier

The main singularity of this pixel is that the reset transistor is replaced by a diode. The charge sensitive element is a two diode system named self-biased diode. It features an n-well/p-epi diode collecting the charge delivered by the impinging particles, and a p-plus/n-well diode providing a constant reverse bias of the sensing diode.
In order to maximize the pixel SNR, the gain of the amplifier was increased as much as possible. The performance of the basic CS amplifier used in the first pixel is improved

using a load based on two NMOS transistors [7]. The AC gain of the modified CS amplifier is increased by a factor of two in this way, but the DC operation point and DC gain remain almost unchanged, which makes the circuit less sensitive to CMOS process variations. Moreover, a negative feedback is used to stabilize the operation point of the amplifier.
This pixel includes the same CDS circuit as described in section 3.1, with a serially connected clamping capacitor, a switch and a SF like in the previous pixel architecture. The main features of the pixel architecture are displayed in Figure 4.

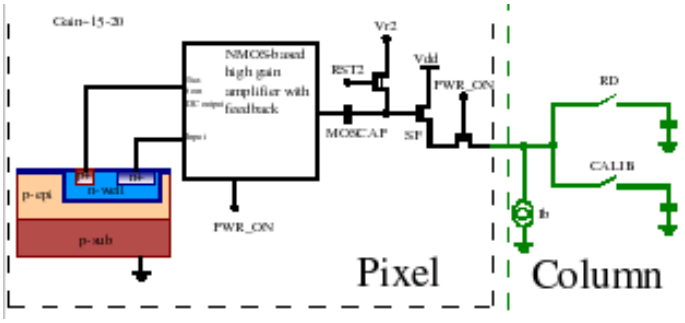

Figure 4: Main features of the pixel architecture based on a self-biased feedback diode.

3.3 Feedback reset diode with common source amplifier

The possibility to combine advantages of the "reset diode" and the "self-biased diode with feedback" schematics was investigated. In this approach, the reset transistor was used to set the working DC point for the amplifier [8]. In this way, the reset transistor generates a time-varying feedback: during the reset phase (where RST1 is high), the amplifier output is connected to the input (100% negative feedback), while during charge integration (where RST1 is low), the feedback is disconnected, and the gain is thus not reduced by the feedback. The amplifier uses an NMOS common source with improved load delivered by a pair of NMOS transistors [7]. The CDS and the readout are achieved in the same way as in the pixel architectures described previously. Figure 5 displays the main features of the architecture.

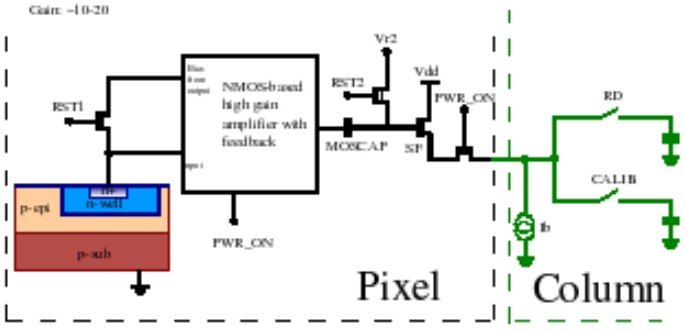

Figure 5: Main features of the pixel architecture based on a feedback reset diode.

3.4 N-well diode configurations

Different sizes of N-well diodes were implemented in the sensor, combined with each of the amplifier schematics, in order to search for optimal signal detection performances. A few pixels were also designed for improved tolerance to ionising radiation. This was achieved by enclosing the sensing diode and replacing the thick silicon oxide around the n-well by thin oxide.

3.5 Simulation of the pixel performances

The performances of all designs were evaluated with the SPECTRE circuit simulation software [9]. To simulate the charge sensing and signal processing, a charge was injected in the sensing diode with a current source and the signal after CDS was calculated with the TRAN analysis. The noise was simulated with the AC noise analysis. The results are summarised in Table 1. The sub–array designations are those used in the sensor user manual [6], which may be consulted for more details on each sub-array.

Sub-array	S1	S2	S3	S4	S5	S6	S7	S8	S9	S10	S11	S12	S13	S14	S15	S16	S17
CVC [$\mu V/e$]	99	89	82	80	83	54	54	51	57	70	72	70	64	68	64	36	34
N [μV]	728	590	561	570	558	830	828	811	852	544	518	543	440	449	439	318	313
N [e^-ENC]	7	7	7	7	7	15	15	16	15	8	7	8	7	7	7	9	9
I_{Amp} [μA]	5	5	7	7	7	7	7	7	7	7	9	7	7	4	7	7	7

Table 1: Simulation of pixel performances: values of the charge-to-voltage conversion factor (CVC), of the noise (N) and of the amplifier current (I_{Amp}) for each of the 17 pixel design variants.

4 Test results

4.1 Introduction

Several sensors were characterised on a test bench at IPHC (Strasbourg) and IRFU (Saclay)[2]. The tests addressed the most essential questions concerning the fast chip architecture to be cleared out before designing the final telescope sensor. These major test objectives are summarised hereafter:

- demonstrate that the full chip operation (including charge sensing, in-pixel CDS and signal discrimination) is performing according to the requirements in all 128 columns simultaneously, in particular that the full chain noise is below 15 e^-ENC

[2]formerly called DAPNIA.

at nominal clock frequency (100 MHz) and that the dispersion between columns (e.g. discriminator thresholds) is substantialy lower than the pixel noise;

- find at least one optimally adapted pixel architecture among the 17 variants implemented in the chip;
- assess the temperature dependence of the chip performance;
- estimate the dispersion of performances between different chips and over their surface.

4.2 Main features of the test procedure

- all measurements were performed at the nominal clock frequency of 100 MHz, corresponding to a read-out time of the complete array of 92.5 μs;
- the chips tested were mounted inside a box protecting them from visible light;
- the chips were operated at a well controled temperature, obtained by circulating a coolant through a pipe traversing the box in which the chip was mounted;
- some measurements were performed by illuminating the chip under tests with a ^{55}Fe source.

All noise values provided in the paper still contain the contribution from the read-out chain.

4.3 Tests of the analog outputs

The pixel noise observed in the best performing sub-arrays ranged typically from $\gtrsim 10$ to 14 e$^-$ENC. The noise values obtained with the best performing pixels of the two main types (self-biased feedback diode and reset diode with standard common source amplifier) are summarised in Table 2, for a coolant temperature of 15°C, translating in a temperature of 20°C at the chip surface. The table also provides CCE measurements performed with clusters of 2x2, 3x3 and 5x5 pixels illuminated with an ^{55}Fe source.
The comparison between different measurements involves a measurement accuracy on the noise of typically $\pm$ 0.3 e$^-$ENC. The charge collection efficiencies were estimated with a typical uncertainty of $\pm$ 0.5 %.
Overall, the noise performance of several different pixel designs is very satisfactory. One observes that the self-biased pixels (S6–S9) and the reset pixels exhibit nearly the same temporal noise. The most significant noise variations originate either from the sensing diode size (i.e. S9 versus S8) or from the (non-)radiation tolerant design (S7 versus S6, S12 versus S10). In particular, the comparison between the temporal noise values of sub-arrays S6 and S7 shows that the radiation tolerant design increases the temporal noise of the self-baised pixels by about 1 e$^-$ENC only. The values obtained for the CCE reflect the expectations and are satisfactory for all 8 pixel designs considered in the table.

Sub-array	diode surface	rad. tol. diode	pixel type	Noise [e$^-$ENC]	Charge collection efficiency 2x2 pixels	3x3 pixels	5x5 pixels
S6	14.6 μm^2	yes	SB	12.4	57 %	73 %	84 %
S7	14.6 μm^2	no	SB	11.4	58 %	75 %	85 %
S8	19.4 μm^2	no	SB	12.8	65 %	82 %	90 %
S9	11.6 μm^2	no	SB	10.5	54 %	72 %	83 %
S10	15.2 μm^2	yes	reset	13.3	60 %	77 %	86 %
S12	15.2 μm^2	no	reset	11.8	58 %	75 %	84 %
S13	15.2 μm^2	yes	reset	13.5	–	72 %	84 %
S15	15.2 μm^2	no	reset	12.5	–	73 %	85 %

Table 2: Temporal noise and charge collection efficiency observed with some of the pixel arrays. S6–S9 include self-biased (SB) pixels, while S10–S15 include reset pixels. The values shown for S13 and S15 were obtained in slightly different conditions than those for sub-arrays S6–S12.

Dispersion between chips: The dispersion of the performances between different sensors was addressed by comparing the observed noise and CCE values measured with 5 different chips. The results are summarised in Table 3.

Sub-array	Chip number	Noise [ENC]	Charge collection efficiency 2x2 pixels	3x3 pixels	5x5 pixels
S6	1	12.5 e$^-$	58 %	75 %	86 %
	2	12.3 e$^-$	58 %	75 %	86 %
	3	12.3 e$^-$	59 %	76 %	87 %
	6	12.4 e$^-$	57 %	75 %	85 %
	7	13.6 e$^-$	58 %	76 %	86 %
S10	1	13.4 e$^-$	59 %	76 %	86 %
	2	13.6 e$^-$	59 %	77 %	87 %
	3	13.2 e$^-$	60 %	78 %	88 %
	6	13.8 e$^-$	59 %	77 %	87 %
	7	14.1 e$^-$	59 %	77 %	87 %

Table 3: Temporal noise and CCE observed with 5 different sensors.The values are shown for the sub-arrays S6 (SB radiation tolerant pixels) and S10 (radiation tolerant reset pixels).

The comparison shows that the noise performance varies by only a few per-cent from

chip to chip and that the CCE differs typically by a negligible amount of 1 or 2 per-cent.

Sensitivity to operating temperature: The sensors were operated at three different temperatures of the coolant: 0°C, +15°C and +30°C. The corresponding temperatures at the chip surface were measured to be about +10°C, +20°C and +35°C respectively. The temperature dependence observed for the average noise and CCE of sub-arrays S6 and S10 are summarised in Table 4.

Sub-array	T [°C] coolant / chip	Noise [ENC]	Charge collection efficiency 2x2 pixels	3x3 pixels	5x5 pixels
S6	0 / 10	12.5 e^-	58 %	75 %	85 %
	15 / 20	12.6 e^-	58 %	74%	85%
	30 / 35	13.0 e^-	59 %	76 %	80 %
S10	0 / 10	12.8 e^-	59 %	77 %	84 %
	15 / 20	13.5 e^-	59 %	76 %	86 %
	30 / 35	14.2 e^-	60 %	76 %	86 %

Table 4: Temperature dependence of the noise and CCE for sub-arrays S6 and S10. The temperature values are those of the coolant and of the chip surface.

Summarising, the temporal noise increases by $\sim$ 0.5 e^-ENC over the full temperature range for the self-biased pixel. It increases by more than 1 e^-ENC for the reset pixel. The difference between the two pixel designs came out as foreseen. Also as expected, the CCE is almost unaffected by the temperature change in the range considered.

Conclusions on the pixel performances: The pixel array is operational at the nominal clock frequency while operated at room temperature. It exhibits very satisfactory performances. The average temporal noise, which is one of the most important parameters addressed by the prototyping, amounts typically to 10.5–12.5 e^-ENC for standard diodes, depending on their dimensions. Radiation tolerant diodes exhibit a noise value which is typically in the range 12.5–13.5 e^-ENC. The self-bias diodes lead to about 0.5 e^-ENC less temporal noise than the reset pixels.
The charge collection efficiency is smoothly depending on the sensing diode dimensions in the range considered. Moreover, this soft dependence translates into a still alleviated effect on the signal-to-noise ratio once the charge-to-voltage conversion gain is accounted for.

4.4 Tests of the digital outputs

The 128 digital outputs of the sensor were analysed in two steps. First the discriminator performances were studied independently from the pixel array. Next, the full chain,

including the pixels and the discriminators, was assessed. Unless quoted otherwise, the chips were operated with +15°C coolant temperature.

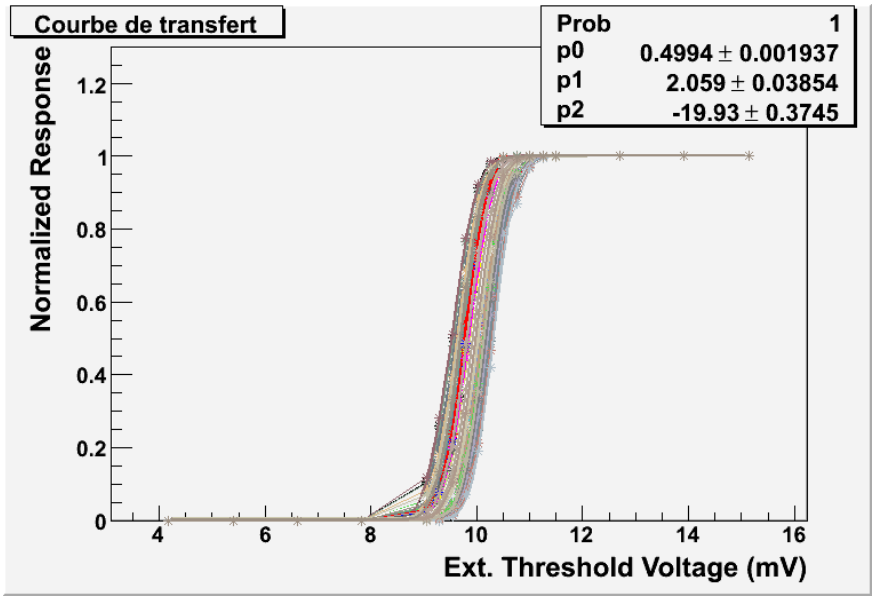

Figure 6: Transfer function of the 128 discriminators when applying a uniform 10 mV voltage at their inputs.

Tests of the isolated digital outputs: A uniform voltage of 10 mV was injected in the 128 discriminators and their transfer functions were evaluated. The responses of all discriminators are shown on Figure 6.
The temporal noise of each discriminator was derived from this measurement as well as the threshold dispersion between the discriminators. The distributions obtained are displayed on Figure 7. The observed temporal noise amounts to ~ 0.35 mV, while the threshold dispersion translates into a fixed pattern noise of ~ 0.25 mV. These results reproduce well those obtained with the MIMOSA-16 prototype [2], which was equipped with the same discriminators.

Tests of the complete chain: The threshold scan was repeated with all pixels activated, in absence of the radioactive source. The dispersions observed thus combine the pixel and the discriminator noise contributions. The chip operating temperature was near +15°C. The measurement results are illustrated in Figure 8, which displays the observations made with sub-array S7 and S12.

The temporal noise derived from this measurement is about 0.6 mV (corresponding to $\sim$ 12 e^-ENC) and the fixed pattern noise due to the threshold dispersion was estimated to $\lesssim 0.3$ mV. These values match the requirements well. Their distributions are illustrated in Figure 9 with the measurements of sub-array S7.

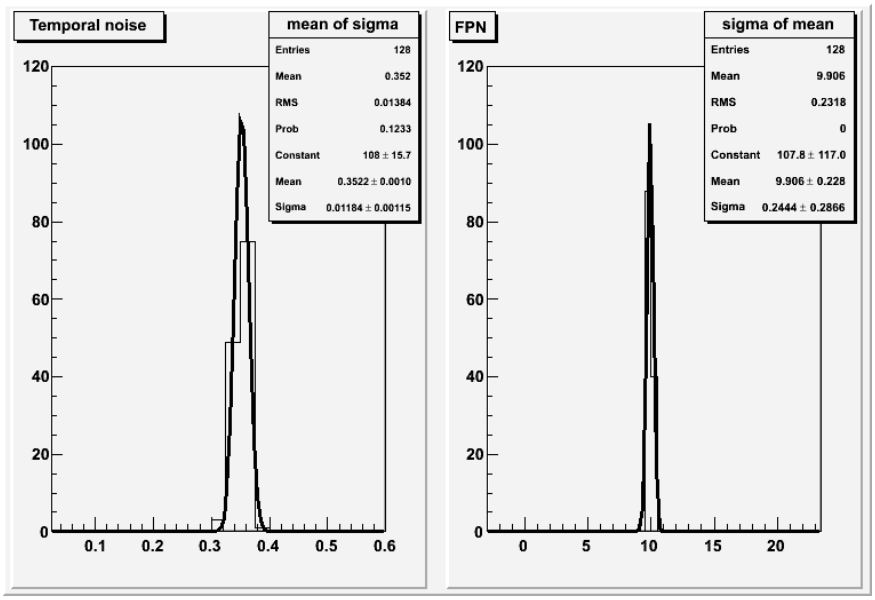

Figure 7: Temporal noise (left) and fixed pattern noise (right) of the 128 discriminators when appyling a uniform 10 mV voltage at their inputs.

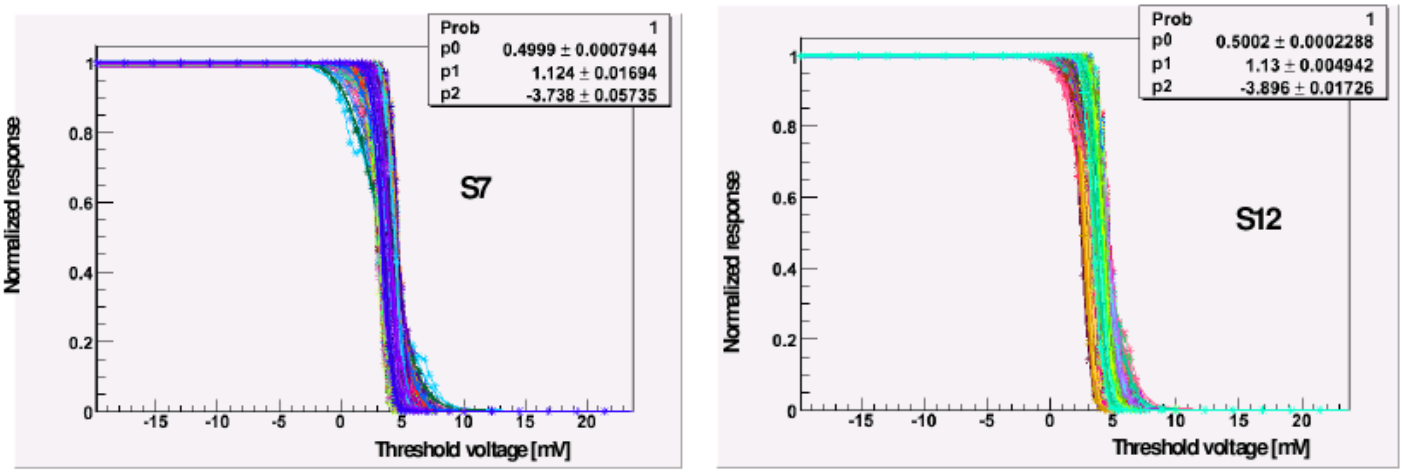

Figure 8: Threshold scan of the 128 discriminators when connected to the pixel array. The latter not being illuminated by any source, the discriminators react only to the pixel noise (here sub-arrays S7 and S12).

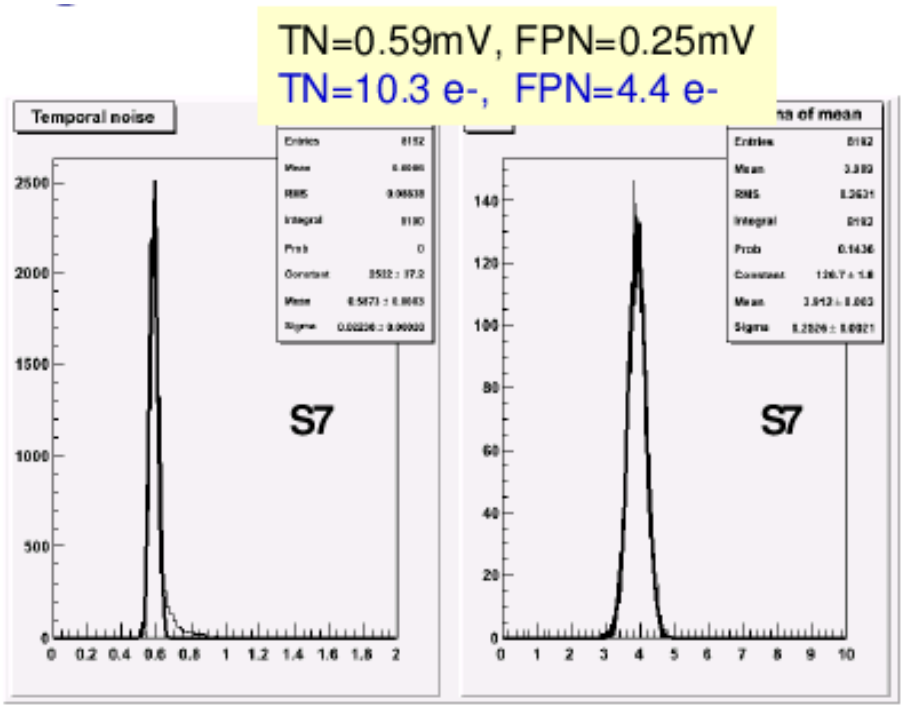

Figure 9: Temporal noise (left) and fixed pattern noise (right) of the 128 discriminators when connected to the pixel array (sub-array S7).

5 Summary

IDC, the final prototype sensor featuring the fast pixel array with digital output required for the EUDET telescope, was designed and fabricated in 2007. It features 128 columns of 576 pixels (18.4 μm pitch), each ended by a discriminator. 8 additionnal columns are not terminated with a discriminator (analogue outputs), in order to allow direct pixel characterisation. Various pixel designs were incorporated in the sensor in order to find the one best adapted to the EUDET telescope running conditions.
The main functionnalities of the sensor were tested at IPHC-Strasbourg and IRFU-Saclay, and found fully operationnal at the nominal clock frequency of 100 MHz. The noise of the different pixel designs integrated in the chip was evaluated. For most of the matrices, low noise values, in the range 10.5–13.5 e^-ENC, were observed at room temperature. The CCE was also found to be fully satisfactory. Several pixels suited to the EUDET telescope running conditions could thus be designated.
The discriminator performances were also assessed, combined with the pixel array. Their temporal and fixed pattern noises reproduce the values observed with the previous prototype generation and increase only marginaly the pixel noise. The overall performances of the sensor are thus very satisfactory. The complete sensor architecture is therefore validated and ready to be combined with the data compression micro-circuit SDC-2 in a single device which will equip the EUDET beam telescope.

References

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