



A Prototype for TDC-based Readout Electronics for the LP TPC

A. Kaukher*, O. Schäfer, H. Schröder, R. Wurth

Institut für Physik, Universität Rostock, Germany

May 1, 2008

Abstract

The Readout Prototype described in this memo sets a milestone for the development of the TDC-based readout electronics for the Large Prototype TPC. The Readout Prototype was designed in 2007 and manufactured early 2008.

*Alexander.Kaukher@desy.de

1 Introduction

A readout electronics prototype has been defined to be a test printed circuit board (PCB) which has all necessary features of the targeted multichannel electronics[1]. The schematics and the design rules meant to be as close as possible to the final version. Even there was no constrain on the size of the PCB, most of the components were intend to be placed in such a way that they would fit in the area of the future “Barcelona”-board.

2 Readout Electronics Prototype

A photo of an assembled readout electronics prototype - the Chip Tester - is shown on the Figure 1. The name is due to a feature of the board - a clam-shell socket for TQFP64 package of ASDQ ASIC.

The size of the board is 116 mm × 82 mm. Two ASDQ ASICs can be installed on the board - one into the clam-shell socket and another one can be soldered on the board directly. The Figure 1 shows only one ASDQ chip placed into the clam-shell.

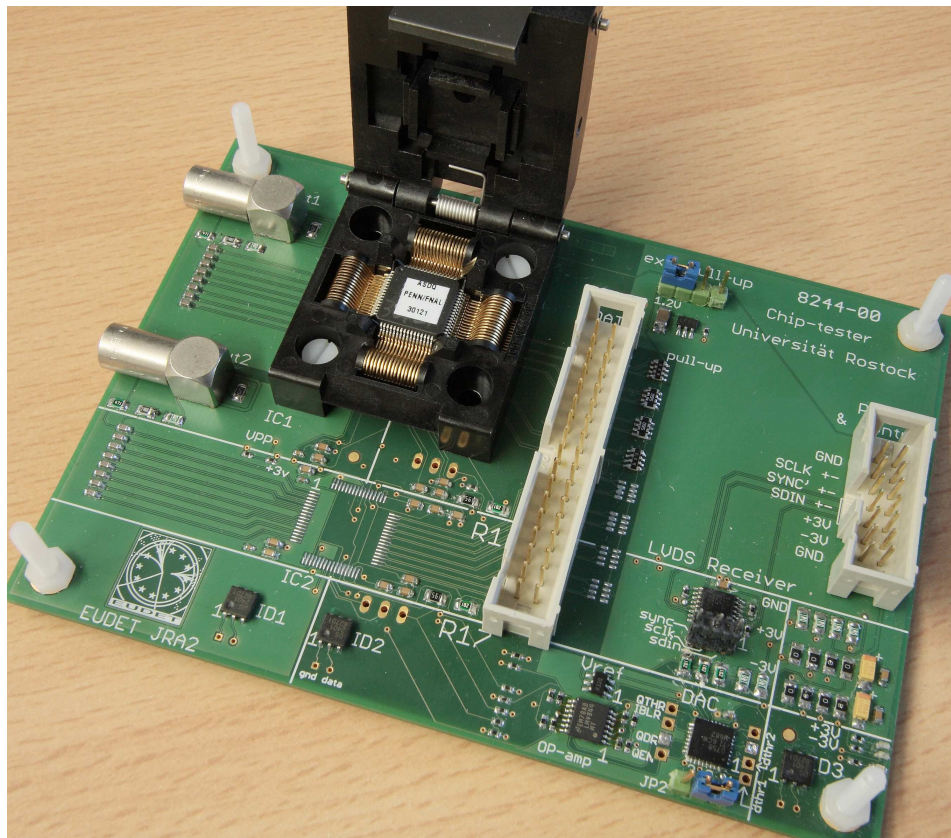


Figure 1: Photo of the Readout Electronics Prototype: The Chip Tester.

A simple charge injector circuit is used to provide signals to ASDQ chips. The charge injector has a voltage divider shared by all channels and a capacitor for every channel of an ASDQ chip. Signals from both ASDQs are routed to a single output connector. Type of the output connector is chosen to be compatible with existing twisted pair cables and is not the one foreseen for the final design.

Evaluation of components for the “Barcelona”-boards and placement study

Control potentials are supplied by a Digital-to-Analog Converter (DAC). Eight channel DAC7558[2] from Texas Instruments is used for this purpose. Main features of the DAC are: low voltage operation, serial digital interface, ultra low digital feedthrough and compact QFN package. Two DAC channels are used to supply threshold potentials to two ASDQ chips of the Chip Tester. In the case of the “Barcelona”-board, four DAC channels will supply threshold potentials for four ASDQ chips, this will allow to trim thresholds individually. Another four DAC channels are used for common control of all ASDQs.

Common control DAC outputs are buffered using a simple operational amplifier, LM324[3]. First test shown, that a rail-to-rail operational amplifier is required. LMV844[3] from National Semiconductors was found to be pin compatible and not expensive replacement of LM324.

The output of the ASDQ is open collector, thus interface to CAEN v1190 VME TDC requires pull-up resistors and a certain pull-up potential. With help of the Chip Tester, pull-up resistors of 56Ω were selected. Among all alternatives this value of available resistors fulfills requirement on the termination of the transmission lines, however leads to somewhat higher power consumption.

Value of the resistor which controls driver current of the ASDQ was selected by counting signals from the Chip Tester with help of the VME TDC. Signals from a pulse generator were supplied to the Chip Tester and the trigger channel of the VME TDC. Output of the Chip Tester was connected to the TDC with 4-meter long twisted pair cable. Full efficiency of signal counting has been achieved with driver current set by a $2\text{ k}\Omega$ resistor.

The footprint of an ASDQ chip has been positioned in such a way that the chip and all required passive components would fit within 15 mm width of the Chip Tester, without limitation on the length. This demonstrated feasibility of placement four ASDQ chips on a 30 mm wide PCB. All other components, including DAC and LVDS receiver were placed within 30 mm width of the Chip Tester, Figure 1.

Communication interface

The interface to the Readout Prototype, as well as for “Barcelona”-board, uses Low Voltage Differential Signaling (LVDS) technique. An LVDS receiver SN65LVDS32 is used for this purpose. Signals from the receiver have TTL-levels with fast rise and fall edges. A resistor in series is placed on every output of the receiver, in order to decrease slopes of the TTL signals, thus improve signal integrity on the board.

SPI-compatible digital interface of the DAC has been programmed using bit-banging technique. Software approach does not allow to use high speed communication, but at the same time does not require special hardware on this stage of the prototyping. Three port lines of a FOX-board[4] are used for this purpose. Low voltage TTL signals from the FOX-board are converted to LVDS signals with the help of an LVDS transmitter, installed on a prototype board.

Other features of the Chip Tester

Unique identification of a “Barcelona”-board will be possible using silicon serial number - an electronic chip with a unique registration number written in it. A DS2401[5] chip from Maxim is used in the Chip Tester and will be replaced later by a digital temperature sensor (for example DS18B20[5]) from the same company, communication to which can be also established with help of the FOX-board. The DS18B20 temperature sensor has a unique serial code stored in ROM, what also can be used for identification of “Barcelona”-boards.

An ASDQ chip has analogue monitor pins for its channel number eight, what enables study of signals before the ASDQ’s discriminator. Those signals are routed from both ASDQ chips of the Chip Tester and can be connected to an oscilloscope using specially designed ASDQ Analogue Monitor board.

Maximum measured current to the Chip Tester with only one ASDQ chip (in the clamshell) is 90 mA (+3 volt) and 82 mA (-3 volt).

3 Mechanical outlines of the “Barcelona”-board and Pitch Adapter

The placement and the routing of the “Barcelona”-board and the Pitch Adapter has been finished and dimensions of the boards were fixed. Outline of a Barcelona board is shown on the Figure 2.

Outline of a Pitch Adapter board is shown on the Figure 3. Dimensions of the boards will be later used for planning of the support structure of the electronics and cables.

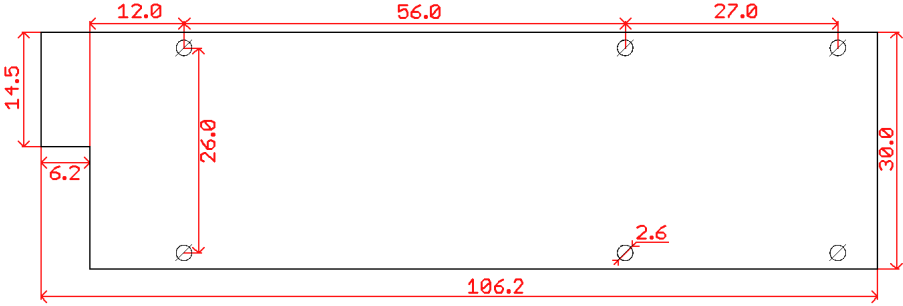


Figure 2: Outline of a “Barcelona”-board.

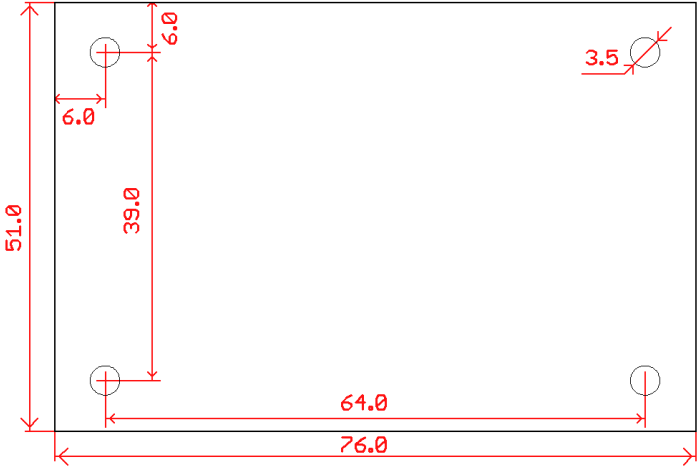


Figure 3: Outline of a Pitch Adapter board.

4 Test of the data acquisition system with the DESY test-beam

First prototype of the data acquisition software has been tested on the DESY test-beam TB24/1[6]. Peak rate of coincidence signal from two scintillating counters was measured with CAEN TDC v1190. Flat counters of size $20 \times 20 \text{ cm}^2$ were installed next to each other, and the overlap area visible by the beam was $10 \times 10 \text{ cm}^2$. The collimator was fully open.

The highest average signal rate observed for 3 GeV beam was $\approx 13 \text{ kHz}$. The highest observed peak rate was $\approx 14 \text{ kHz}$. Analysis of data has shown, that in some rare cases data acquisition software reads the same value from the TDC twice. This sets no problem for data processing, but so far the source of the effect was not found.

Study of DESY II beam time structure

DESY II accelerator accelerates/decelerates beams with period of 80 ms. In order to be able to measure longer time intervals, a signal from a pulse generator was provided to another channel of the TDC. The frequency of this “reference” signal was 20 kHz. This signal “appears” twice during the time range of the TDC. This allows to perform “time stitching” using offline software, and thus the measurement of time intervals longer than the range of the TDC ($\approx 100 \mu\text{s}$).

Figure 4 shows arrival time of particles within first 2.5 s. Due to the test beam optics, particles of selected energy will reach test-beam area only during a certain time interval after the beginning of the cycle. The time interval between particles for the beam energy of 6 GeV is shown on Figure 5. The histogram shows time interval between consecutive particle arrival time measurements. The time interval “free of particles” in this case is $\approx 60 \text{ ms}$. For the beam energy of 1 GeV this time is $\approx 20 \text{ ms}$.

This specific time structure of the DESY test beam can be useful for power pulsing option study of TPC readout electronics.

5 Conclusion

A Readout Prototype of TDC-based readout electronics has been built. This sets a milestone for the development of TDC-based readout electronics. The Chip Tester will be used in the future to select ASDQ chips which will have to be soldered onto the “Barcelona”-boards.

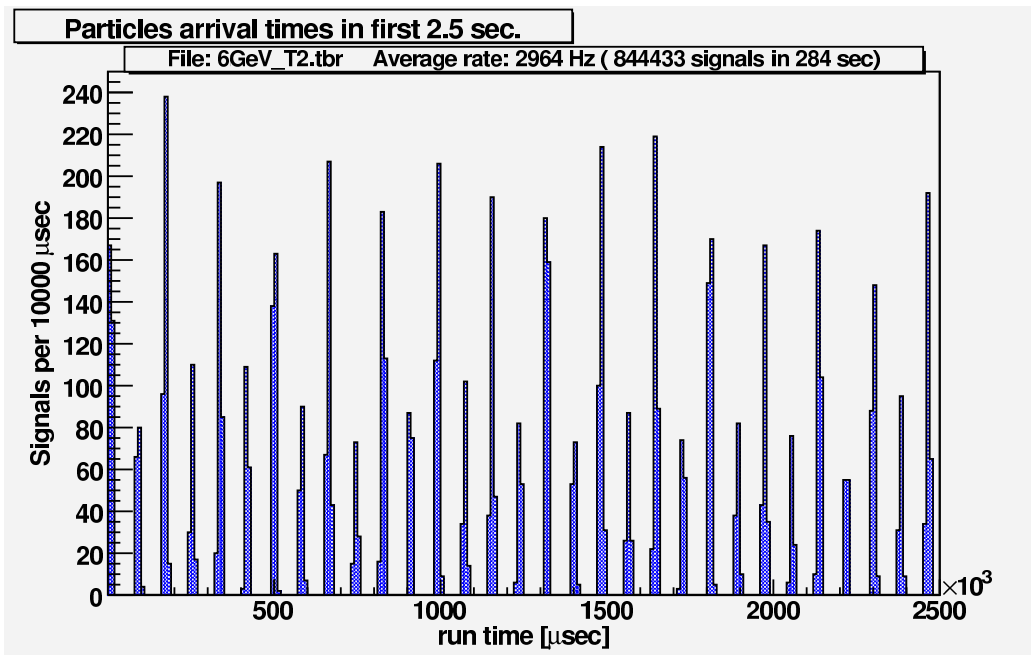


Figure 4: Time structure of the DESY 6 GeV test beam.

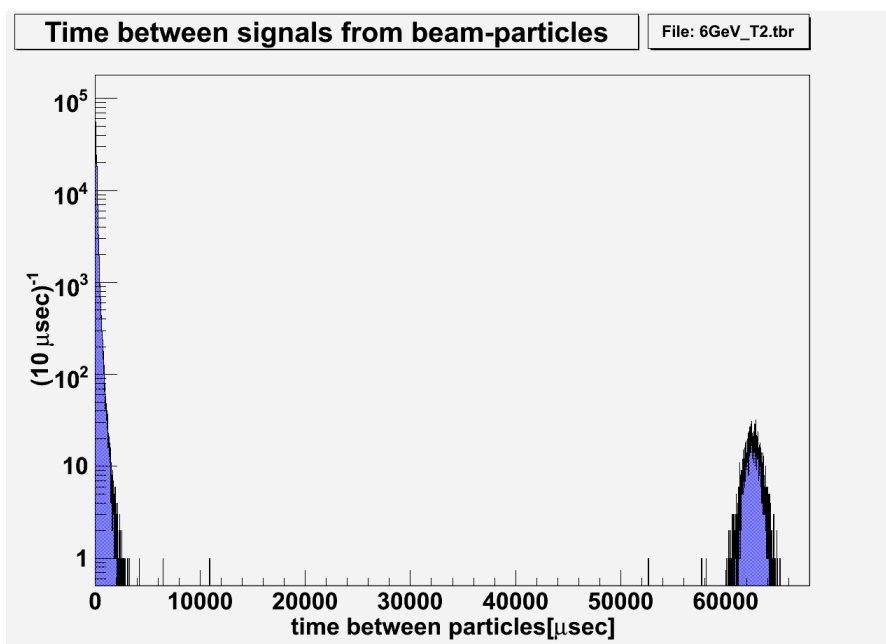


Figure 5: Time interval between particles in the DESY 6 GeV test beam.

Acknowledgement

This work is supported by the Commission of the European Communities under the 6th Framework Programme "Structuring the European Research Area", contract number RII3-026126.

References

- [1] A. Kaukher, O. Schäfer, H. Schröder, R. Wurth, "Status Report on TDC-based readout electronics for the LP TPC", EUDET-Memo-2007-38
- [2] <http://www.ti.com>
- [3] <http://www.national.com>
- [4] <http://www.acmesystems.it>
- [5] <http://www.maxim-ic.com>
- [6] T. Behnke, E. Garutti, I. M. Gregor, T. Haas, U. Kötz, I. A. Melzer-Pellmann, N. Meyners, J. Mnich, F. Sefkow, "Test Beams at DESY", EUDET-Memo-2007-11

Update: September 17, 2008

ASDQ selection with the Chip Tester

With help of the Chip Tester, ASDQ chips were selected for installation onto the "Barcelona"-boards. Procedure of selection included following steps:

- optical inspection
- check of power consumption
- counting signals with TDC
- analysis of time and charge measurements for a defined condition on the input

164 out of 200 chips fulfilled criteria on uniformity of the time and charge measurement, however only 120 will be used for installation on 30 "Barcelona"-boards.