



A General Purpose Electronic readout system for tests of Time Projection Chambers, equipped with different avalanche multiplication systems.

Report given at the annual EUDET meeting at NIKHEF, Amsterdam, October 6-8 2008.

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December 17, 2008

Abstract

The report describes the 2048 channel electronic readout system developed within the EUDET project as a general readout system for tests of different readout concepts of a Time Projection Chamber. The design characteristics, experiences from prototyping and the final tests on a small Time Projection Chamber are reported. A system noise level, corresponding to an RMS noise of 370 electrons has been achieved for a 128 channel prototype operating on a TPC chamber. The perspective of extending the system to 10000 channels is discussed as well and the planned mechanical assembly.

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1. Introduction

A large volume Time Projection Chamber (TPC) offers possibilities to match the exceptional requirements on momentum resolution for spectroscopic measurements at large transverse momenta in a future linear e^+e^- collider experiment. Even for a TPC, the momentum as well as the nearby track resolution have to be substantially better than in today's TPCs in order to satisfy the design criteria.

This calls for new solutions of the TPC readout technology, which up to now, generally has been based on Multi Wire Proportional Chambers (MWPCs), equipped with pad readout on the segmented outer cathode. This readout technique has limitations imposed by the large image charge, different position response across and along the wires, distortions due to the interplay between the electric and magnetic fields (ExB effect) within in the MWPC and rate limitations due to ion feedback.

Novel gas detector techniques with avalanche multiplication like GEM (Gas Electron Multiplier) and Micromegas detectors promise substantial improvements on these aspects. In particular, the lateral spread of the avalanche signal is small (few millimeters) and the absence of a long ion tail on the pulse confines the information also in the time dimension. To fully benefit from this, the readout should be made with substantially smaller (a factor 10 to 20) pads than used in today's MWPC readout. Small pad size is beneficial both for momentum and nearby track resolution point of view.

The main challenges in recent years detector development for pp experiments at LHC have been sensitivity and rate capability so that the extremely large luminosity, by which rare phenomena can be produced, can be fully exploited. Thus, detectors with long drift times (like TPCs) have been unsuitable.

Heavy Ion collisions at the LHC are however governed by much lower luminosities than pp and the minimum bias collision rates will be only ca 10kHz. Also this is much larger than the anticipated collision rate at a linear collider, but still compatible with a large volume TPC if it is gated on triggered events only. The main tracking detector in the ALICE experiment is an 88m^3 TPC with MWPC readout [1]. The requirements on momentum resolution for Heavy Ion physics are not as high as for the linear collider. However, as high energy heavy ion collisions produce an enormous number of particles, the nearby track resolution is as challenging as in a linear collider experiment. TPCs with MWPC readout are limited by the pad size, governed by the size of the image charge, in this respect. The number of channels in the ALICE electronic readout system is very large (500k channels) however still about an order of magnitude lower than anticipated for the LCTPC (Linear Collider TPC).

For the design of general purpose readout system for the EUDET TPC tests it has thus been very beneficial to be able profit from the development done for ALICE. Thus it has been possible to construct a readout system with the performance of a large collider experiment for the more moderate situation of beam tests at the beam line at DESY.

The final electronics, must be miniaturized substantially compared to the present system. Presumably all readout electronics for a channel must fit behind the pad that it serves, i.e. must not occupy a footprint larger than about 6mm^2 . Basically all front end functions must be integrated in the same chip. The ASICs developed for the EUDET TPC-readout, constitute a valuable starting point for such further integration.

2. System description

Fig 1 shows schematically the layout of the complete data acquisition system (DAQ). In this paper we will focus on the front end electronics i.e. the pulse processing and data handling on the detector itself. This includes amplification and digitization, local event storage and formatting of data for serial transfer, off the detector via optical fiber. Special

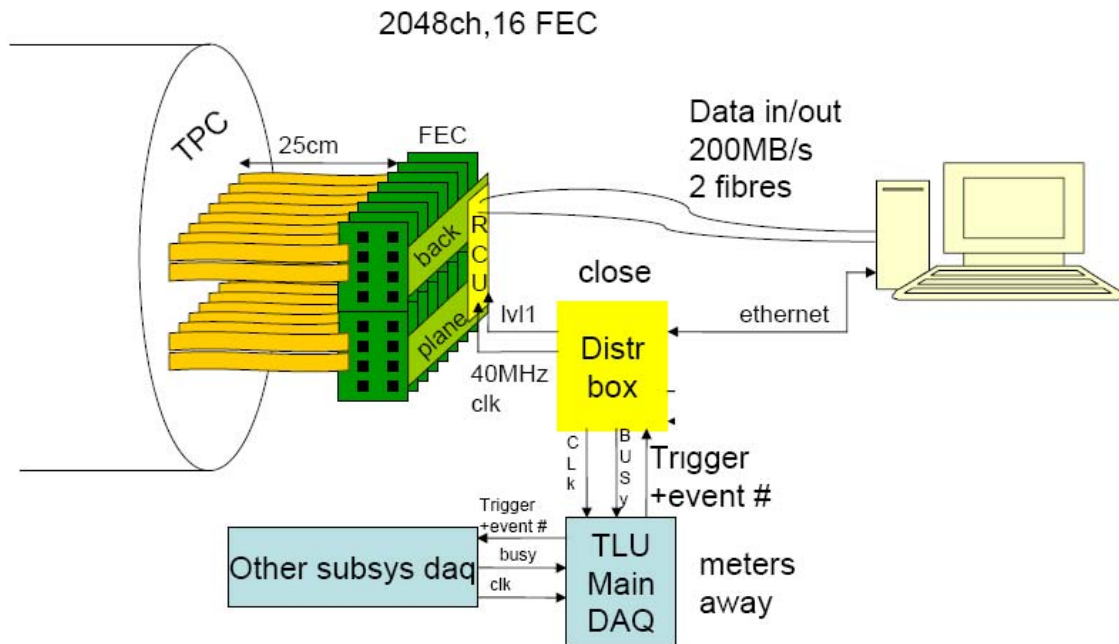


Fig 1. Schematic layout of a 2048 channel system, showing the different blocks of the DAQ system. The front end electronics is directly attached to the TPC.

attention is paid to the changes made relative to the ALICE front end electronics [1]. Details of other parts of the DAQ, e.g. Timing Logic Unit (TLU), distribution box and Main DAQ are described in detail in other contributions.

The Front End electronics is adapted to an architecture, typical for the DAQ in a modern collider experiment. In this application, where the event rate is not a major concern, the DAQ will be used as in a fixed target experiment i.e. receipt of a trigger, starts digitization of an event (which is 1000 time samples of the analog waveform) and a busy is asserted which inhibits further triggers until readout of the event is completed.

Upon receipt of a 1st level trigger, the analog waveform from the PCA16 analog ASIC is digitized by the ALTRO ASIC in a sequence of 1000, 10 bit samples which are stored in the ALTRO, until readout. The sampling frequency can be chosen to be 5,10 or 20MHz with full voltage resolution. 40MHz operation is possible at a loss of resolution to about 8.5 bits. 10-12 FEC will be equipped with a high speed version of the ALTRO which can operate at 40MHz with almost full 10 bit resolution. Operation at 40MHz has not yet been verified by prototypes.

There are two types of ASICs on the FEC, the newly developed PCA16 preamplifier-shaper chip and the ALTRO which performs the AD-conversion of 1000 consecutive samples. The ALTRO chip is the same as being used for readout of the ALICE TPC. The limited number of ALTROs, operable at 40MHz with full resolution, are however slightly modified compared to the ALICE version of the chip.

2.1 The programmable Charge Amplifier chip, PCA16.

The PCA16 charge amplifier chip has been equipped with several important features programmable. With the implementation chosen, the programming is done remotely. The programmability makes the PCA16 chips ideal for the purpose of the EUDET TPC-electronics i.e. to provide a general purpose DAQ system by which many different readout techniques can be tested, evaluated and optimized. The acronym PCA16 stands for the 16 channel version of the **P**rogrammable **C**harge **A**mplifier.

The characteristics of the PCA16 in summary are:

- 1.5 V supply; power ~8 mW/channel
- 0.13 μ m CMOS process
- 16 channel charge preamp + shaper
- Ca 300 electrons noise at 10pF
- single ended charge input, differential output
- Programmable features
 - input signal polarity
 - Power down mode (wake-up time = 1 ms)
 - Peaking time between 30 and 120 ns (7 steps)
 - Gain between 12 –27 mV/fC (4 steps)
 - Preamplifier output mode (bypasses shaper)
 - Tunable decay constant of the preamplifier output

The possibility to bypass the shaper allows the timing characteristics of the electron arrival from the drift volume in the TPC to be preserved.

2.2 The ALTRO digitizer-drift storage chip

The characteristics of the ALTRO digitizer chip has been described in detail elsewhere [1,2] as it is unchanged from the ALICE version. Some features, like cancellation of the

long ion tail of MWPC signals are disabled when GEM or Micromegas chambers are read out.

The ALTRO characteristics in summary:

- 2.5 V supply. 20-40mW per channel depending on sampling frequency
- 0.250 μ m CMOS technology
- differential input
- 16 channels per chip
- 10 bit resolution, typically 1mV per ADC channel
- 1k samples per event
- sampling at 5,10 or 20MHz at full resolution
- pedestal subtraction, common to all samples
- powerful zero suppression-good data is sequence (selectable) of non-zero samples.
- stored pulse data, + pre samples and post samples
- 4-8 event buffering. (multi event buffering will not be used here)

A limited number of modified ALTRO chips with enhanced performance at sampling freq. 40MHz are available. About 1280 channels (10FECs) will be equipped with these modified ALTROs to be used to instrument a high time resolution part of the test TPC endcap.

2.3 The EUDET-specific FEC

Figure 3 shows a photograph of the assembled FEC with the Kapton cables which connect to the pad plane, mounted.

The PCA16 chip is pin-compatible with the PASA (preamp-shaper chip used for the ALICE-TPC), except for the 9 programming pins which are for PCA16 only. The routing of noise sensitive signal traces could thus be kept identical to that of the ALICE FEC. Thus, we could benefit from the successful noise reduction work, invested in the ALICE TPC-FEC.

The major changes implemented on the EUDET-FEC, compared to the ALICE-FEC, are related to the programmability of the PCA16 chip. Fig 4 shows schematically the additional circuitry needed for the PCA16 control. The control data for the PCA16 is downloaded to the board controller FPGA via the general data path on the backplane where configuration data for the ALTROs is downloaded.

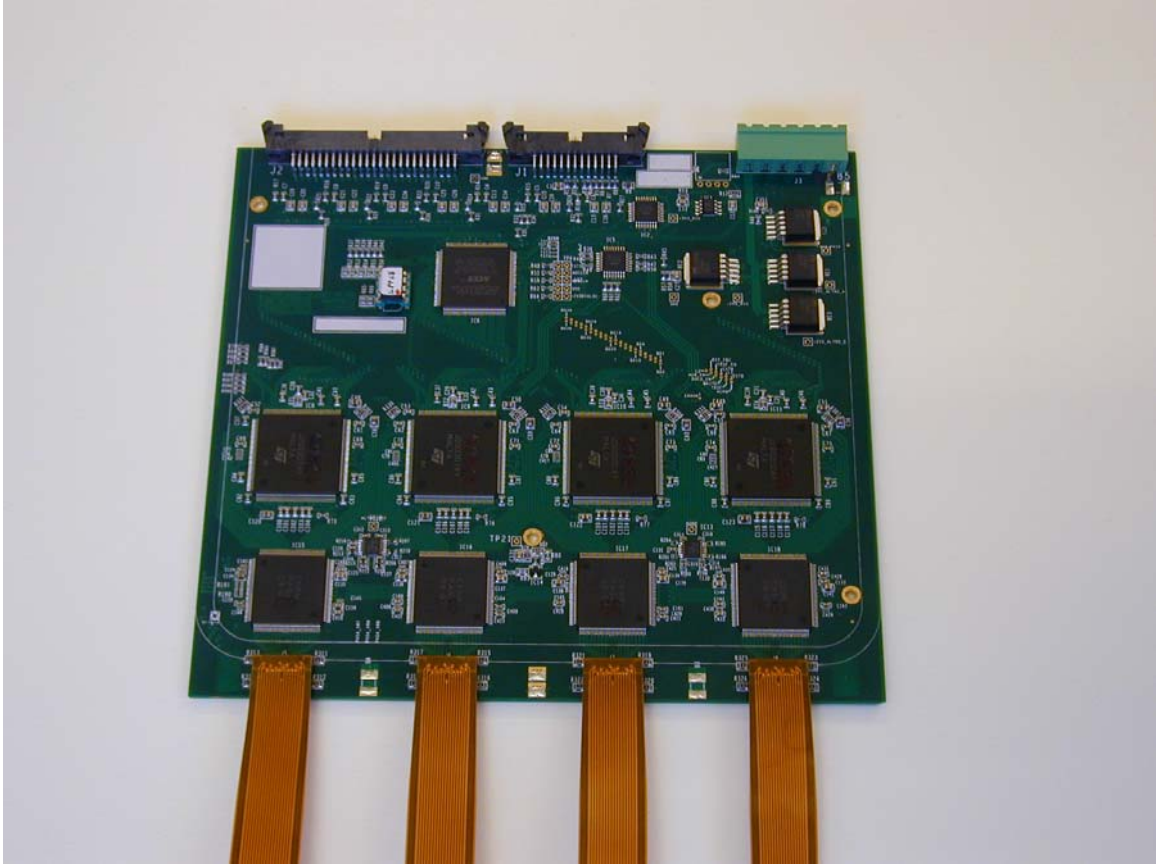


Fig 3. The FEC seen from the top side. The below side carries four PCA16 and four ALTROs just like the top side. The Kapton cables are attached on the input connector on the board. The back edge is occupied by the backplane contacts and the LV connector.

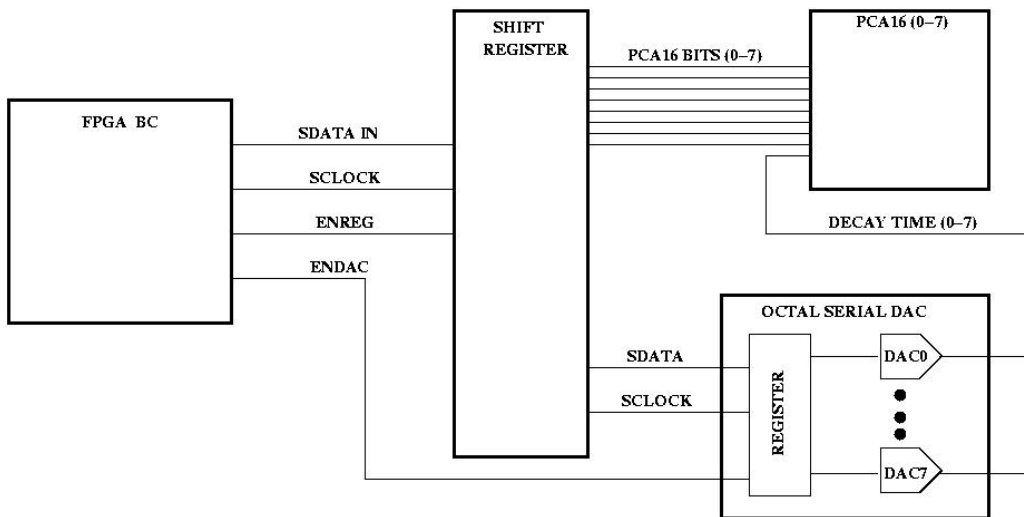


Fig 4. The circuitry involved in the PCA16 control

Since the PCA16 control introduces an electrical connection between the digital activity in the board controller/readout part and the amplifier chips, special attention was paid to

proper filtering on these traces. The FPGA had no available space for the PCA16 control and some of the functionality (related to slow controls) of the ALICE design had to be removed. Lack of available output pins (and the desire to minimize the number of FPGA to PCA16 traces made it necessary to send the control data serially from the FPGA. The data includes 8 bits (made parallel in a shift register) for the digital settings and another 12 bits for the DAC, whose analog voltage controls the decay constant of the preamp output. The programmability has been implemented on the board such that all eight PCA16 chips have the same setting.

2.5 Noise optimization

The ALICE-FEC had experienced some coherent clock noise pointing at a source of these problems related to every 4th sample. This was identified as being due to the digital activity in the ALTRO which starts when processing of the four first 10 bit ADC-samples is finished and 40 bit words are composed from the 10 bit words of four consecutive samples. This coherent digital noise remains throughout the 1000 samples and appears at one quarter of the sampling frequency in the frequency domain.

It turned out that while this problem was suppressed below the noise threshold on the ALICE-FEC it remained still a limiting factor on the EUDET-FEC. The main reason that the EUDET-FEC was more sensitive to this was the shorter shaping time on the preamp-shaper. It was evident that at the longer shaping times (120ns) we did not observe this noise but it was substantial on some channels for the shortest shaping time (30ns). The clear visibility of this noise made it possible to address the problem systematically. The solution was found in modifying the grounding around the ALTRO, thus tying the analog (the ADC) and digital ALTRO grounds together close to each chip. This reduced the clock noise substantially and an overall RMS noise level for all 128 channels on a FEC at 370 electrons was obtained. The board tests and the performance on the chamber are discussed in chapter 5.

3. Cables and Connectors

The FEC has 4 male, multi connectors from Japan aviation. The same kind of connector will be placed (fig.5), on the pad panel of the TPC endcap, connected to the sensor pads via blind vias. Each connector has 40 pins with 0.5mm pitch. Out of these, 32 pins will be used for pad signals while 8 will be reserved for ground connections.

Four Kapton flat cables of length 30cm connect the pads with the FEC. The cable has the mating counterparts of the connectors with a right angle version in the pad end and a straight connector in the FEC end.

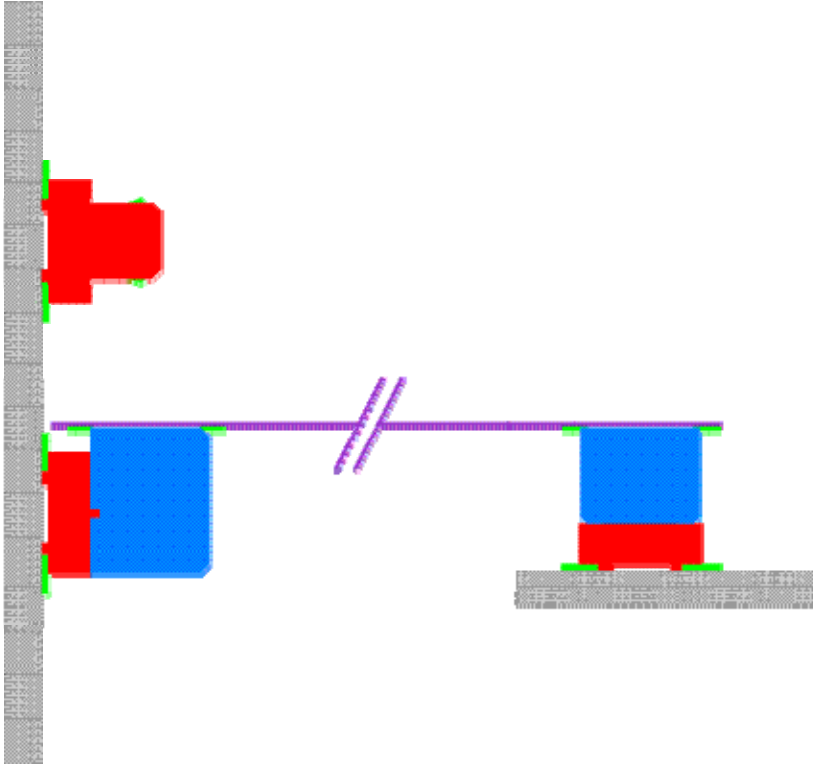


Fig 5. Schematic illustration of the connectors on the FEC, the backplane and the Kapton cable

A cable is shown in fig 6. It has traces on both sides and the largest capacitance between traces is from one side to the other although the traces on one side have been placed opposite to the trace gaps on the other. Initial crosstalk tests showed 1-2% crosstalk between close traces on opposite sides and an increase of the pitch to 0.5mm and with a trace width of 0.2mm has been implemented in a new version.



Fig 6. A photograph of a 30cm long Kapton cable.

4. The LV system and cooling.

The Low voltage system (LV) to supply the front end electronics is based on LV modules from Delta Elektronika. These modules have been used in the prototyping reported in the coming chapters.

TABLE 1. *The required specifications of the LV system.*

Chip	Chip voltage	Current/FEC	Max Power /FEC	module	Volt span	Current /module	modules for 32 FEC
PCA16	1.5V	1A	1.5W	S6-40	0-6V	40A	1
ALTRO	2.5V	3A@40MHz	7.5W	150SX5	3.3-6V	26A	3
RCU+FECctrl	3.3V	1A	3.3W	150SX5	3.3-6V	26A	1

The switched LV-supplies are available in different voltage/current configurations. The modules are placed and powered in a “Euro cassette”. Table I summarizes the requirements on the LV system for a system with 32 FEC read out via one RCU.

The LV crates will be placed ca 5 meters away from the electronics.

Cooling of the front end electronics has not yet been finalized. The total power of a FEC is ca 9W i.e 900W for a 100 FEC system operated at the highest frequency. Only forced airflow can be used for the cooling since the spacing between FECs had to be kept at a minimum (14mm pitch) in order to house sufficient number of FECs inside the envelope of the magnet.



Fig 7. *A LV module of the type 150SX5 from Delta Elektronika*

Heating up of the TPC is a major concern. Thus a heat barrier must protect the TPC from heat produced by the electronics. If fans are used, these have to be placed outside the magnetic field and the airflow has to be distributed by plastic tubing. Possibly, compressed air, injected by thin tubes so that blowing is outwards away from the TPC may be the best alternative. The final solution of this issue awaits a full scale test of a 32 FEC system.

5. Test of a 128 channel system on a small TPC

From the EUDET first deliverable, a 128 channel system (1 FEC) was tested on a small TPC with GEM readout made available to us by the EUDET partner Universities Aachen and Bonn. Fig 8 is a photograph of the cosmic setup with the TPC cylinder, trigger scintillators above and below the TPC and the one FEC readout system.



Fig 8. Photograph of the cosmic setup with a TPC and one FEC+RCU for readout.

5.1 Noise performance

Figure 9 summarizes the excellent noise performance of the front end electronics, connected to the pads on the chamber. The electronics is powered by the LV-modules (see chapter 4) envisaged for the full system. The figure contains two parameters for the full FEC of 128channels (x-axis). The red stars (values read on the left Y-axis) are the pedestal values on the ADC scale for each channel and the blue squares (read off to the right) represent the RMS value of the pedestal i.e. the total noise measured in ADC channels. It should be noted that the data is obtained with the highest gain (27mV/fC) and shortest shaping time (30ns) i.e. the most sensitive setting. The average RMS noise (ca. 1.6 ADC channels) translates to the customary noise unit i.e. equivalent number of electrons:

$$N_{\text{electrons}} = 1.6(\text{ch}) \cdot 1\text{mV/ch} / 27(\text{mV/fC}) \cdot 1.6 \cdot 10^{-4} \text{fC} = 370$$

This excellent value includes random noise, coherent clock noise and actually also any long term variation of the order of few seconds.

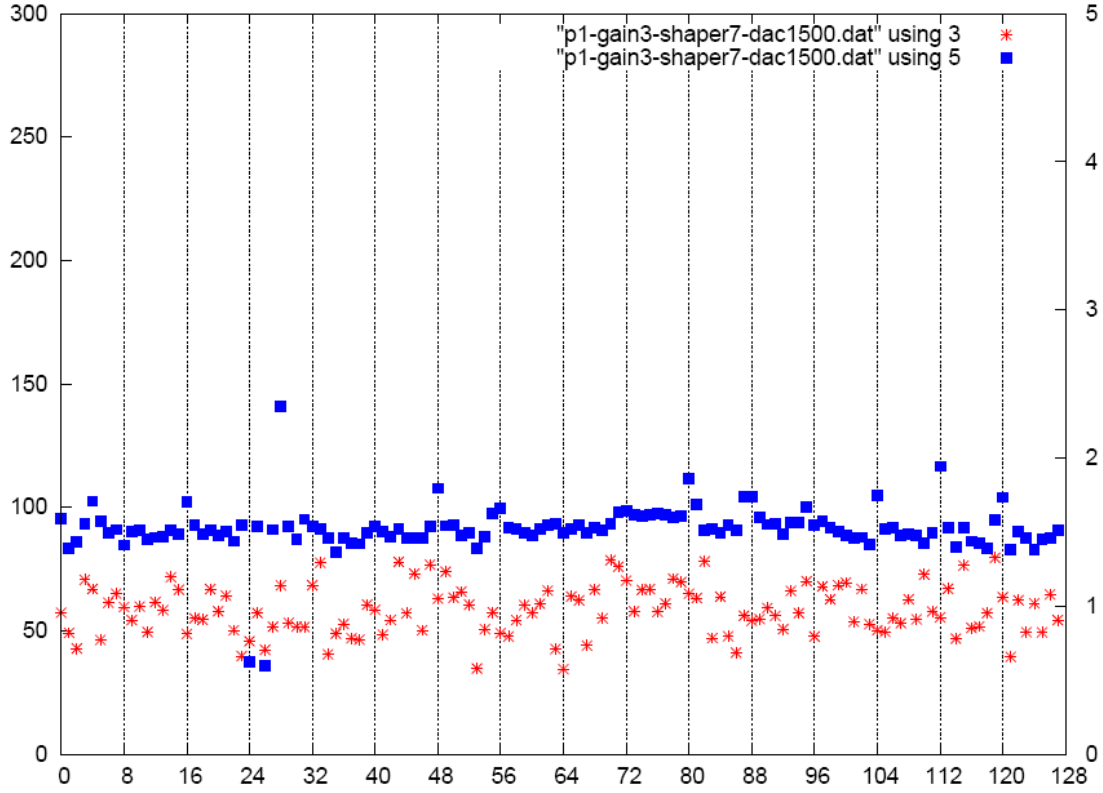


Fig 9. The pedestal average and noise rms for each of the 128 channels (x-axis) on one FEC connected to the chamber. The vertical axes are in ADC channels. At the actual gain, one ADC channel (1mV) corresponds to $1/27\text{fC}$. The two channels with low RMS have lost the pad connection.

5.2 Cosmic data from the TPC.

The TPC with two plastic scintillators, above and below for triggering on muons from the cosmic radiation is seen in figure 8.

The TPC had a maximum drift length of 25cm and a diameter of 20cm. The chamber gas was Ar- CO_2 where the quencher admixture was 20%. A 3 GEM multiplier system provided the avalanche gain. The pad plane consisted of two sets of pads, one being $1*6\text{mm}^2$ and the other $1*4\text{mm}^2$

With the limited number of channels used, only two pad rows of 64 pads each could be read out. Thus a projected area of $64*8\text{mm}^2$ placed such that most of the TPC volume defined by the trigger scintillators, could be read out.

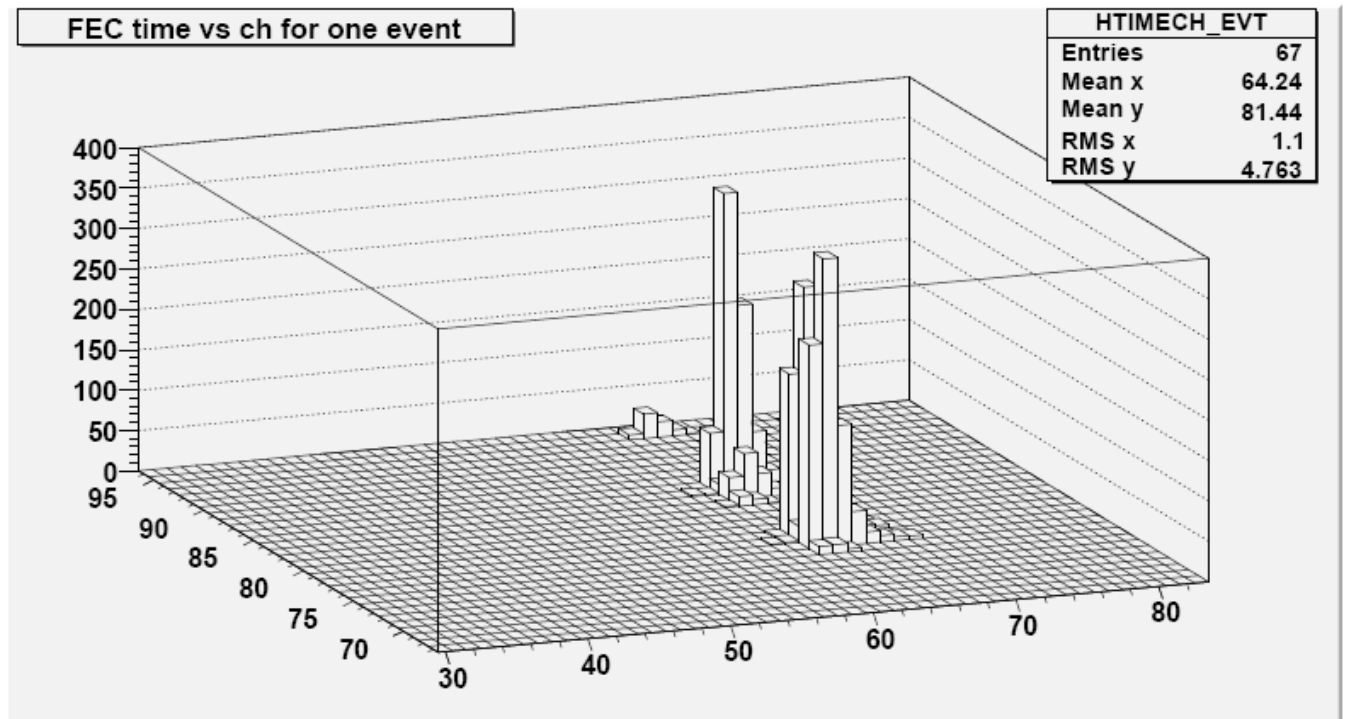
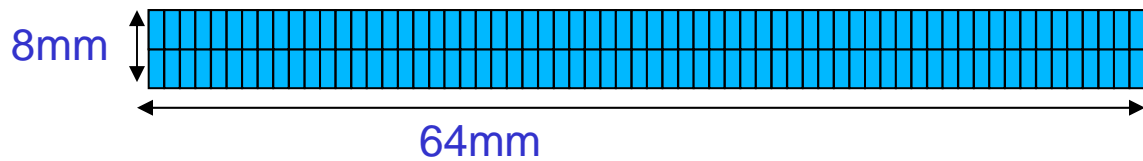


Fig 10. Recorded track data from a particle passing the TPC. The time dimension is displayed in a limited interval between time slices 30 and 82 with 100ns per slice. The pad numbering (65-95) is slightly arbitrary and can not easily be translated to position of the hit pad. The two large clusters reaching high ADC values (~ 350) correspond the hit in each of the two instrumented pad rows (top of figure).

A final result from the cosmic tests is the sampled dE/dx distribution obtained by adding the charge recorded in each nonzero pad sample. The resulting histogram in Fig. 11 has been fitted with a Landau distribution. The distribution appears shifted away from zero, indicating 100% efficiency.

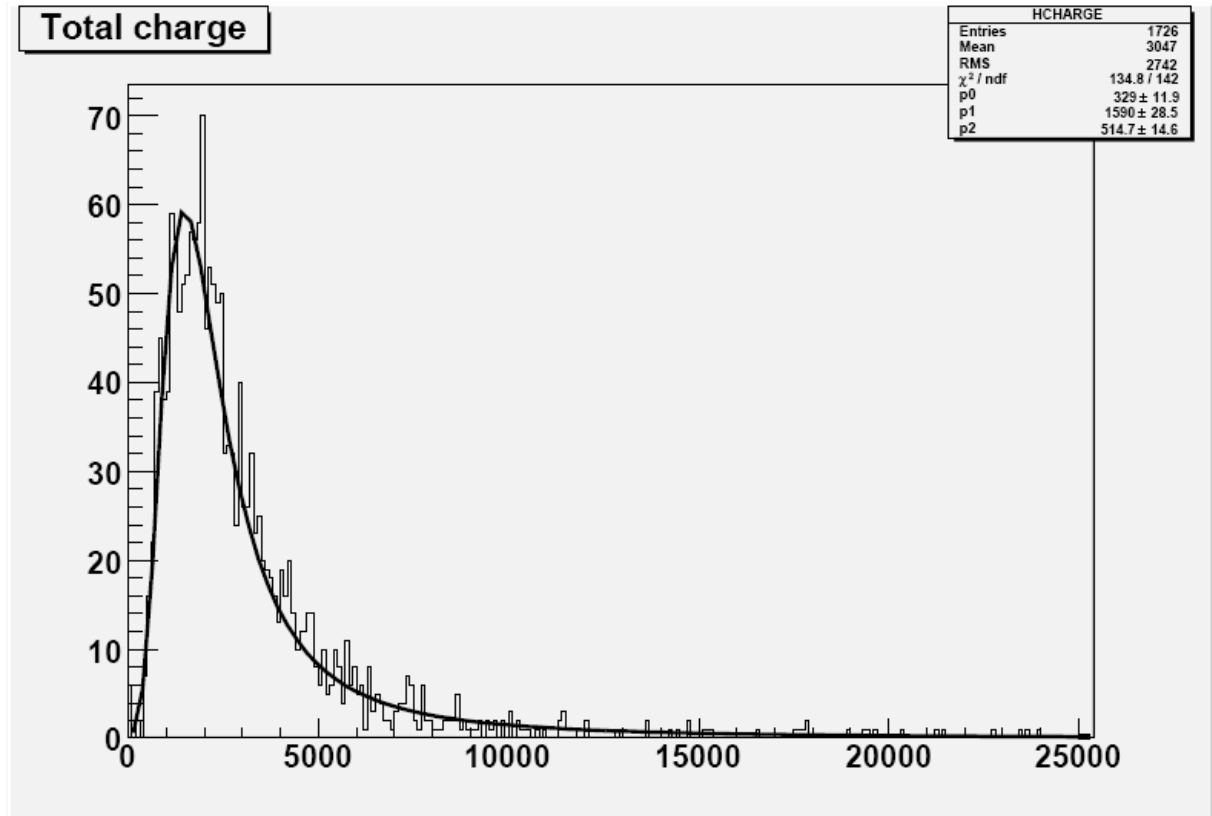


Fig 11. The dE/dx distribution deduced from the charge sum of the samples resulting from a passing cosmic minimum ionizing particle.

The cosmic test was not a major objective of this work whose main motivation is to report on the performance and performance and readiness of the Front End Electronics. However, without reading out real signals from a chamber, important verification would be missing. With this said, we stress that not much work has been put into tests on the chamber. Among other, far from optimized chamber conditions, we point out that the chamber gas was probably not sufficiently free from oxygen to allow higher quality tests within the time allocated to these tests.

6. Mechanical assembly

The back plane of the prototype TPC is illustrated in fig 12. It has 7 openings where different pad panels and avalanche chambers can be placed. Openings not used are closed by blind panels. An opening and its pad panel is shaped like a sector in a tentative final TPC design. The radial position of the pad panel on the final TPC, determines the radius of curvature of the circular edges of the openings. Pads will be oriented with their long edge along the radial dimension (vertical in the figure) for the best momentum resolution for high momentum tracks which are almost straight and radial. The typical particle direction in the beam tests will be along the radial dimension

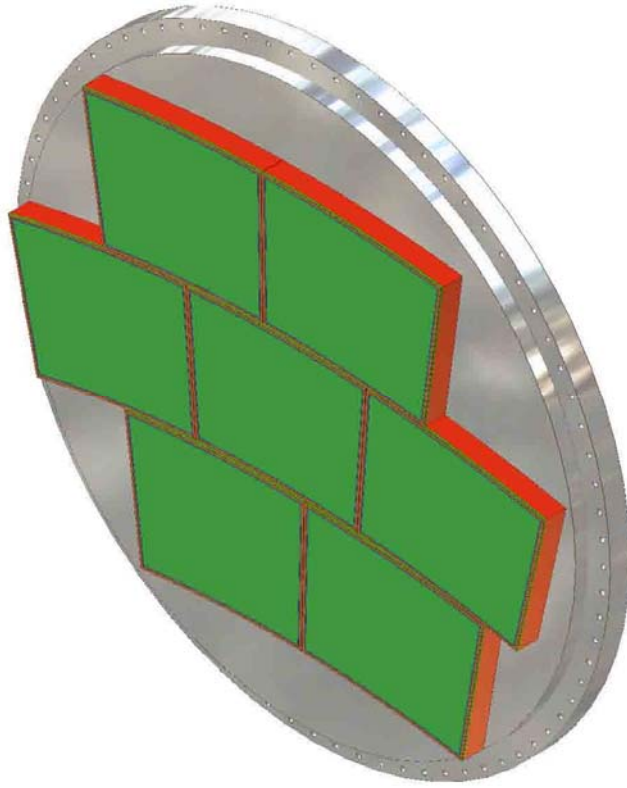


Fig 12. The back flange of the large prototype TPC (as viewed from inside the TPC) with seven pad panels . The flange diameter is ca 80cm.

The mechanical assembly structure for the electronics shall allow instrumenting the three radial levels with sufficient number of channels. A full pad panel contains ca 4200 pads of the size 6mm^2 size.

Fig 13, shows the mechanical structure for mounting the FECs on the TPC. The basic carrying structure consists of two rings which have the same outer diameter as the TPC and rests on the same supporting rail system as the TPC. The front ring is attached to the TPC such that it follows the sliding and rotating movement of the TPC without loading it with any weight. The small freedom of movement thus needed between the TPC and its electronics is insured by the flexibility of the Kapton cables.

The FECs have to be stacked as closely as possible in order to obtain the desired channel density. The backplane for FEC readout and the mechanical crate structure to hold the FECs are made with 14mm pitch between adjacent FECs. The width of a FEC is slightly larger than the height of the pad panel. Thus it is also important to be able to place the FECs as closely as possible also in the vertical direction (orientation as in fig 12) in order to minimize the length of the Kapton cables. Another and more severe constraint is that no parts of the electronic readout system may extend outside the outer edge of the rings (i.e. the TPC outer diameter) as they would then hinder the rotation of the TPC + electronics. The ultimate size constraint is that the electronics will have to fit inside the inner

radius of the magnet since, when in use, the TPC+electronics setup will be pushed fully inside the Magnet. The magnet opening leaves just ca 2cm space around the TPC.

Fig 13 illustrates the mechanical structure with the two rings and the three crate platforms with plastic guide rails in which the FECs slide. The top and bottom platforms

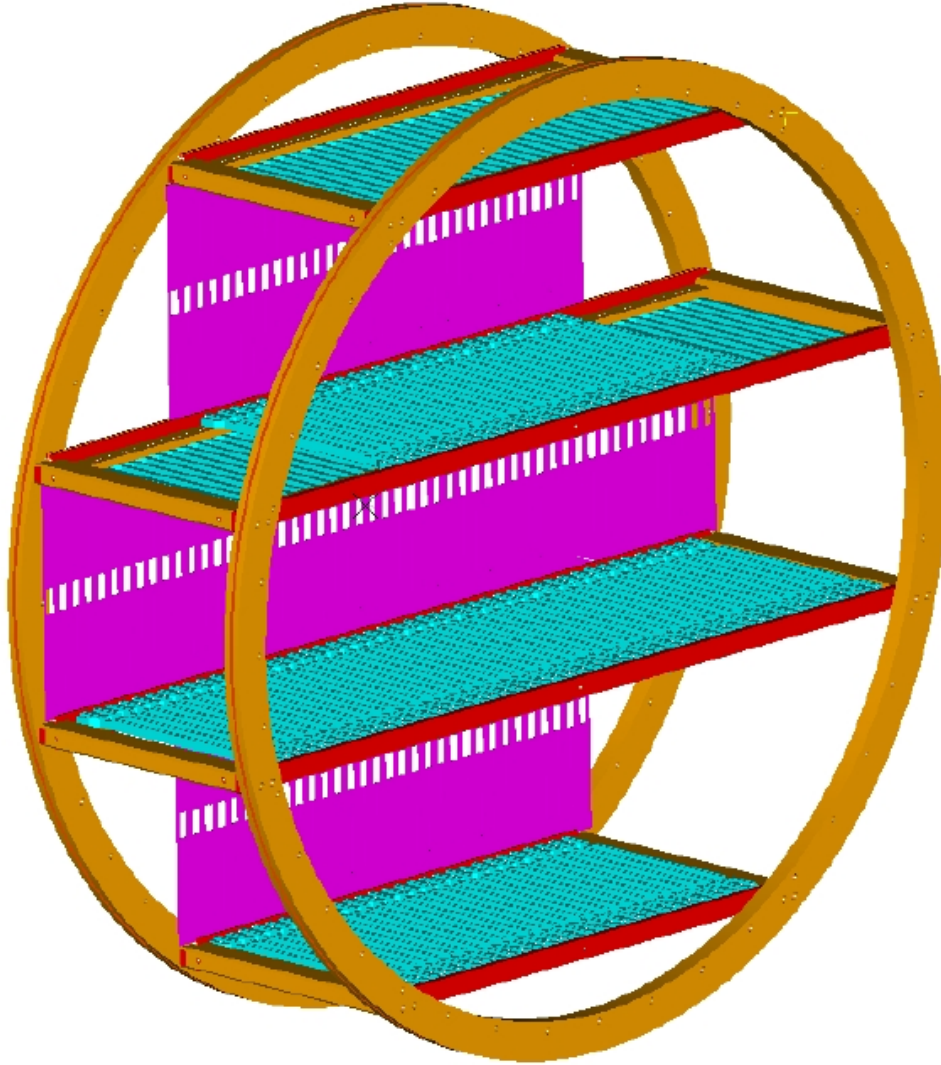


Fig 13. *The mechanical support structure for the front end electronics showing the two rings and the crate platforms made up by the plastic guide rails. The view is from the back i.e. the TPC itself is behind this structure.*

have at most 32 FEC positions and the middle one has at most 52 positions.

The ring facing the TPC will be fully closed with shield plates made of circuit board material (one sided copper clad). These plates will serve the purpose of providing an electromagnetic shield between the FECs and the sensitive analog input cables and pads.

In addition they will make a heat barrier preventing heat from the FECs to warm up the TPC and its gas. Fig 14 shows in detail the front shield plates with slits, slided into a groove in the support bar (attached to the front ring), which also serves as support of the front end of the plastic guides for the FECs.

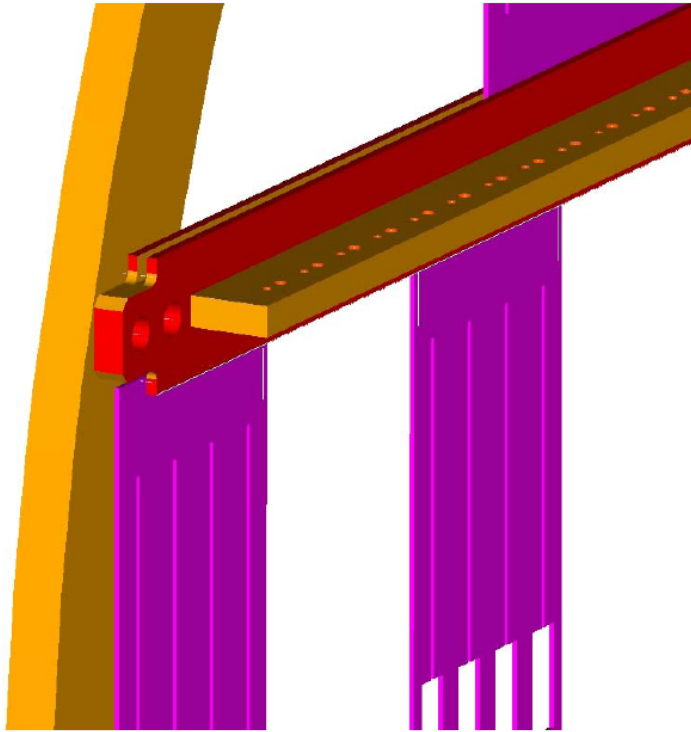


Fig 14. *Detail of shield plates mounted on the front ring.*

The Kapton cables will reach the FEC via narrow slits in these plates which in this way also will provide a mechanical fixture of the Kapton cables. This may prove particularly important in the assembly phase which is expected to be difficult due to the limited space. The ring structure can be divided (fig 15.) in two parts where the front ring and its shield plates is one.

The plan is that each shield plate, which covers four FECs, is mounted individually and its cables are inserted into the slits before the next shield plate is put in place. This should give access to the connector side of the pad panels as well as holding the Kapton cables in place until all of them are mounted on the chamber. Finally, the FECs are inserted in sequence, one after the other, and the cables are attached before the next FEC is put in place. Replacement of a broken FEC will have to be done by removing all FECs on the cable side of the bad FEC. Having the cables fixed in the slits will prevent them from coming loose in the pad panel end when working with the FECs..

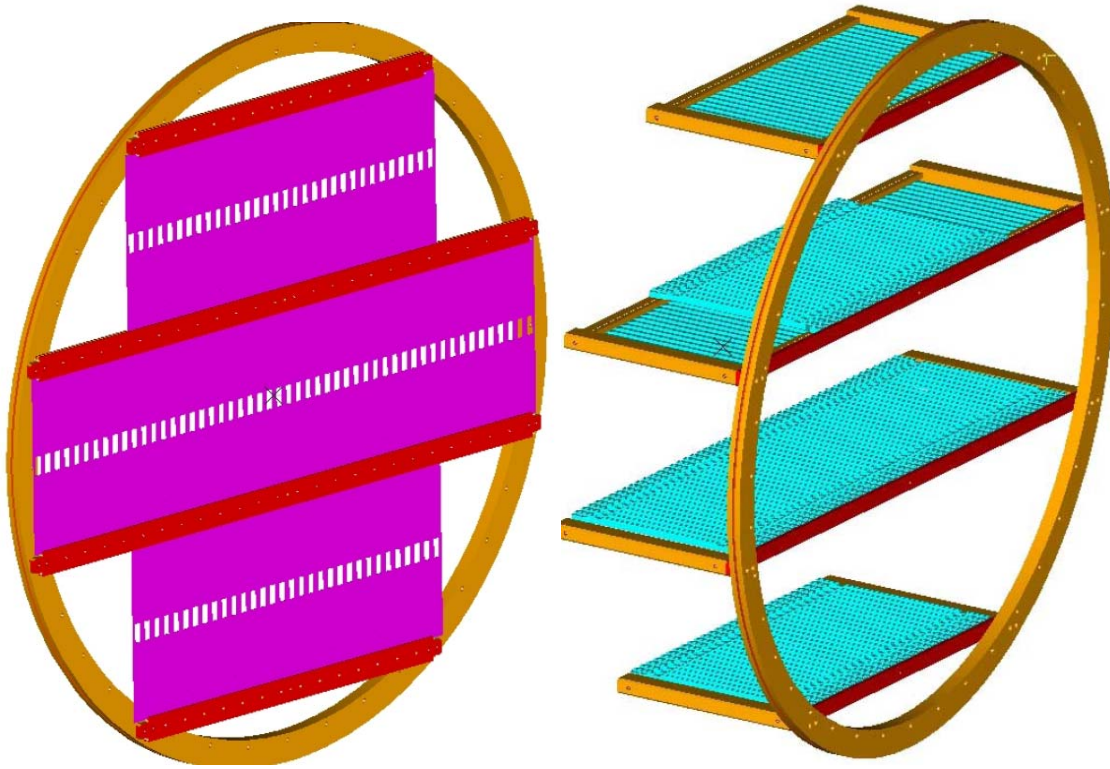


Fig 15. *The front and back rings detached for cable assembly.*

The back ring has mounting holes for flexible use for attachment of RCUs, the cool air distribution and strain relief for LV cables.

7. Conclusion

The present availability, as of October 6, is 7 fully functional front end cards (896 channels). In principle, this meets the minimum required EUEDET delivery. Our plan has however been to build a 2048 channel system (16 FECs plus spares) for the EUEDET purpose.

Additional funding from the LC-TPC collaborating partners have been made available and there is funding and chips available to build about 80 additional FEC (10240 ch). The final number of extra FECs that can be built depends on the chip yields.

For the readout of the total of ca 96 FEC an order on 4 complete readout chains (RCU-fiber optic link and receiver in the PC) has been placed. In addition to the two existing chains it will then be possible to simultaneously operate 3×27 FECs at the DESY beamline with one spare RCU system available on site, keeping one system running at Lund University for further development and having one available for preparations at collaborators home institutes.

As of December 1st, the plan is to have the 96 FEC system operating for the February 1st beam tests at DESY

Acknowledgements

This work is supported by the Commission of the European Communities under the 6th Framework Program "Structuring the European Research Area", contract number RII3-026126, by the Belgian "Fonds de la Recherche Scientifique - FNRS" and by the Swedish Research Council (VR).

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