EUDET-Memo-2008-52

JRA1 Milestone: Final Readout Ready

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Abstract

For the EUDET pixel telescope [1] a flexible and performant data acquisition system (DAQ) has been developed. A first version of the data acquisition has been used together with the demonstrator telescope [5] in the years 2007 and 2008 and has been described in detail in [2] and [3]. This memo summarizes the final readout, which has been adapted to the TC/Mimosa-26 sensor. In addition the overall performance of the system has been improved.

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1 Introduction

Within EUDET JRA1 a test beam telescope based on pixel sensor was developed [1], [5]. It will provide a high precision of better than 3 μm, even at the lower energies available at the DESY test beam facility. In addition to high precision, a high readout speed and easy handling is of importance.

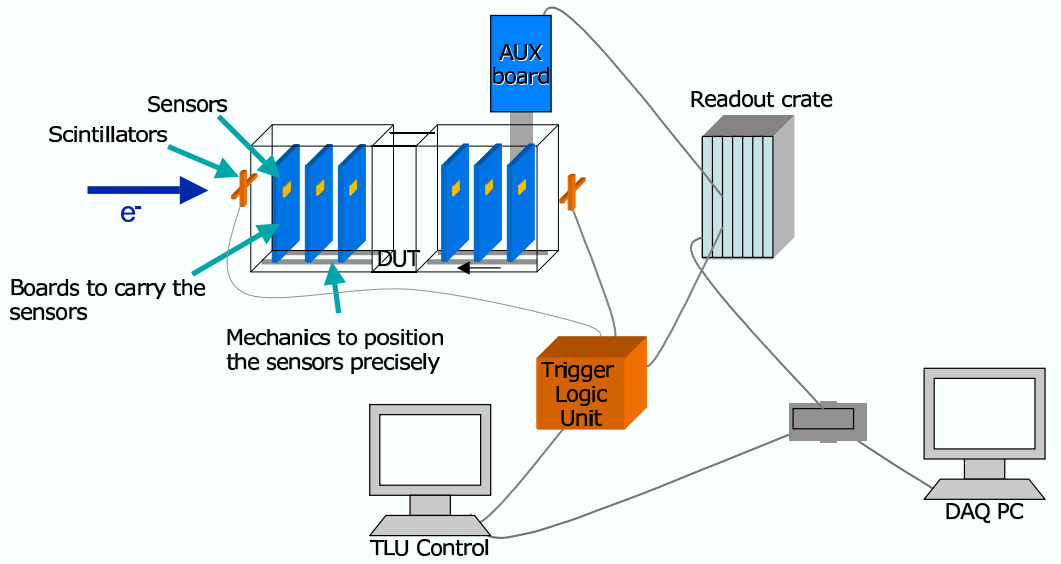

Figure 1: Overview of the ingredients needed for an analogue telescope.

In Figure 1 all "ingredients" of the pixel telescope are shown. All components are available since beginning of 2007 and this "demonstrator" version of the telescope is running in user mode since September 2007 [5]. During phase 2 the analog telescope will be completed by a fully digital sensor chip [10] and the DAQ hardware adapted to the final sensor chip.
For the readout of the demonstrator telescope as well as for the digital sensor, a dedicated data acquisition system has been developed.

2 The DAQ system

The data acquisition system, as shown in Figure 2 for the EUDET beam telescope is a combination of dedicated hardware and software with the following sketched data flow: The pixel sensors are read out by custom made data reduction boards (EUDET Data Reduction Board - EUDRB), sent via VME64x block transfer to a VME CPU (PowerPC MVME6100) and from there via Gigabit Ethernet to the central DAQ computer. This DAQ computer combines the telescope events with the information from the custom made Trigger Logic Unit (TLU), which is controlled by its own PC. The whole system is controlled by the EUDET Data Acquisition software (EUDAQ). The system

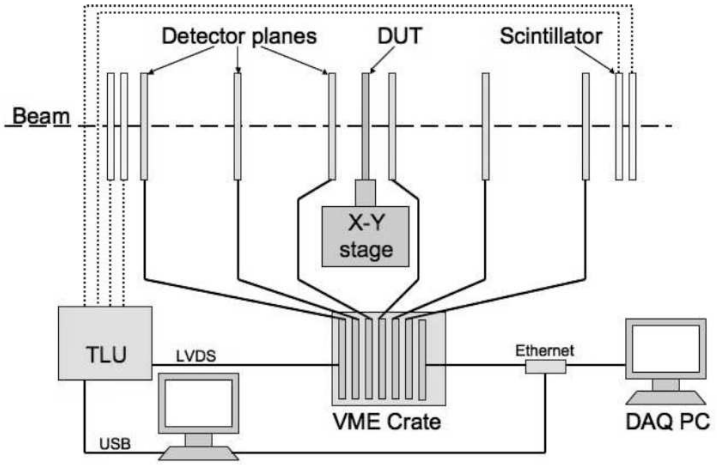

Figure 2: The DAQ system of the EUDET pixel telescope.

allows flexible integration of multiple Devices under Test (DUTs). Offline analysis of the data is performed within the ILC software framework on the GRID using a dedicated EUTelescope package. The details to the different components are given below.

2.1 The Data Reduction Board - EUDRB

The EUDET Data Reduction board (EUDRB) was developed to read out Monolithic Active Pixel Sensors (MAPS). The board generates detector timing signals in LVDS logic levels and provides analog to digital conversion of the four analog single-ended/differential input with 12bits resolution at a sampling frequency currently set at 10 MHz.
The EUDRB also features an output port (with TTL signalling levels) to configure detectors with JTAG programmable features. The motherboard has 4 banks of 256k×48bit SRAM memories providing storage for up to three full frames for a 1Mpixel sensor like the MIMOSA-5. On this collected data the EUDRB performs Correlated Double Sampling (CDS), pedestal subtraction and threshold comparison to reduce the data size for the events selected by the experimental trigger. However, the EUDRB also provides the full frame information when the RAW operating mode is selected. The EUDRB features a 256k×32bit FIFO memory to provide temporary storage for data selected by a trigger and waiting to be readout. Both a VME and a USB2.0 interface are implemented; the EUDRB may be used for reading out the MAPS both in standalone mode on a bench-top and in a standard VME-based data acquisition system. The trigger input port on the front panel of the EUDRB was designed to interface it to the EUDET Trigger Logic Unit (TLU) (see section 2.2) and a trigger bus is also foreseen to distribute/receive trigger information over the free lines of the VME J2 connectors by means of a private bus on flat cable.
Two LEMO connectors on the front panel of the EUDRB can be used to synchronize

the data collection operations over a pool of boards. The operation of the EUDRB is controlled by an ALTERA Cyclone II Field Programmable Gate Array (FPGA) device in which a NIOS-II microcontroller is also implemented to do initialization, housekeeping and diagnostic. An 8 MByte serial configuration device EPCS64 is used to store both the FPGA configuration information and the microcontroller code. At power up the FPGA loads its configuration from the EPCS64 and begins operation; the first task executed by the NIOS-II is to copy its ROM-resident code from the EPCS64 to its 1MByte program/data RAM and then jump to executing the code in RAM.

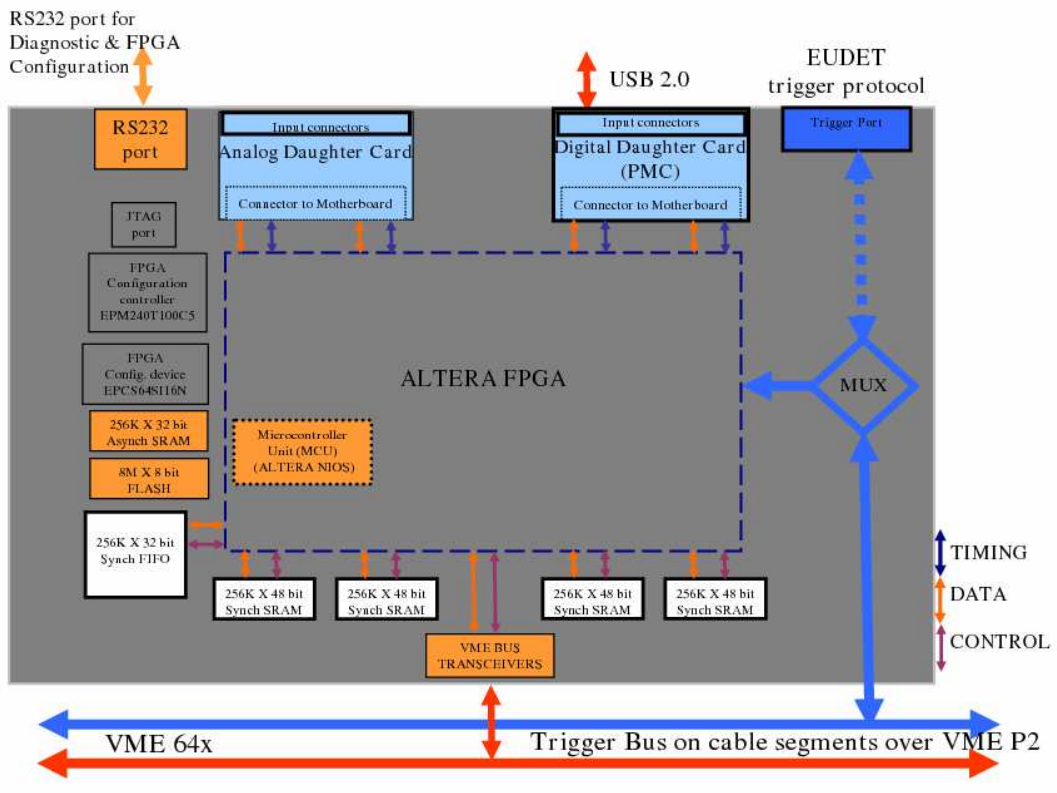

Figure 3: Diagram of the EUDRB functionality.

2.1.1 EUDRB Motherboard

The larger green block represents the motherboard (EUDRB_MoBo) and the resources supported by it:

- the ALTERA EP2C70F896C8 FPGA (dashed blue outline) with the NIOS-II block in evidence. Details of the sequencers and logic blocks implemented in the FPGA are given in a later section
- the four banks of 256k x 48bit SRAM whose function is to hold the pixel voltage samples recorded during the last three scans of the four MAPS submatrices. The

SRAM also hold values of pedestal (6bits) and threshold (6bits) which are specific to each pixel

- the 256k x 32bit FIFO used as temporary storage for the data requested with a trigger pending the readout through the VME or USB2.0 port utilities:
- the 256k * 32bit SRAM used as program/data memory by the NIOS-II
- the 1M * 8bit Flash (non volatile) memory which could be used by the NIOS to store permanent data (i.e. default pedestal/threshold values)
- the configuration device EPCS64
- the configuration controller based on an ALTERA EPM240T100 which provides an alternate method for bootstrapping the FPGA
- the EUDET TLU ports: the front panel port to connect the EUDRB directly to the EUDET Trigger Logic Unit. An EUDRB connected to the TLU will act as the TLU-Interface for all the EUDRBs in a VME crate. The TLUInterface fans out the trigger informations to other EUDRBs via a private bus on a cable segment installed on the free pins of the VME P2 connectors
- the RS-232 port which allows a simple and direct connection of the NIOS-II to an host PC for lower level diagnostics and debugging

2.1.2 EUDRB Digital Daughter Card

The EUDRB_DCD is a board with standard PCI Mezzanine Card (PMC) format and PMC compatible connectors toward the EUDRB_MOBO. On the front side of the EUDRB_DCD four connectors are available. The EUDRB_DCD features a Cypress CY7C68013A-56PVXC, which, like in the MAPS readout boards designed by the SUCIMA collaborations, provides a relatively simple way of interfacing the EUDRB?s FPGA to an USB2.0 bus, via the front panel connector J4. The CY7C68013A-56PVXC holds its bootstrapping data into a 24LC128 128kbit serial EEPROM. The EUDRB_DCD then provides an I/O port with single ended 3.3V TTL signal levels (connector J1, RJ45) to control the configuration of sensors with features programmable via a JTAG interface, like the IPHC MIMO⋆2. The J2 connector provides detector timing signals (Scan Clock and Scan Reset) in LVDS format. For driving the MIMOTel sensor used in the demonstrator telescope an interface board has been developed at INFN Ferrara (MIMOTel level adapter) which translates the voltage levels of the JTAG signals from the EUDRB_DCD J1 connector, rearranges connector pin definitions and drives the output signals through two RJ45 connectors to the MIMOTel. Fig. 2.4 shows the electric diagram of the ?MIMOTel level adapter. The J3 connector receives detector timing signals (Scan Clock and Scan Reset) in LVDS format from an external source (like a sensor?s proximity board or another EUDRB). This feature has not been used in the demonstration telescope because a different port, on the analog daughter card) for such synchronization signals has been used.

2.1.3 EUDRB Analog Daughter Card

The EUDRB_DCA is a board with standard PCI Mezzanine Card (PMC) format and a pair of IEEE-1386 PMC connectors toward the EUDRB_MOBO; the signals assignment on this connectors is not compatible with the PMC standard. On the front side of the EUDRB_DCA two RJ45 connectors are available, whose pin definition is reported in Fig. 2.3; there are also 6 LEMO connectors, as shown in Fig. 2.5. The EUDRB_DCA J1 is the port for the differential analog input signals, which are usually buffered and driven differentially by the sensors proximity board along a four-pair shielded twisted cable, to reduce noise pick-up. The EUDRB_DCA J2 is an output port which could provide four channel of polarization voltages or four static signals to the MIMOSA-5 detector to configure its operating mode. The main task of the EUDRB_DCA is to digitize the four input signals. The design of the ADC stage and its ADC driver is based on the designs developed by the IPHC in Strasbourg and the University of Cracow and exploited by the SUCIMA collaboration. The four A/D converters used on the board are of the type AD9226 by Analog Devices. The AD9226 resolution is 12 bit and its sampling frequency can reach 65MHz. The AD9226's differential inputs (with a 2V dynamic range) are driven by a buffer stage based on the differential amplifier AD8138. The buffer stages also take care of translating the single ended inputs from the LEMO connectors into the differential format; this option can be enabled by modifying solder-jumpers on the analog daughter card.
The two following modes of operation have been implemented in the EUDRB firmware so far:

- **Transparent mode:** All pixel signals are transferred without further data processing. This mode is important for debugging and for the characterisation of the telescope sensors itself.
- **Zero suppressed mode (ZS):** The correlated double sampling (CDS) is performed online and only the signals and addresses of pixels above a certain user-defined threshold are transferred. This mode is intended for datataking at high rates keeping the output files reasonably small.

The output of the EUDRBs is collected by a MVME6100 single board computer which is located in the same VME64x crate. Finally, the data are send to the main DAQ PC using gigabit ethernet. This computer can also collect the information from the device under test (DUT).
For the final sensor, the EUDRBs get an improved firmware, implementing interrupt driven readout and enhanced VME speed using the 2eSST protocol.

2.2 Trigger Logic Unit

Figure 4: Front Panel of the TLU

A simple easy to use trigger system is desirable for a user telescope, given that at beam-tests rapid installation of the device under test is often needed. Triggering on beam particles has traditionally been done using modules housed in NIM crates. However, NIM crates are bulky and heavy. Moreover they are either expensive if purchased new or often in poor repair if drawn from a "loan pool". In addition it is not straightforward to expand a NIM trigger system to provide trigger time-stamping, allowing self-triggered or triggerless operation of the device under test (DUT). Modern field programmable logic allows construction of a low-cost, compact and flexible trigger unit which addresses these issues.
An important design aim was to place few *restrictions* on the user of the TLU, whilst being as flexible as possible. The trigger unit should be as simple as possible, since ILC detectors will not be triggered. It should also be low cost, to allow widespread distribution. Ideally, each group developing detectors should be able to have at least one TLU.

2.2.1 Operating Modes

The TLU is able provide "classic" beam-test trigger system. Incoming beam triggers are combined in a user selectable combination and passed to one or more DUT. The TLU also keeps a record of the arrival time of each trigger. Hence it can operate as time-to-digital converter for triggerless or self-triggered DUT. Both modes are active simultaneously, allowing triggered and triggerless/self-triggered DUT to be mixed in the same beam-test.

2.2.2 Interfaces

Four 50Ω terminated coaxial connectors accept NIM,TTL or photo-multiplier level pulses and receive a trigger for each particle passing through the test-beam. These four inputs are combined to form a beam-trigger. The arrival of a beam-trigger will cause a trigger

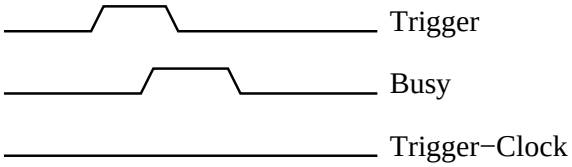

Figure 5: Simple Handshake Mode

to be output to active DUTs, unless one or more have indicated that they are busy. Interface to the DUT is via RJ45 connectors each carrying four LVDS signals. The signals from the TLU to the DUT are *trigger* and *reset*, the signals from the DUT to the TLU are *busy* and *DUT-clock*. There are six DUT connectors.
The FPGA is configured via the USB interface. Memory-mapped communication is used for setup and control. Then, block transfer is used to transfer time-stamps from the TLU to the host computer.
A photograph of the TLU front panel showing the various interfaces is shown in figure 4. In 2008, the TLU has been upgraded to allow software switching between LVDS, TTL and also NIM levels.

2.2.3 Handshake with Device Under Test

There are three handshake modes available for communication between the TLU and the DUT. The modes can be mixed, with different DUT using different handshake modes. The handshake modes are:

- **No Handshake.** The TLU asserts the *trigger* line for a fixed length of time. The *busy* line from the DUT is not monitored. In this mode the TLU acts like a simple discriminator and coincidence/veto unit.

- **Trigger/Busy Handshake.** The TLU asserts the *trigger* line connected to every DUT in the system. The TLU waits for each DUT to assert its *busy* line. When a DUT does this, the TLU de-asserts the corresponding *trigger* line and waits for the DUT to de-assert its *busy* line. The TLU does not issue any further triggers until all the DUT drop their *busy* lines. This mode is illustrated in figure 5.

- **Trigger/Busy/Trigger-Data Handshake.** This mode is similar to the Trigger/Busy handshake, but trigger information is transferred from the TLU to the DUT. When the TLU de-asserts the *trigger* line in response to the DUT asserting its *busy* line, the DUT toggles its em DUT-clock line and the TLU will clock out trigger information on the *trigger* line. Normally the trigger information is the bottom sixteen bits of the trigger counter. After the DUT is ready for new triggers and has clocked out the trigger information, it de-asserts the *busy* line.This mode is illustrated in figure 6.

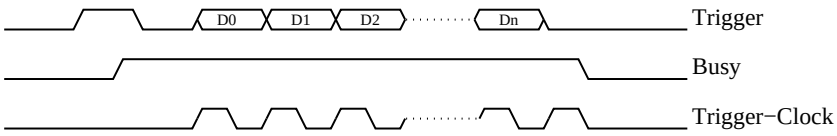

Figure 6: Trigger-Data Handshake Mode

2.3 DAQ Sofware - EUDAQ

The custom DAQ software framework named EUDAQ has been implemented in C++ [2], [3]. Several producer tasks, that run on different computers, communicate with a global run control using sockets. These producer tasks connect to the hardware of the beam telescope, to the TLU and eventually to the DUT. Data from all producers is sent to the central data collector and can be monitored by several processes. An online monitor based on the ROOT framework showing online data quality monitoring histograms as well as a process to collect log messages are available. EUDAQ has been written platform independent and runs on MacOS, Linux and Windows.
In 2008, the EUDAQ has undergone some major improvements, described in [4] to increase the VME readout speed and to adapt the framework to the architecture of the final telescope chip. With the improved driver, the system achieves data rates of a few hundred Hertz with 6 Mimotel sensor boards.

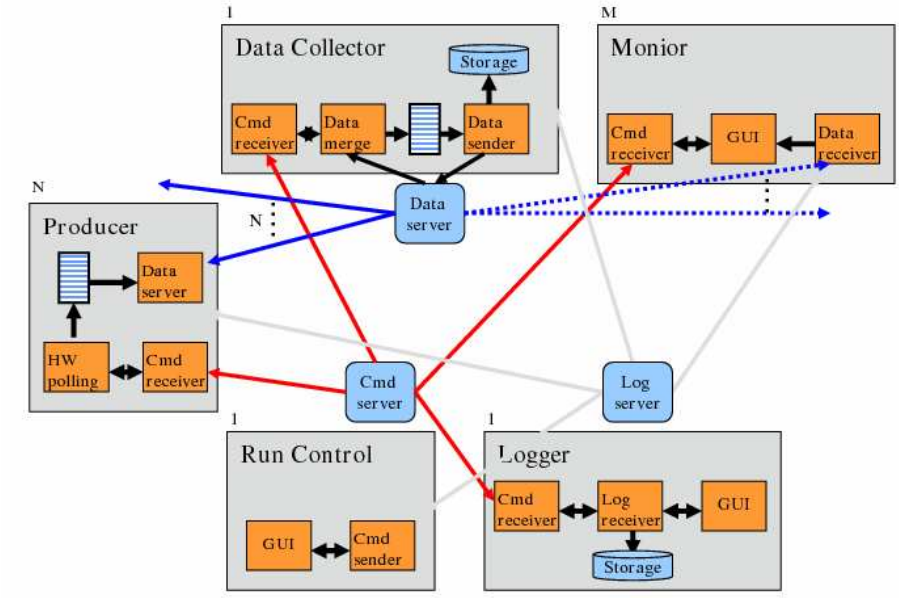

Figure 7: Overview on the organisation of the DAQ software EUDAQ.

2.4 User DAQ Integration

Different scenarios for the integration of the DUT in the DAQ system of the EUDET pixel telescope are possible:

- **Integration at hardware level:** In this case the user has to provide a hardware interface able to read out the telescope sensors and the DUT. This approach is supported by the EUDRB boards, but is only feasible for some dedicated DUTs.
- **Integration at DAQ software level:** The user provides own DAQ hardware to read out the DUT, but the data are be treated by a common DAQ software. In case EUDAQ is used as the common DAQ system, a producer to read out the DUT needs to be implemented.
- **Integration at trigger level:** This default scenario was chosen by most users so far, because it is easy to implement and relatively safe. Different hardware and software are used for the telescope and the DUT. The synchronisation is done using the trigger, busy and reset logic provided by the TLU. To protect against slippage of event numbers between the telescope and the DUT, the event number provided by the TLU can be read by the DUT.
- **Integration at data level:** Both, the DUT and the telescope use their own dedicated DAQ hardware and software. The data streams are combined offline by inter process communication. In this scenario the synchronisation and the configuration during the start-up might be difficult.

3 Summary

For the EUDET JRA1 pixel telescope, a complete, stable and performant data acquisition system has been developed. The DAQ has been used successfully in test beam campaigns 2007 and 2008. Recently, the system has been adapted for the final sensor chip and the overall performance has been enhanced to take into account the increased data throughput. With the current sensors, the system can run at a few hundred Hertz. The final system will be used to deploy the TC/Mimosa-26 in 2009.
After an initial commissioning phase in 2009 the system will then soon be again available to users with a readout speed of about 1 kHz.

Acknowledgement

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