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JRA-1 Beam Telescope
Towards the Final Pixel Sensor

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Abstract

The final sensor equipping the EUDET telescope is expected to cope with typically 1 million particles per second. Its architecture relies on a parallelised processing of the pixels, complemented with a fast zero suppression logic. The developement of the sensor is organised accordingly along two lines, one focussed on a pixel array organised in columns with discriminated output read out in parallel, and one addressing the zero suppression logic complemented with output memories.

The final prototype of the column parallel architecture (IDC) was fabricated in 2007/08 and fully tested in 2008. The zero suppression micro-circuit (SDC-2), which was fabricated in 2007, was also characterised in 2008. Both chips meet all their requirements. This note summarises their features and performances, and provides an overview of the final sensor design.

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1 Introduction

The EUDET beam telescope will be equipped with fast and high resolution pixel sensors allowing to provide high density particle tracking adapted to intense particle beams. Because of the sizeable number of pixels composing the sensors (close to 1 million) and of their read-out frequency (about 10^4 frames/s), their output oughts to be limited to the pixels having collected a signal charge.
The signals delivered by the sensors are therefore discriminated before being filtered by an integrated zero-suppression logic. To allow for the fast read-out frequency, the pixels composing the sensitive area are grouped in columns read out in parallel and ended by a discriminator. The development of this chip, called Telescope Chip (TC, alias MIMOSA-26), relies on two tasks progressing in parallel. One of them addresses the upstream part of the signal conditionning chain, which includes the sensitive area and the discriminators ending the columns. The other concerns the downstream part of the chain, combining a zero-suppression logic with output memories. This report summarises the progress achieved during the last twelve months in the development of these two parts of the final architecture.
The development of the two components of the sensor requires designing and fabricating prototype chips, which allow evaluating various conceptual approaches as well as extracting and fine-tuning the most appropriate ones.
IDC, also called *MIMOSA-22*, is the final prototype of the upstream part of the sensor architecture, which includes charge sensing, average noise removal and analogue-to-digital conversion. It was designed and fabricated in two versions, one in Autumn-Winter 2007 and the other in Spring 2008. Both versions were tested extensively in 2008. Laboratory test results were provided in [1]. The complete test results, which include running the sensor on a particle beam, are summarised in section 3.
SDC-2, also called *SUZE-01*, is a prototype featuring the zero-suppression micro-circuit and output memories. Fabricated in Autumn 2007, its tests were completed in Spring 2008. Its main components and test results, which go beyond those exposed in [2], are summarised in section 4.

2 Main objectives and chracteristics of the IDC prototype

The IDC represents a crucial step towards the final sensor design. It is intended to allow defining the main characteristics of the analog and mixed components of the charge collection and read-out chain, as well as the integrated steering and testing elements of the final sensor (TC).
Its architecture is derived from the design of the SDC-1 prototype (alias MIMOSA-16 [3]), which features already the column parallel read-out architecture with binary outputs required to achieve the necessary read-out speed, but is 24 times smaller than IDC (and thus 216 times smaller than TC). MIMOSA-16 was fabricated in 2006 in the same CMOS technology (AMSC35B4O1 CMOS-Opto 0.35 μm [4]) as IDC. It was

successfuly tested in 2007 with charged particle beams at the CERN-SPS. Summarising, a detection efficiency of about 100 % was obtained for discriminator threshold values allowing a fake rate well below 10^{-4}, and the single point resolution was found to be better than 5 μm for a pitch of 25 μm.
Despite these excellent performances, SDC-1 being only made of 24 columns of only 128 pixels (i.e. 3072 pixels in total), it was necessary to reproduce these performances over a substantially larger surface and for a number of columns closer to the final one (e.g. in order to investigate potential dispersions between discriminators). Moreover, the pixel architecture implemented in SDC-1 was not optimised in terms of signal-to-noise ratio (SNR) and radiation tolerance, and the pixel pitch was too large for the single point resolution ambitionned. Finally, the sensor was not yet equipped with the necessary controlling and testing features provided by JTAG.
2 versions of IDC were designed and manufactured. The first version (MIMOSA-22) was mainly used for defining the overall pixel architecture, while the second version (MIMOSA-22bis) was used to make the design more robust, to fine tune its parametres and to improve its tolerance to ionising radiation. The goal was to validate at least one of the designs implemented in the IDC, and then to merge it with the SDC-2 design in the architecture of the final sensor TC (alias MIMOSA-26).
Both IDC prototypes have full dimensions of 12.0 x 3.7 mm^2, including a charge sensitive area of 10.6 x 2.5 mm^2.
The charge sensitive array contains 136 columns and 576 rows of pixels. The latter have a pitch of 18.4 μm. 128 columns are ended with a discriminator featuring a common adjustable threshold for analogue-to-digital conversion. The remaining 8 columns have direct analogue outputs for functionnality tests and pixel characterization purposes. The outputs of the 128 column level discriminators are multiplexed by a serializer block onto 16 binary output pads. The pixel array is designed to be read out on a column parallel basis and row by row (i.e. rolling shutter mode) with a frequency of 6.25 MHz. The corresponding integration time is less than 100 μs.
In order to realise the final sensor with optimised performances, different sensing diode dimensions, with and without radiation hard structures, have been implemented in the chip to find the best signal detection conditions, essentially governed by the SNR. Moreover, three types of pixel architectures were implemented: one with a reset diode with common source amplifier, one with a self-biased feedback diode with common source amplifier, and one with a feedback reset diode with common source amplifier. All of these pixels use the same clamping technique to achieve Correlated Double Sampling (CDS). More information on these different pixel architectures may be found in [1].
Different functionnal modes of the chip, controlled by the digital sequencer and the circuit bias can be set and removed via a JTAG [5] controller [6]. The values of the discriminator threshold voltages can be set both via the JTAG controller and dedicated input pads.

Figure 1 represents a photograph of the chip. Figure 2 shows the IDC functionnal view. It differs slightly from the final floor-plan, in which both the core and the pad ring were slightly modified in order to accommodate constraints emerging in the ultimate steps of

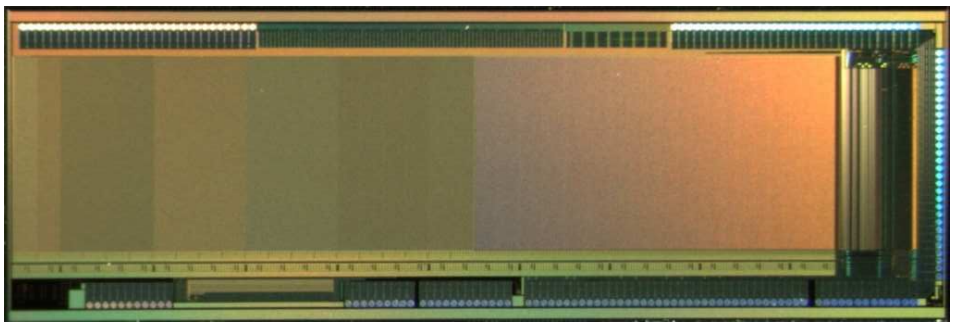


Figure 1: Photograph of the IDC sensor.

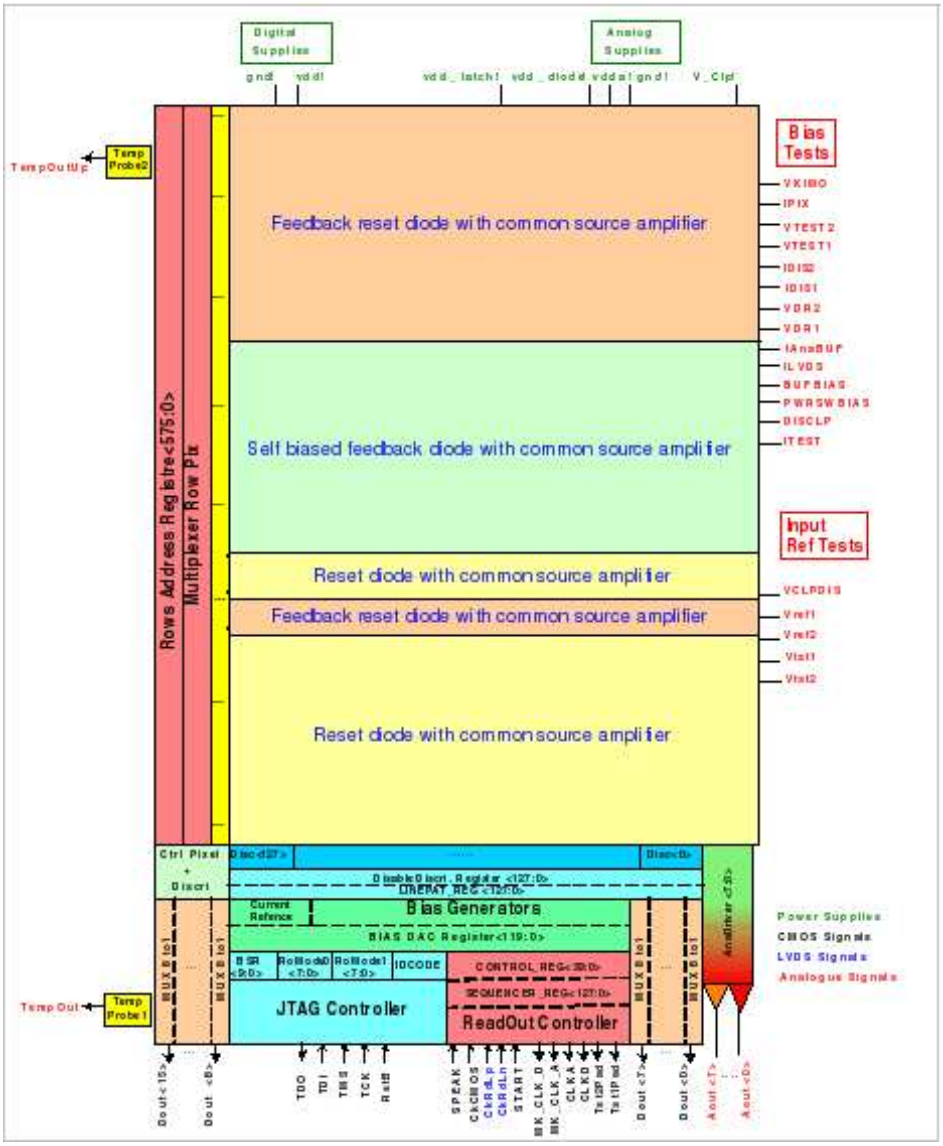


Figure 2: IDC functionnal view.

the design.

3 Test results

3.1 Introduction

The manufactured chips were validated in two steps. The first step consisted in characterising them in the laboratory, mainly to validate their operation mode, to assess their noise performances and to check the uniformity of their response over their whole sensitive area when illuminating them with a radioactive source.
Next, they were mounted on a beam telescope and exposed to charged particle beams at the CERN-SPS in ordre to evaluate in detail the advantages of each IDC sub-array for the detection of relativistic charged particles. The running conditions at the CERN-SPS are similar to those governing the EUDET beam telescope which the TC will equip.

3.2 Laboratory test results

3.2.1 Pixel performances

Several sensors were illuminated with an ^{55}Fe source in ordre to calibrate their Charge-to-Voltage Conversion factor (CVC) and to evaluate their signal collection and conversion performances, as well as the discriminator performances. These operations were performed for each individual sub-array.
The characteristics of the pixels were evaluated by analysing the signal delivered by the 8 columns with analogue output, i.e. which are not ended with a discriminator. The main test results are summarised below:

- Noise performances:
  - the temporal (i.e. pixel) noise was found to be between $\sim$ 10 and $\sim$ 14 e$^-$ENC[1], depending on the sub-array studied;
  - the Fixed Pattern Noise (FPN), reflecting the dispersion of the pixel characteristics belonging to the same column, was measured to be $\sim$ 5–6 e$^-$ENC;
  - the pixels featuring a design protecting the collection diode against the side-effects of intense ionising radiation doses exhibited a temporal noise value exceeding the noise of standard pixels by only $\sim$ 1 e$^-$ENC;
  - a modest temperature dependence of the total noise was observed. Its increase amounted to $\lesssim$ 10 % when ramping the chip operation temperature from +10°C to +35°C;
- The charge collection efficiency was observed to be $\sim$ 70–80 % for a 3x3 pixel cluster, depending on the sub-array. Its value was found to be $\sim$ 80–90 % for 5x5 pixel clusters;

[1] abbreviation of Equivalent Noise Charge.

- No significant variation in the detection response over the sensitive area was observed;
- These results were derived from 5 different chips, which exhibited the same measurement results within ± 5 %.

The noise performances of several of the sub-arrays composing MIMOSA-22 are provided in table 1.

Sub-array	S6		S7		S8		S9		S10	
	[mV]	[e$^-$]	[mV]	[e$^-$]	[mV]	[e$^-$]	[mV]	[e$^-$]	[mV]	[e$^-$]
TN	0.612	11.5	0.601	10.7	0.615	11.3	0.595	10.0	0.639	11.6
FPN	0.250	4.7	0.263	4.6	0.254	4.4	0.273	4.6	0.222	4.0
Sub-array	S12		S13		S15		S16		S17	
	[mV]	[e$^-$]	[mV]	[e$^-$]	[mV]	[e$^-$]	[mV]	[e$^-$]	[mV]	[e$^-$]
TN	0.636	11.2	0.692	13.4	0.682	12.8	0.536	12.4	0.627	11.4
FPN	0.225	4.0	0.269	5.2	0.277	5.2	0.218	5.1	0.217	4.7

Table 1: Noise performances of sub-array S6, S7, S8, S9, S10, S12, S13, S15, S16 and S17 observed in the laboratory. The measurements are provided for the temporal noise (TN) and the Fixed Pattern Noise (FPN), in mV and in ENC.

It is worth noticing that sub-array S6 and S10, which feature sensing diodes with improved ionising radiation tolerance, exhibit respectively total noise values of 12.4 and 12.3 e$^-$ENC only.

3.2.2 Discriminator performances

The performances of the 128 discriminators were investigated by measuring the sensor response as a function of the discriminator threshold, with and without illuminating the sensitive area with the ^{55}Fe source. Good uniformity of the discriminator response was observed, the dispersion featuring a standard deviation of $\sim$ 4 % only.

3.3 Beam test results

3 copies of MIMOSA-22 and of MIMOSA-22bis were mounted on a beam telescope [7] which was installed on a charged pion beam (average energy 120 GeV) at the CERN-SPS. The telescope is made of 2 arms, each composed of 2 pairs of silicon micro-strip modules. The strips of the modules composing a pair are orthogonal, allowing to reconstruct the position of the impact of traversing particles with about 2 μm accuracy. The response

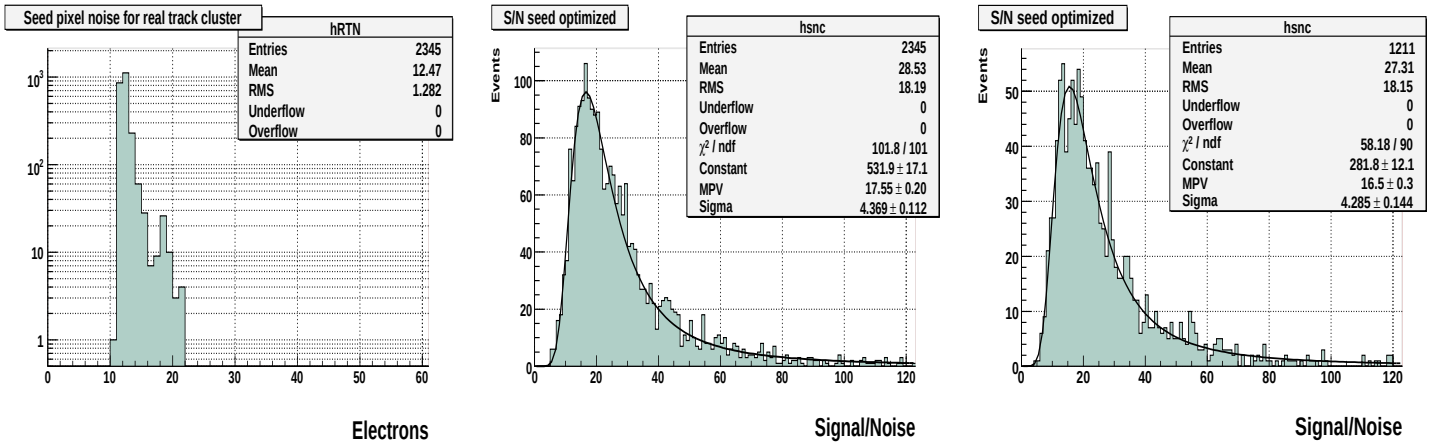


Figure 3: MIMOSA-22 analog output analysis: noise distribution of sub-array S6 (left) and SNR distributions of sub-arrays S6 (centre) and S10 (right) observed at the CERN-SPS.

of the sensors was recorded for more than one million of tracks reconstructed in the telescope during 4 weeks of running time in August, Septembre and Octobre 2008.

3.3.1 Analog output analysis

The detection performances of the pixels were investigated by analysing the signals delivered by the 8 columns of the sensors which are not ended by a discriminator, and thus provide analogue information. Of particular interest are the values of the electronic noise and of the SNR. The latter translates into an estimate of the detection efficiency. The observed noise and SNR distributions are illustrated in figure 3 for sub-array S6 and S10, which are both composed of pixels featuring a charge collection system with improved ionising radiation tolerance.

One observes that the noise of S6 is $\sim 12.5 \pm 0.3$ e^- ENC (i.e. identical to the value found in the laboratory, see table 1) and that the SNR amounts to ~ 17, a value well above the minimum ensuring a detection efficiency close to 100 %. The corresponding detection efficiencies are provided in table 2, which displays the values of the noise, the SNR and the detection efficiency for each of the best performing sub-arrays.

Excellent detection efficiencies were thus obtained with several different sub-arrays. The single point resolution was also determined, and found to be ~ 1.5 μm, as expected from measurements performed with previous MIMOSA chips featuring similar pixel characteristics [8]. Overall, these results validate the pixel architecture, in particular in terms of charge sensing diode, radiation tolerant design and amplification scheme.

Sub-array	S6	S7	S8	S9	S10	S12	S13
Det. eff.	99.93 ± 0.05 %	99.95 ± 0.04 %	100.00 +0/-0.30 %	100.00 +0/-0.14 %	99.87 ± 0.09 %	100.00 +0/-0.08 %	100.00 +0/-0.07 %
N (e^-)	12.5 ± 0.1	11.6 ± 0.1	12.3 ± 0.1	10.6 ± 0.1	13.6 ± 0.1	12.1 ± 0.1	14.0 ± 0.1
SNR	17.6 ± 0.2	18.5 ± 0.2	20.9 ± 1.1	19.5 ± 0.5	16.5 ± 0.3	18.2 ± 0.3	16.0 ± 0.3

Table 2: Detection efficiency, pixel noise (N, in ENC) and SNR measured at the CERN-SPS with each of the seven best performing sub-arrays. The values quoted for the SNR are most probable values for the seed pixel of the signal clusters.

3.3.2 Digital output analysis

The signal delivered by the 128 columns ended with a discriminator were mainly analysed to determine the detection efficiency, the fake hit rate and the single point resolution as a function of the discriminator thresholds. The main objective was to find a threshold value which was high enough to keep the fake rate at an affordable level while the detection efficiency was still close to 100 %.
To illustrate the performances observed, the values obtained for the three parametres above are displayed in figure 4 as a function of the discriminator threshold for 2 sub-arrays of MIMOSA-22 and 1 sub-array of MIMOSA-22bis.

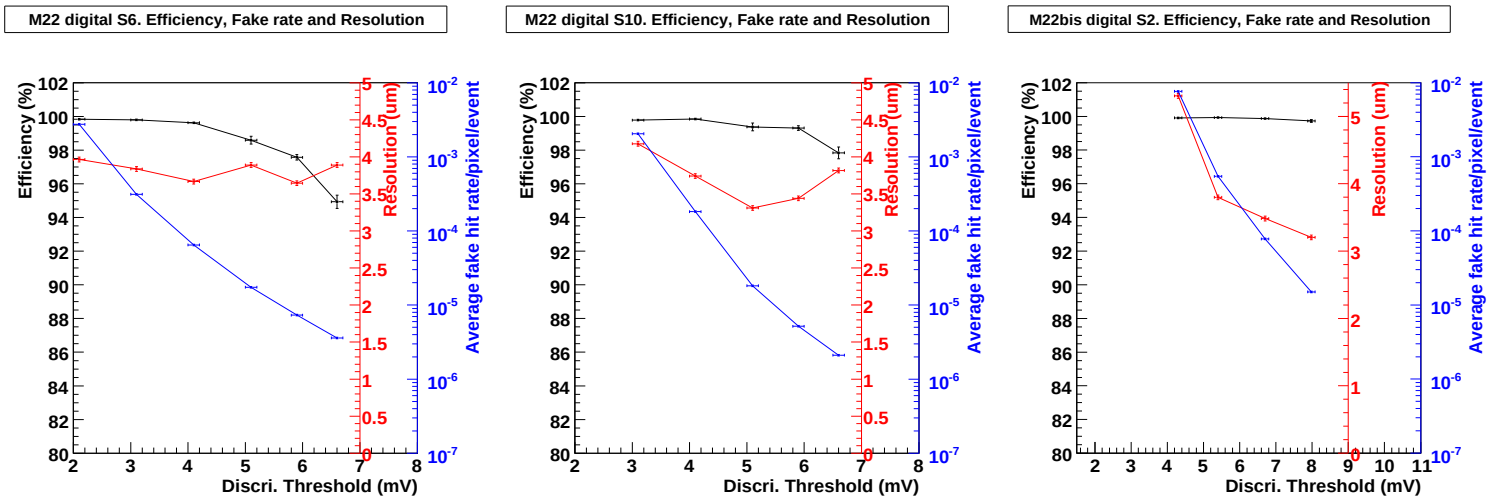


Figure 4: Variations of the detection efficiency (black points and curve), of the average fake hit rate (blue points and curve) and of the single point resolution (red points and curve) measured at the CERN-SPS as a function of the discriminator threshold. The measurements are shown for sub-array S6 (left) and S10 (centre) of MIMOSA-22 and for sub-array S2 (right) of MIMOSA-22bis.

A major outcome of the tests is that a detection efficieny of $\gtrsim$ 99.8 % is achievable for threshold values high enough to restrict the fake hit rate to the range 10^{-4}–10^{-5}. The single point resolution is $\gtrsim$ 3.5 μm, as expected when scaling the value observed with SDC-1 (MIMOSA-16) linearly with the pixel pitch. Finally, no performance non-uniformity was observed over the chip surface, and all chips tested featured very similar performances. Overall, these beam tests have shown that the sensor pixel and column architectures are viable at real scale. Several sub-arrays (i.e. pixel designs) exhibit very similar performances. The choice of the best suited pixel design had to account for the radiation tolerance assessments, which are exposed in the next section.

3.4 Improvement and assessment of the radiation tolerance

3.4.1 Introductory remarks

The radiation doses to which the EUDET beam telescope is expected to be exposed are - a priori - rather modest. For instance, running the telescope at DESY would expose it to a maximum annual integrated flux of $\lesssim 10^{11}$ e^- of a few GeV. This would translate into an annual ionising dose of $\lesssim$ 3 kRad and a corresponding fluence of $\lesssim 10^{10}$ n_{eq}/cm^2. These values remain harmless even after several years of operation.
The situation may be less relaxed on hadron machines, where a large fraction of the telescope users may want to operate it. This trend has already manifested itself with the telescope demonstrator, which has been operated at the CERN-SPS during numerous weeks. The integrated flux of particles (typically π^-) traversing the telescope in this case may amount to several 10^{12} charged particles per year, with a typical energy of $\sim$ 100 GeV. This may translate into several tens of kRad ionising dose per year and into a fluence of $\sim$ O(10^{12}) n_{eq}/cm^2. These values, which are likely to overestimate the annual doses at CERN, may however reflect realistically the doses accumulated after a couple years of operation. This observation makes it mandatory to take radiation tolerance into consideration when chosing the pixel design to be implemented in the final sensor (TC).

3.4.2 Laboratory tests

The sensitivity of the sensors to ionising doses was investigated by exposing three MIMOSA-22 sensors to a 10 keV X-Ray source. Each chip was irradiated with a different integrated dose, i.e. 50, 150 or 300 kRad. The main effect of ionising radiation on the chip performance is an increase of the thermal noise consecutive to a leakage current enhancement. The latter was measured on the different sub-arrays composing the sensor. Its values are shown in figure 5, which displays the noise measured within different sub-arrays and tests structures of MIMOSA-22 and -22bis before and after irradiation. Most test structures were declined in different design versions, which differ from each other by design details such as the dimensions of the transistors of the amplification and CDS circuitry.

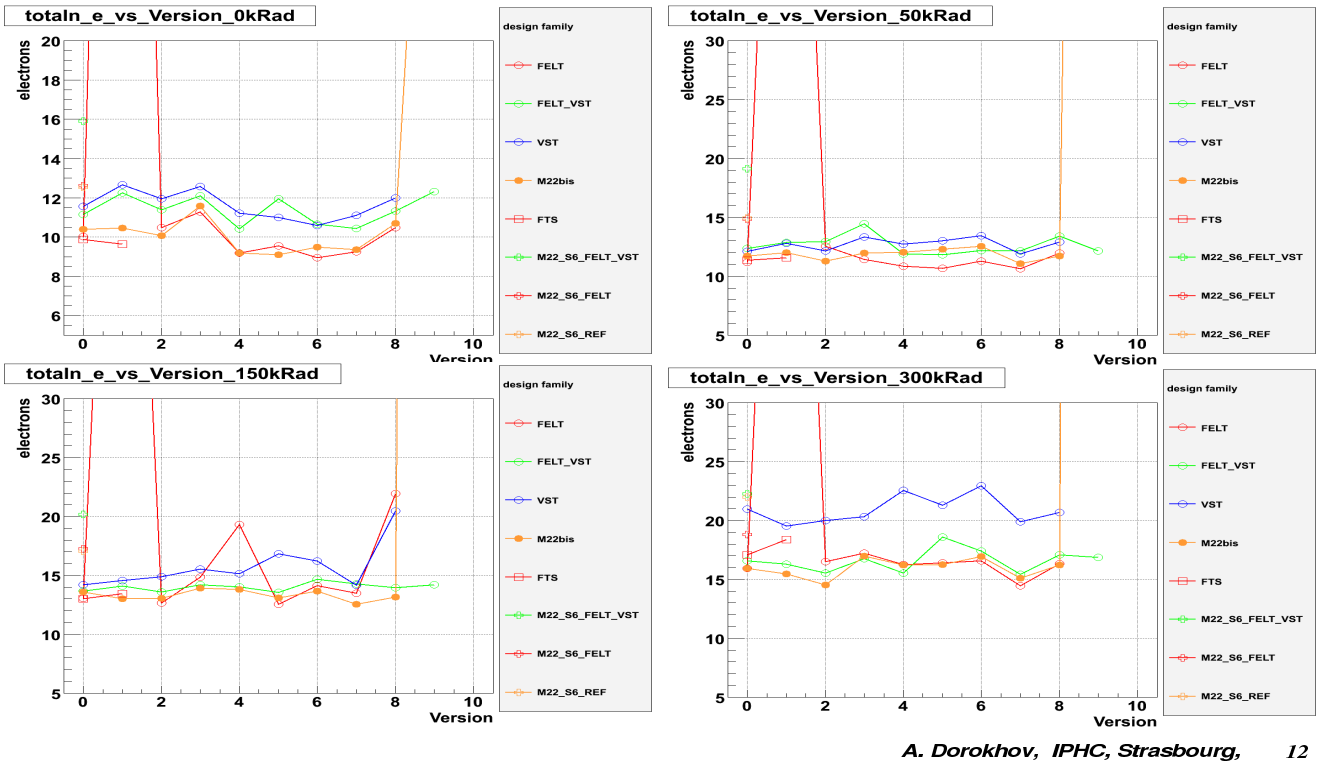


Figure 5: Measured noise of different sub-arrays and pixel variants of MIMOSA-22 and -22bis before (top left) and after irradiation. The integrated doses considered are 50 kRad (top right), 150 kRad (bottom left) and 300 kRad (bottom right). The horizontal axis expresses design variations of the pixel design (e.g. dimensions of the transistors achieving the CDS and the signal preamplification). The measurements were performed at a temperature of +20°C.

One observes that the noise increase, though substantial, is still affordable for integrated doses as high as 300 kRad, provided the adequate pixel architecture is chosen (e.g. the one called M22bis in the figure). However, the observed increase is larger than the one observed with previous sensors, which did not feature substantial in-pixel amplification [9]. There is thus presumably room for improvement in the radiation tolerance of the design.

3.4.3 Beam tests

The chip exposed to an integrated dose of 150 kRad was mounted on the silicon strip beam telescope mentioned earlier, and tested at the CERN-SPS with a $\sim$ 120 GeV π^- beam. Figure 6 displays the detection efficiency of various sub-arrays before and after irradiation as a function of the discriminator threshold values.

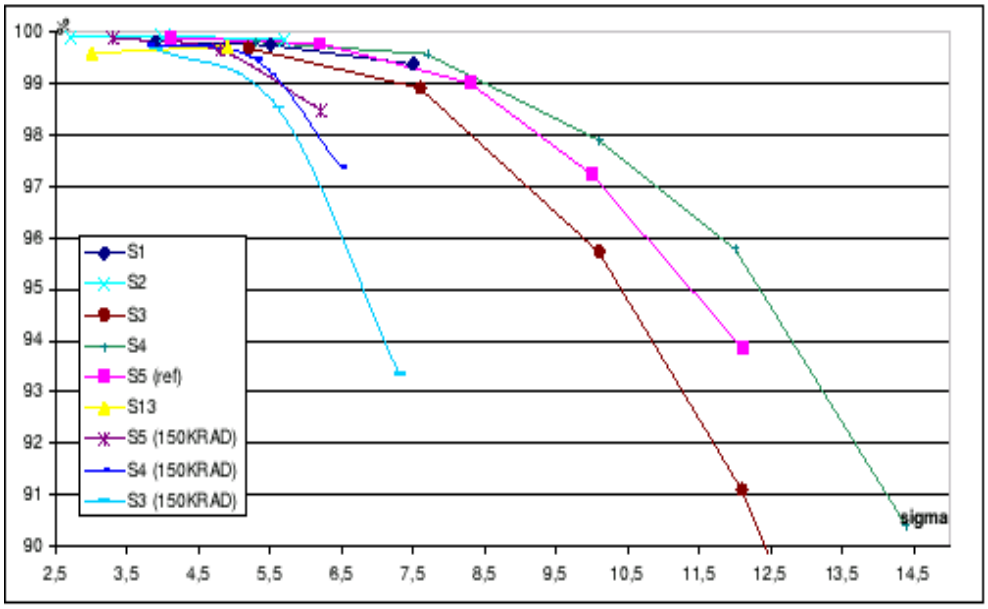


Figure 6: Detection efficiency of various MIMOSA-22 sub-arrays measured at the CERN-SPS, before and after 150 kRad irradiation, as a function of the discriminator threshold value. The latter was converted in units of SNR.

The drop in detection efficiency, consecutive to the noise increase mentioned in the previous section, is clearly visible. The detection efficiency remains however above 99.5 % for threshold values of up to 5–5.5 times the SNR. Figure 7 illustrates how the detection efficiency and the fake hit rate vary with the discriminator threshold values after 150 kRad integrated dose. The measurements are shown for a few sub-arrays of MIMOSA-22bis.

One observes that the fake hit rate stays below 10^{-4} for threshold values $\gtrsim$ 4.5 times the SNR. It is therefore possible to operate the sensors with high detection efficiency even after an exposure to ionising radiation equivalent to 150 kRad, provided the pixel

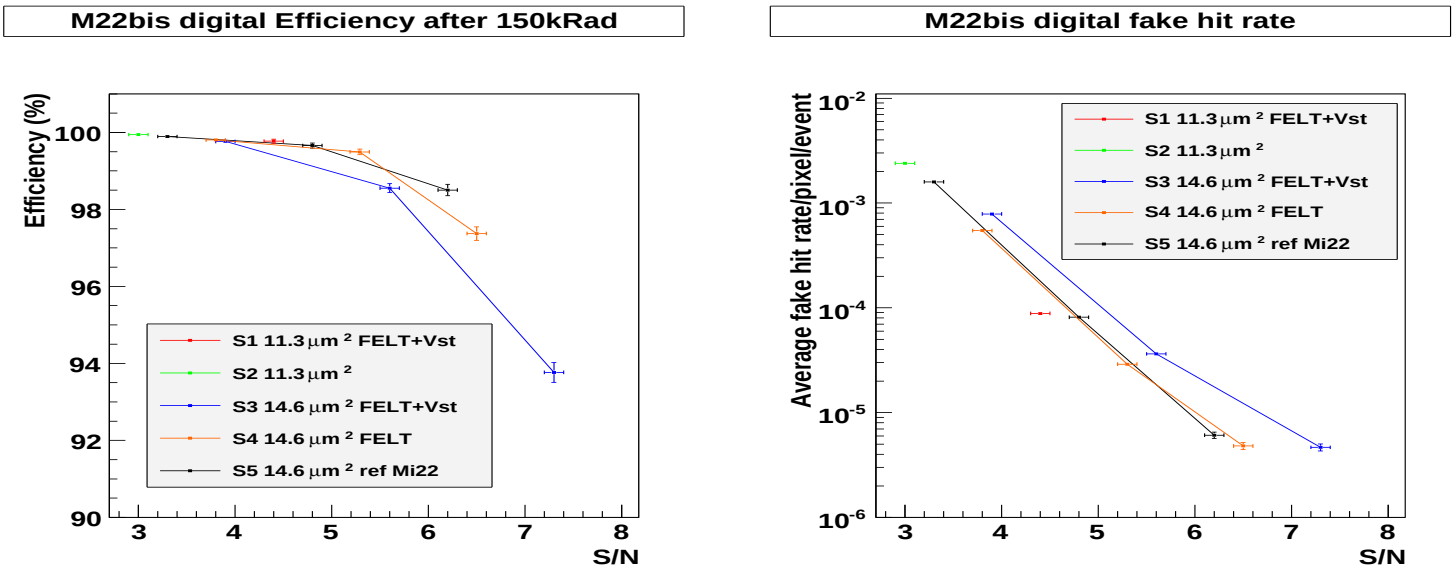
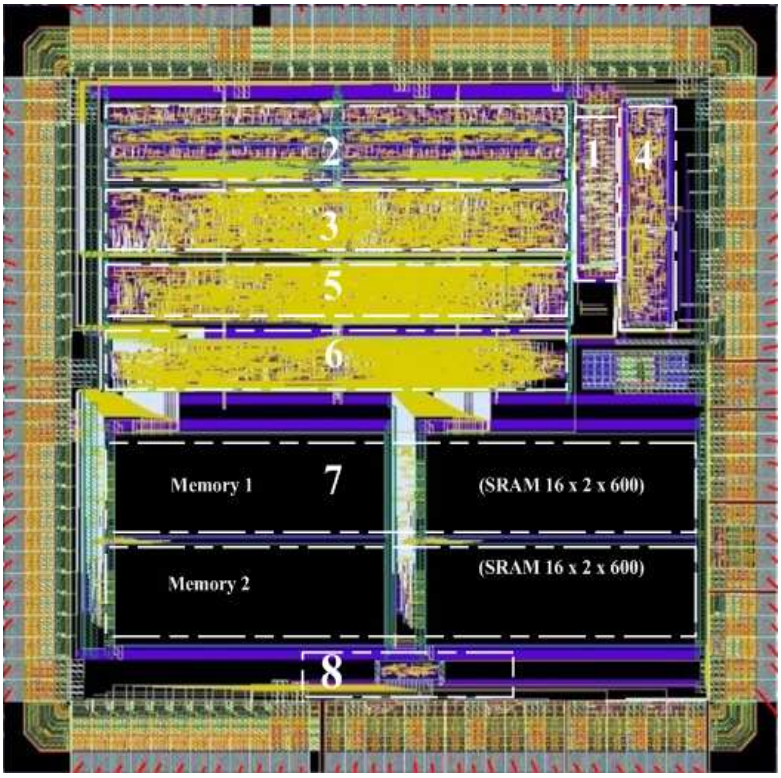


Figure 7: Detection efficiency (left) and fake hit rate (right) as a function of discriminator threshold measured on a $\sim$ 120 GeV π^- beam at the CERN-SPS for a MIMOSA-22bis sensor exposed to 150 kRad integrated dose. The chip response is displayed for various sub-arrays. The threshold values are expressed in SNR units.

architecture is chosen properly and the discriminator thresholds are set around 5 times the SNR.
In conclusion, the sensors exhibit a tolerance to ionising radiation which is satisfactiory enough for its standard use. The noise increase consecutive to irradiation is however more significant than expected from previous studies. It is therefore likely that additional studies will bring substantial improvement. It is in particular suspected that some transistors of the amplification micro-circuit integrated in each pixel are sensitive to the irradiation. It is therefore expected that a radiation tolerant design of these specific transistors would still mitigate the sensitivity of the pixel to ionising radiation.

4 Zero-suppression micro-circuit SDC-2

The SDC prototype 2 features the micro-circuits allowing to select those pixels of a frame having collected a signal charge superior to the discriminator threshold. The consecutive data flow reduction will allow running the telescope on high intensity particle beams.
The chip was fabricated in 2007, mainly composed of zero-suppression micro-circuits combined with output memories. Its logic features two consecutives steps. The first one addresses groups of 64 columns and considers up to 6 series of $\leq$ 4 consecutive pixels hit in a row. When selecting a group of pixels, it provides their address in a compact way which minimises the size of the information transmitted to the second level of the



Part 1:
JTAG

Part 2:
Priority Look Ahead algo.

Part 3 & 4:
Sequencer for row, frame & memory synchronisation

Part 5:
Selection of 9 states among 2 x 6 states

Part 6:
Memory management

Part 7: FIFO
2 blocks of memories with M states storage

Part 8:
Serial transmission

Figure 8: Layout of SDC Prototype 2, alias SUZE-01.

logic. The latter combines the results of the logic attached to the different groups of 64 columns. SDC-2 is restricted to 2 groups of 64 columns. The encoded information delivered by the logic feeds an output memory. The memories are duplicated in ordre to allow simultaneous writing in one memory, while a neighbouring one is being read out from the outside world. Figure 8 displays the layout of the chip.
The chip functionnality tests started in 2007 and continued until Spring 2008 in ordre to investigate its response to a large variety of pixel patterns. The tests demonstrated that the pixel selection and information encoding are fully operationnal. They work as expected up to clock frequencies as high as 115 MHz, i.e. 1.15 times the nominal frequency. These results validate the architecture for its integration in the TC design.

5 Final sensor TC

Designing the final telescope sensor consisted in interconnecting the IDC with the SDC-2, while extending them from 128 to 1152 columns, each ended with a discriminator. The pixel pitch (18.4 μm) and the number of pixels per column (576) remain unchanged. The total number of pixels of the sensor ($\sim$ 660 000) corresponds to a sensitive area of $\sim$ 21.$\times$10.6 mm^2.
The chip operation will start with a slightly slower read-out than the IDC because of the large number of discriminators (1152) working in parallel. The initial frequency will

be set to $\sim$ 9 000 frames per second. It will then be increased progressively, making sure that the discriminators stay all well synchronised and provide a well controled uniform threshold value. The ultimate operation speed will thus be reached after the sensor commissioning.
The pixel architecture selected among the different variants assessed with the IDC, features a so-called radiation tolerant charge collection system, where the effects of high ionising radiation doses are alleviated by protecting the charge sensing diode from potential parasitic charge accumulation and leakage current increase.
The read-out logic is a so-called rolling shutter mode, which processes the pixel signals row by row in serial mode. For each row, up to 9 series of ≤ 4 consecutive hit pixels can be processed. The signals delivered by the sensor are transmitted to the outside world either through a single output driven at $\geq$ 80 Mbits/s or through a pair of outputs, each operated at $\geq$ 40 Mbits/s.

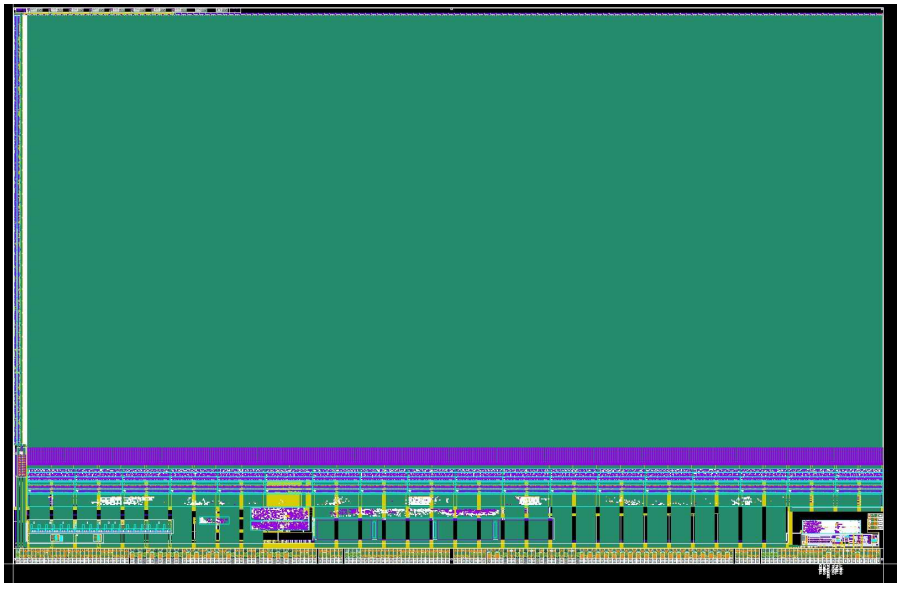


Figure 9: Layout of the final sensor (TC) foreseen to equip the EUDET beam telescope. The uniform green surface stands for the sensitive area. The signal processing circuitry is integrated at the chip periphery visible at the bottom, complemented with a narrow, $< 400\ \mu m$ wide, vertical band visible on the left, used for the row by row addressing. A $\sim 200\ \mu m$ wide band along the top of the picture contains the circuitry achieving the (slow) read-out of the pixels for their individual functionnality tests.

The chip steering is provided by JTAG. Contrary to the IDC, all columns are ended with a discriminator, which forbids controling the raw pixel signals during the nominal operation of the sensor. Nevertheless, the possibility remains to address pixels directly at low frequency in ordre to investigate sources of potential dysfunctionning. Figure 9 displays a layout of the chip.

The sensor layout was ready to be sent to the AMS foundry in Novembre 2008, for manufacturing in exactly the same 0.35 μm feature size technology as the IDC, with a 14 μm thick epitaxial layer. The fabrication had however to be delayed until Decembre 2008 because of weaknesses observed in the simulated reactivity and stability of some of the discriminators, implemented at one end of the sensor. These features could only be spotted once the simulation software of the complete operation of the sensor, which is extremely time consuming due to its complexity (being composed of several tens of millions of transistors), could be ran reliably and with an affordable duration. The correction of the design weaknesses took a couple of weeks only. The sensor is finally expected to come back from fabrication around the middle of February 2009.

6 Summary and conclusion

The last steps necessary to define and validate the inputs to the architecture of the final sensor supposed to equip the EUDET beam telescope were all achieved in 2008. They consisted in assessing two complementary chips (IDC and SDC-2) adapted to a nineth of the final sensor surface, i.e. to 128 columns of 576 pixels read out in parallel. One chip (IDC) addressed the design of the pixels and of the columns ended with discriminators. The other chip (SDC-2) addressed the downstream part of the read-out chain, essentialy composed of zero-suppression micro-circuits and output memories.
The IDC was shown to achieve the ambitionned read-out frequency of $\sim 10^4$ frames per second with a signal processing capacity of at least 100 hits per frame and per cm^2. Numerous variants of pixel architecture were investigated. Several of them were shown to provide a SNR $\gtrsim 17$, translating into a minimum ionising particle detection efficiency > 99.5 % for discriminator threshold values high enough to keep the fake hit rate below 10^{-4}. This rate value ensures that the signal processing micro-circuits will not be saturated by pixel noise fluctuations. Finally, a single point resolution better than 4 μm was observed, i.e. substantialy less than the binary resolution (5.3 μm) associated to the pixel pitch (18.4 μm). The resolution achieved translates into an extrapolated impact position on the surface of the Devices Under Test (DUT) known with $\lesssim 2$ μm accuracy, which fully satisfies the telescope specifications.
Among all pixel variants implemented in the IDC, the one retained for the final sensor was selected on the basis of its tolerance to ionising radiation. It was shown to withstand doses in excess of 150 kRad at room temperature, a value which is likely not to be reached before several years of operation. The perspectives of an intensive use of the telescope (due to its success) at hadron machines triggered nevertheless an additional effort to adapt the pixel design to doses close to 1 MRad.
The SDC-2 was tested extensively in the laboratory until Spring 2008 with millions of patterns at its nominal clock frequency (i.e. 100 MHz) and above. No failures were spotted for frequencies up to 115 MHz, i.e. 15 % higher than the nominal frequency at which the circuits will be operated once integrated in the final sensor. This safety margin guarantees that the micro-circuits are suited to the TC specifications.

The TC was designed during Summer and Autumn 2008. It combines the architecture of the IDC with the one of the SDC-2 in a complete charge sensing and signal readout chain, providing discriminated signals in a binary mode including the pixel address. The design was facing two difficulties, one consisting in ensuring the connection between the IDC and the SDC-2 and the other reflecting the extension of both chip designs from 128 to 1152 columns. The validation of the sensor design required lengthy and complicated simulations. Once their reliability was established, it became clear that part of the discriminators, concentrated at one end of the sensor, did not operate with the expected robustness. Implementing the required design modifications took a couple of weeks, translating into a fabrication start delayed to Decembre 2008. The sensor is now expected to come back from foundry around the middle of February 2009.
The realisation of the steering and test equipment necessary to characterise the sensors is well advanced and will allow to start validating the TC architecture for its use in the EUDET beam telescope as soon as the sensors come back from the foundry. The chip characterisation in the laboratory is then expected to take a couple of weeks only.

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