

### JRA2 SITRA Silicon Tracking Infrastructure

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#### Abstract

The JRA2-SITRA task of EUDET project aims in creating silicon tracking infrastructure that will be available to users at the beam tests to obtain information on track of the beam particles.

It consists of several key components necessary for charged particle track determination (silicon sensors, readout electronics, cooling, 3D table, etc.). The readout system is adapted for synchronization with other systems (telescopes, DUT).

This infrastructure is a completion of a EUDET deliverable No. JRA2-D14.

# 1 Introduction

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## 2 Module prototypes

Several prototypes of tracker modules have been designed and constructed. The detailed description of the last one can be found at [1].

### 2.1 Sensors

Dedicated silicon strip sensors have been designed by HEPHY Vienna and manufactured in Hamamatsu (see Fig. 1). The wafer was approximately 320 micron thick and a resistivity of 6.7 k $\Omega$ cm of the bulk material was chosen such that the full depletion voltage of the sensor fell between 50 and 100V. The sensors are single sided AC coupled and their dimensions are 91.5 x 91.5 mm<sup>2</sup>. They have 1792 readout strips with a strip pitch of 50 µm. The strips are connected to the bias line using poly-silicon resistors with a resistance of 20M $\Omega$ . More details about the sensors can be found at [2].

The precision required for the measurement of the momentum of charged particles is better than the structural stability of the tracker and its elements. A system that measures the stability of the whole structure is then needed. Indeed, prior to an exhaustive track alignment, a hardware alignment system can provide very useful, precise (better than 100  $\mu$ m) and fast (<1 s) reconstruction of selected modules of the tracker system. This serves as a starting point for the track algorithms.

Matching the global ILC material budget reduction philosophy, a system based on infrared laser tracks has been proposed within the SiTRA task. This system, based on former AMS and CMS predecessors, modifies few microstrip detectors opening a ~1 cm diameter hole in the Al backplane allowing a laser beam to pass through. Then this beam is used as an infinite momentum pseudo-track and its path reconstructed. The optical absorption of Si permits a suitably chosen infrared (IR) wavelength to traverse consecutive planes of Silicon while still leaving a signal measurable with the on-board electronics. The material burden introduced by this system is therefore minimal. Only optical fibers and one collimator per line of sight are needed.

The key parameter of this system is the transparency of the full detector (Si, metal strips, passivation...) to the chosen wavelength. A complete simulation of the propagation of light through the detector has been used to identify the strip width to pitch ratio as the most important parameter in the transmittance of a module [3]. In short, the thinner strips, the more light can be propagated. Then, a further optimisation of the material thickness of the layers leads to constructive interference of the transmitted beam, well beyond the best performance of AMS and CMS predecessors. We have calculated a maximum transmittance of 75% with these minor modifications in the alignment window.



Figure 1: Hamamatsu silicon wafers

#### 2.2 Electronics

In the context of the Silicon for a Linear Collider (SiLC) R&D, a highly compact 88-channels mixed-signal chip has been designed in 130nm CMOS technology intended to read Silicon Strip detectors for the experiments at the future International Linear Collider. The chip is designed in collaboration between the Paris High Energy Physics Laboratory (LPNHE Paris) and the Electronic Department at the University of Barcelona. Optimized for a detector capacitance of 10pF, it could be configured according to the detector to be implemented. It includes eighty eight channels of a full analog signal processing chain and analog to digital conversion, with the corresponding digital controls and readout channels. The chip is  $5x10mm^2$  where the analog implementation represents 4/5 of the total silicon area. The chip parameters as well as the achieved chips performance is described in a detail in [4].

#### 2.3 Mechanics



Figure 2: Silicon module prototype

Silicon strip sensors are glued on a baseboard and connected to the hybrid populated with the front end chips via a fanin. Several readout chips were used in history of the project (VA1,

APV25 and SITRA dedicated SITR-180 and SITR-130). All the components are attached to the frame (see Fig. 2). Modules were constructed in Karlsruhe, Vienna and Paris.

# 3 DAQ

The data acquisition system brings data from the chips to the computer. Various methods were used in past. Current prototypes used in the infrastructure utilize the fact, that digitization is performed at the FE chip level, so no A/D converter is needed in the DAQ system. However, for the compatibility with the previous module electronics the system allows use of several chip flavors. Fig. 3 shows the mixed system. The data are handled via FPGA Altera (Fig. 5) and sent to PC via a USB link.

The system has been designed in a way that enables synchronization with other DAQ systems. There are various possibilities: working on trigger/busy signal level, using TLU for synchronization, using common DAQ system.



Figure 3: DAQ scheme

GA board 1	FPGA board 2	FPGA board 3
PGA Id 0	FPGA Id 0	FPGA Id 0
FEE Eoards VA1 - FEE 1 VA1 - FEE 2 SITr - FEE 1 SITr - FEE 2 SITr - FEE 3 Load FPGA Configure FPGA	FEE Boards VA1 - FEE 1 VA1 - FEE 2 SITr - FEE 1 SITr - FEE 2 SITr - FEE 3 Load FPGA Configure FPGA	FEE Boards VA1 - FEE 1 VA1 - FEE 2 SITr - FEE 1 SITr - FEE 2 SITr - FEE 3 Load FPGA Configure FPGA

Figure 4: Screenshot of a configuration dialog from the DAQ SW



Figure 5: DAQ card

## 4 Cooling

Depending on the cooling needs of the detector-under-test two cooling systems can be used. One is based on the convection cooling, while the other exploits conduction. The systems are described in [5] and [6]

## 5 Mechanical arrangement, 3D motorized table

The tested system as well as reference detectors are positioned at the 3D motorized table. Two 3D motorized tables are part of the infrastructure.

#### Paris table:

A 3-dimensional motorized table has been built by the LPNHE team and it is used for the Lab test bench to test the Silicon modules prototypes and for the test beam at CERN. It is currently piloted with a program LABVIEW based. Figure 6 shows the photograph of the table.

The table dimensions (LxWxH) are  $700x250x200 \text{ mm}^3$ . The precision of movement is  $\pm 10\mu\text{m}$  on both the length and the height and allows steps of 5  $\mu\text{m}$  on the transverse direction. This permits very fine scans of the sensor strip structure when testing it with a laser on the lab test bench. It allows moving the box with the small Silicon modules equipped with the new FE readout DSM chips, tested last year and in the first test beams in 2008.

### Torino table

Another 3D table allowing moving larger size Silicon tracking prototypes has been constructed at University of Torino/Torino-INFN (Figure 7).

It consists of the base and the platform that could be moved in vertical, ( $\pm$  20cm), and transverse to the beam ( $\pm$  10cm) to align the hodoscopes and scintillators to the beam line. On the platform the hodoscopes are fixed, and allow the Detectors Under Test (DUT) to be aligned and displaced with respect to the hodoscopes. The center of the platform has 3 movements:

- Z, vertical, to align the sensors vertically with respect to the beam in different positions
- Y, transverse to the beam
- phi, rotation around Z

The platform has dimensions (X,Y,Z) of  $150x27x4.5 \text{ cm}^3$ . Basic profile system by BOSCH-REXROTH is used that allows aligning easily. It is flexible enough to allow any kind of DUT, from 4 x 15 x  $15\text{cm}^3$  to 20 x 40 x20 cm<sup>3</sup>. The DUT is mounted on top of a rotating head that could easily interface to any DUT size. The details of the platform with the movable "head" part are shown in Figure 7. In case, the "head" could be modified according the necessity.

Both tables are described in a detail in [7]



Figure 6: Paris 3D table



Figure 7: Torino 3D table

## 6 Test beam experience

All components of the system have been subject to extensive tests not only in the labs, but also in a beam of high energy particles in DESY and CERN (see Fig. 8). Here many important aspects of the system were checked:

- synchronization with other systems
- remote control over 50 m
- noise and common-mode noise suppression
- triggering to the beam of various time structures

#### The list of test beam sessions:

Place	Year	Participants	Prototypes
DESY	2006	Paris, Prague, Santander, Karlsruhe, Obninsk, Helsinki	CMS, VA1, SITR180
DESY	2007	Paris, Prague, Santander, Karlsruhe, Obninsk	Hamamatsu, VA1, SITR180
CERN	2007	Paris, Prague, Santander, Karlsruhe,	Hamamatsu,SITR180
CERN	2008	Vienna, Prague	Hamamatsu, APV25
CERN	2008	Paris, Prague, Santander, Barcelona	Hamamatsu, SITRA130-88



Figure 8: CERN Test beam setup with the EUDET telescopes

## 7 Conclusion

The above described parts (DAQ standalone system easily integrated in a combined test beam with another EUDET subdetector, FE chips, sensors, cooling system), together with deliverables from 2007 (3D motorized table) are now combined to the Silicon Test Infrastructure. Groups, interested in testing their tracker prototypes can run in a combined mode with the infrastructure that was made available now. But the tracking information can be very useful for the other detector systems (calorimetry, muons, etc), so there may be a number of potential users of the infrastructure in the remaining 2 years of the project. The first one will be the combined test beam with the LPTPC at DESY in 2009.

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