Results from SPiDeR

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Abstract

We present test results from the "TPAC" and "FORTIS" sensors produced using the 180 nm CMOS INMAPS process. The TPAC sensor has a 50 μm pixel size with advanced in-pixel electronics. Although TPAC was developed for digital electromagnetic calorimetry, the technology can be readily extended to tracking and vertexing applications where highly granular pixels with in-pixel intelligence are required. By way of example, a variant of the TPAC sensor has been proposed for the Super$B$ vertex detector. The FORTIS sensor is a prototype with several pixel variants to study the performance of the 4T architecture and is the first 4T MAPS sensor tested for particle physics applications. TPAC and FORTIS sensors have been fabricated with some of the processing innovations available in INMAPS such as deep p-wells and high-resistivity epitaxial layers. The performance of these sensor variants has been measured both in the laboratory and at test beams and results showing significant improvements due to these innovations are presented. We have recently manufactured the "CHERWELL" sensor, building on the experience with both TPAC and FORTIS and making use of the 4T approach. CHERWELL is designed for tracking and vertexing and has an integrated ADC and targets very low-noise performance. The principal features of CHERWELL are described.

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1 Introduction

CMOS Monolithic Active Pixel Sensors (MAPS) have been pioneered since in 1990's mainly for imaging applications. The main advantages compared to CCDs are the lower manufacturing costs, the possibility of having electronics in the same substrate and the possibility for very small pixels building on the development of ever-smaller features sizes in CMOS processes. MAPS have been also proposed for particle physics [1]. There have been significant improvements from the initial designs, which now allow in-pixel electronics, better charge collections and very low-noise performance. This is mainly possible due to advanced process features becoming available for MAPS design, but also due to new epitaxial materials and improved circuitry. These improvements make it possible to achieve the requirements for detectors at future colliders in terms of granularity, speed, power and material budget.
These proceedings are organized as follows; first the INMAPS process is described, then results from the TPAC and Fortis chips that have been manufactured using the INMAPS process are presented, and finally an outlook on the new Cherwell chip and on the TPAC for Super$B$ concept is given

2 The INMAPS Process

The INMAPS process is a standard CMOS process with a feature size of 180 nm, up to six metal layers, precision passive components, low-leakage diodes and a choice of epitaxial layer thicknesses between 5, 12 and 18 μm. Additional process modules are deep p-wells, high resistivity epitaxial layers, 4T structures and stitching.
Standard MAPS collect the signal charge via diffusion using a n-well diode as shown in Fig. 1. This limits the in-pixel electronics to only NMOS transistors, as the n-well from the PMOS transistors would parasitically collect the signal charge and therefore lead to a low charge collection efficiency. This can be overcome by implanting a deep p-well, which shields the n-wells from the PMOS and therefore allows full CMOS capability in-pixel. This is also illustrated in Fig. 1.
The charge collection by diffusion in a MAPS is relatively slow O(100 ns) and radiation soft. Using INMAPS on a high-resistivity epitaxial layer (1- 10 kΩcm) has the potential benefits of a faster charge collection, a reduced charge spread and an increased radiation hardness [2].
A further technology module is the 4T (4 transistor) pixel architecture [3] shown in Figure 2. Previous MAPS used mainly a 3T (3 Transistor) approach, with a readout diode, reset transistor, a source follower transistor, and a row select transistor. In a 3T pixel, the readout diode is both the charge collection area and the node from which the signal is read within the pixel. In a 4T pixel there are three additional elements : the charge transfer gate (TX) the floating diffusion node (FD), and a pinned photo-diode. The pinned photo-diode can be fully depleted, which allows a noise-free transfer. It collects charge as long as the transfer gate is off. During readout, charge is transferred through the charge transfer gate onto the floating diffusion node and read from there.

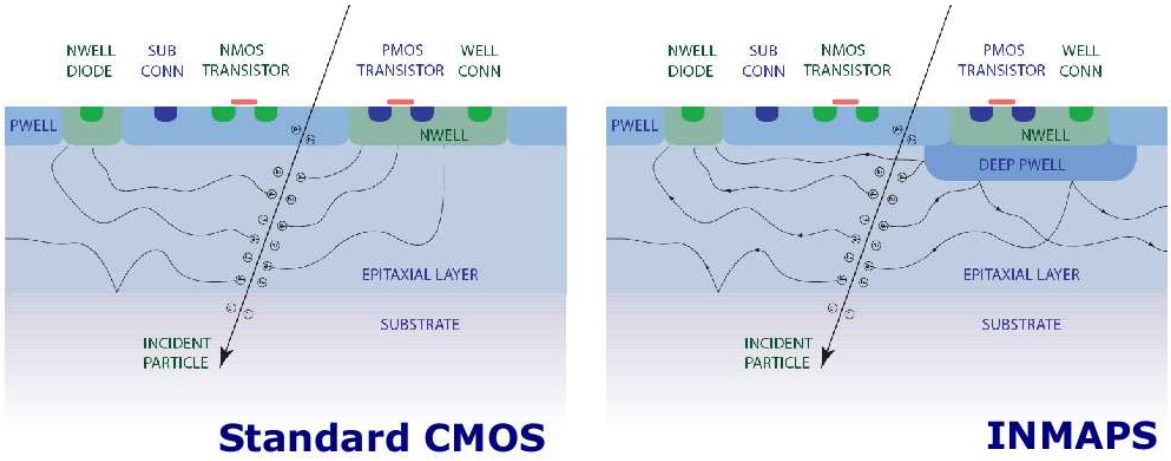

Figure 1: The INMAPS process. Left shows the standard CMOS layout without a deep p-well implant, the right one shows the PMOS n-well shielded by the deep p-well.

This leads to a separation of charge collection and the signal readout. This has two advantages, it allows the application of in-pixel CDS(Correlated Double Sampling) and a high conversion gain due to the small capacitance of the floating diffusion node. This results in the low noise performance of 4T pixels.
The most recently added module to INMAPS is the capability to do stitching. This allows to make sensors that are larger than the full reticle size, which is typically the order of 2.5 $\times$ 2.5 cm^2 in CMOS. With stitching this can be extended to produce chips with dimensions only limited by the wafer size. A technology demonstrator aimed at imaging applications has been designed at RAL with a size of 5.4 $\times$ 5.4 cm^2 [4].

3 The TPAC Sensor

The TPAC sensor [5, 6, 7]was the first chip to be designed using the INMAPS process. The target application for this sensor was a Digital Electromagnetic Calorimeter (DECAL). A DECAL counts the number of particles in the shower instead of measuring the deposited energy and therefore requires a highly granular readout sensor. The TPAC chip consists of 168 $\times$ 168 pixels with a size of 50 $\times$ 50 μm^2 and associated control logic. The total chip area is 79.4 mm^2 and it consists of 8.2 million transistors. A picture of TPAC is shown in Fig. 3.
Each individual pixel has four charge collection diodes, a pre-amplifier, a shaper and a comparator. The CR-RC shaper circuit generates a pulse in proportion to the signal received from the pre-amplifier gain to yield 150 μV/e$^-$ with respect to total collected charge. The pixel then has a 6-bit trimming register and a mask bit to disable it. Each pixel has a power consumption of 8.9 μW. The readout circuitry uses full CMOS and is therefore embedded in deep p-well as shown in Fig. 3. 42 pixels share a common row register, which contains the control logic, the time-stamping and the SRAM to store the

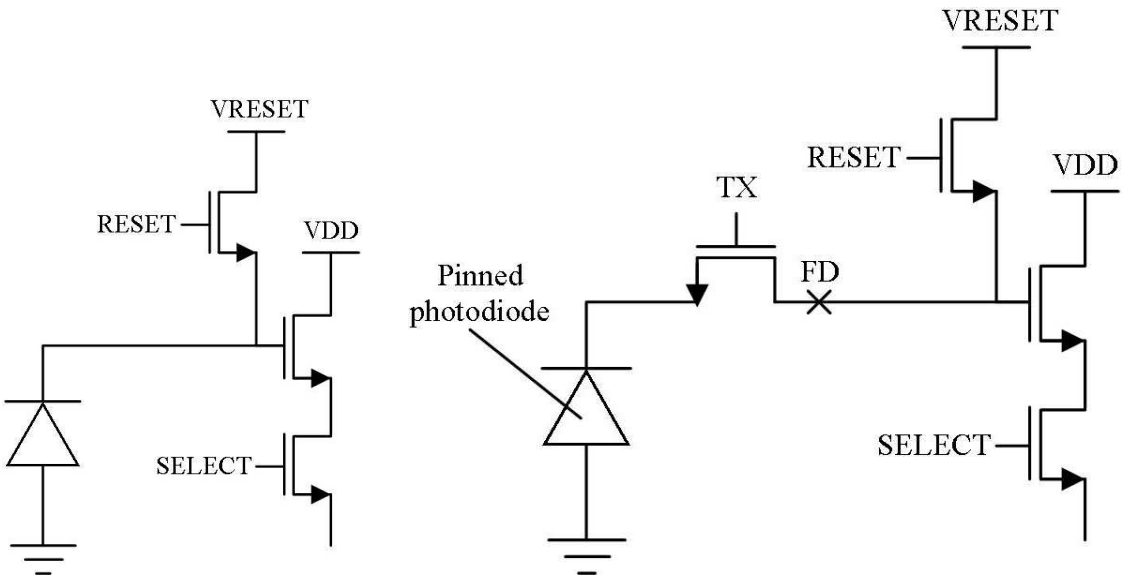

Figure 2: Left: Standard 3T CMOS pixel architecture. Right: Advanced 4T CMOS pixel architecture.

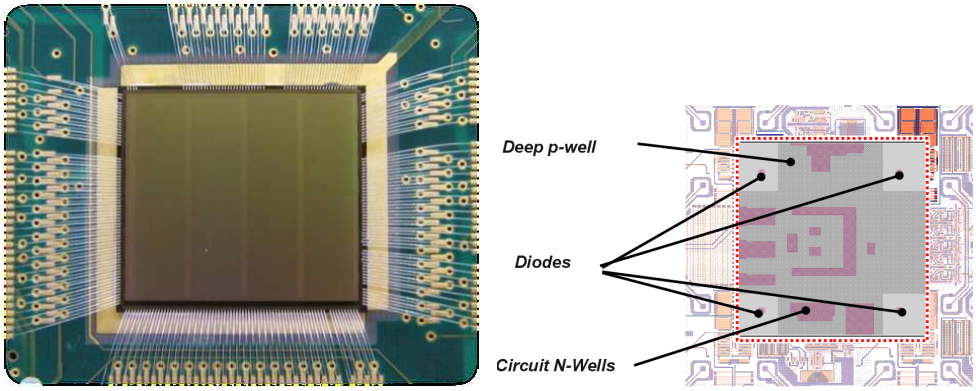

Figure 3: A photograph of TPAC 1.0 (left) and the location of four charge-collection diodes, the deep p-well and the circuit n-wells in TPAC. The pixel boundary of 50×50 μm^2 is indicated by the dotted line (right).

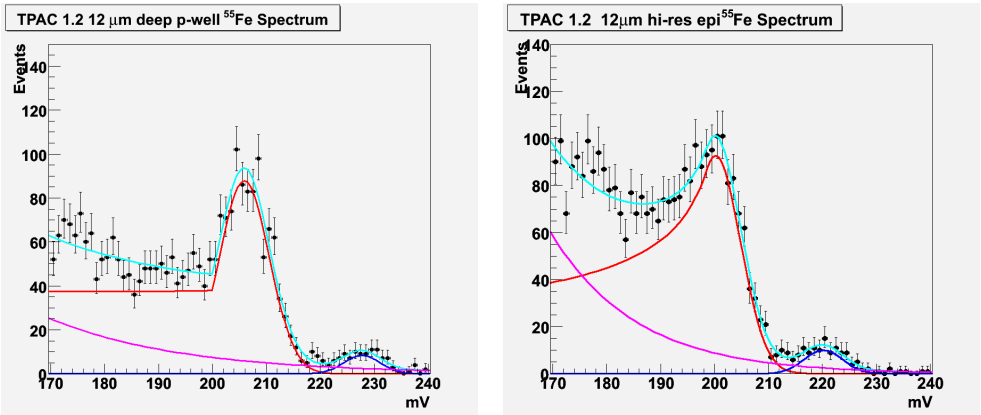

Figure 4: The Sensor response using an ^{55}Fe source for a TPAC 1.2 with 12 μm epitaxial layer and deep p-well sensor (left) and TPAC 1.2 with a 12 μm high-resistivity epitaxial layer. Both the K_α and the K_β line are clearly visible on both sensors. The different lines show the different fit contributions to the data (dots).

hits. There are four rows of control-logic, which lead to 11 % dead area on the chip. The data are then moved off-chip using a 30-bit parallel data bus. TPAC also has two test pixels with analog readout, which can be used for calibration purposes. TPAC 1.2 has been manufactured using both deep p-well and high-resistivity epitaxial layers and used epitaxial layer thicknesses of 12 and 18 μm.

The sensor has been tested using an IR laser, an ^{55}Fe source and in test beams at CERN and DESY. The response of the analog test pixels to the ^{55}Fe source are shown in Fig. 4. Both the K_α and the K_β peaks are clearly visible here. These are due to a direct hit of the photon in one of the four diodes. Charge generated from hits outside the diodes is only partially collected by the diodes, leading to the well-known exponential shape. Fig. 4 also shows that the high-resistivity material works well and does not affected the integrated electronics.

The sensor was tested in test beams at CERN in August 2009 and DESY in March 2010 using a stack of six TPAC sensors and three scintillators in the configuration shown in Fig. 5. A block of tungsten (Or iron, copper) was inserted when the TPAC stack was run in Calorimetry mode. The EUDET telescope [8] with the FORTIS sensor were run in parallel using in the same beam line. A first result direct from the TPAC online monitoring, the time difference between a triple coincidence in the scintillators and the hits in the TPAC sensors is shown in Fig. 6. Of the six sensors five show a clear peak around 0, while the sixth sensor appears to be much more noisy. This is due to the fact, that it does not use a deep p-well, hence the benefit of having a deep p-well are already clearly visible in the online monitoring. The tracking efficiency was then found by using four TPAC planes to perform the track finding and then deriving the MIP detection efficiency of the two inner planes, This was done for several threshold values. The results are shown in Fig. 7. The version without a deep p-well shows a very low MIP efficiency. The inclusion of the deep p-well then boosts the detection efficiency up

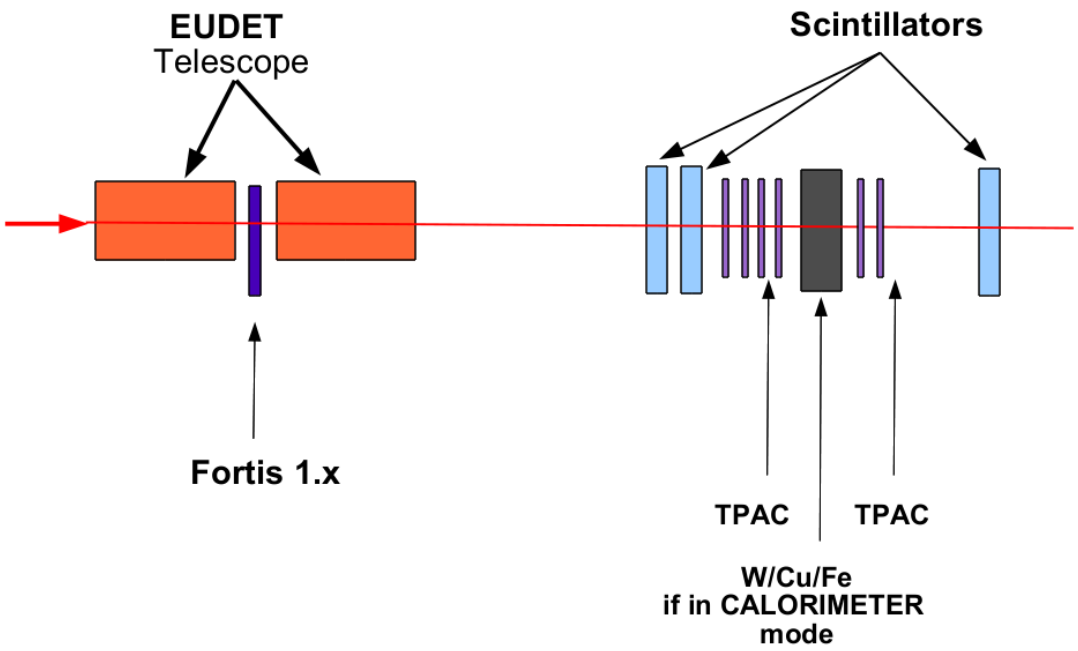

Figure 5: .The Test beam setup used for the test beams at CERN and DESY using the EUDET telescope and the FORTIS and TPAC sensors.

to around 80-85%. The addition of the high-resistivity epitaxial layer then makes TPAC close to a 100 % efficient.

4 The Fortis Sensor

FORTIS [10, 11] has been developed as a demonstrator for the 4T-pixel architecture with a standard rolling-shutter readout and an analog output. Two iterations were made containing 12 and 13 different variants of the basic 4T architecture. The variants include the size of the source follower, the size of the collecting diode, the pixel pitch (6-45 μm) and combined diodes at the floating diffusion node. Furthermore, FORTIS 1.1 also used variants with a deep p-well and a high-resistivity epitaxial layer.
FORTIS has been tested using the Photon Transfer Curve (PTC) technique [12] and using an ^{55}Fe source. The most-probable noise was $< 5e^-$ with a gain of 65 $\mu V/e^-$, as can be seen in Fig. 8. The results using ^{55}Fe show similar results, proving that the 4T architecture offers an excellent low-noise performance.
Up to now 4T architectures have been predominantly used in imaging applications and FORTIS was the first one to be taken to a test beam. Test beams at CERN and DESY using the EUDET telescope and the setup shown in Fig. 5 have shown that FORTIS does detect particles and that the noise performance is excellent. The first preliminary analysis has focused on the C variants which have 15 μm pitch and different source follower transistor variants. Results for the noise distribution and cluster charge are

shown in Fig. 9 for the FORTIS 1.1 Variant C1 using standard CMOS without a deep p-well or a high-resistivity epitaxial layer.
The resulting signal-to-noise ratio is about 87 for C1 on standard CMOS. The preliminary signal-to-noise ratios for the four C variants have been measured, also depending on the processing variant. This is shown in Fig. 10.
The test beam data from remaining pixels variants of FORTIS are currently being analyzed.

5 The Cherwell Sensor

Building on the experience with the TPAC and FORTIS, the CHERWELL chip has been designed as a demonstrator for a pixel tracking chip. It uses the INMAPS process with high-resistivity epitaxial layers and the 4T architecture. Several new ideas are tested in this design, the usage of embedded electronic "islands", where part of the column logic is embedded in the column instead of being at the end and the usage of the Strixel approach by sharing electronics for one column. It is planned to make two iterations, CHERWELL as technology testbed and in a second iteration CHERWELL 2 as a larger device. The embedded electronics Islands are possible, because the deep p-well allows us to embed full CMOS within the empty areas of the 4T-pixel. Therefore the entire column-end logic can be moved into these islands thereby reducing the dead area at the end of the column to a minimum. This is illustrated in Fig. 11.
For the first iteration chip, CHERWELL, a size of 5×5 mm^2 was chosen, incorporating four different variants using a common backend with a ramp-based ADC with 10-bit resolution per column.(see Fig. 11). Two variants are technology demonstrators for a future DECAL chip, which will be a large-area device for digital electromagnetic calorimetry. The DECAL variant provides a global shutter with in-pixel storage, so it can be used in a triggered mode and it provides CDS as well. The difference between the two variants is the pixel pitch, either 25×25 μm^2 or 50×50 μm^2. A summing circuit allows us to sum up the charge of four 25×25 μm^2 pixels to form a virtual 50×50 μm^2 pixel. This tests the benefits of a single-diode versus a multi-diode approach for relatively large pixels. The two other variants test the Islands approach with the in-pixel electronics. Both variants have a pixel pitch of 25×25 μm^2 and are read out using a rolling-shutter approach. In the first variants, there are embedded deep p-wells islands between the pixels, although there is no active electronics located in there. The second variant has the per-column ADC folded into the pixel using the deep p-well islands. The devices have been produced and just been delivered to RAL.

6 TPAC for Super$B$

For the proposed Super$B$ project in Italy [13, 14, 15], a high-luminosity B-Factory, an all-pixel vertex detector concept based on a modified version of the TPAC cjip has been proposed as an option [13]. This proposal uses a modified version of the TPAC chip

as described in Section 3. The vertex detector requirements for Super$B$ involve dealing with an almost DC beam (5 ns bunch spacing) and large backgrounds, so even with a finely pixelated vertex detector with 50 $\times$ 50 μm pixels, the hit rate per pixel is 2.5 kHz. To keep the occupancy low, a snap shot of the vertex detector is made every 500 ns. The poroposed derivative of TPAC adds a peak-hold circuit in each pixel and an 4-bit pipelined ADC at the end of each column. The hit flag is used to timestamp the hit and the ADC only digitizes pixels with a hit-flag, therefore having in-column sparsification. In order to increase the throughput, the ADC has been implemented as a four-stage pipeline This is currently a conceptual design study, but may go ahead after the approval of the Super$B$ project by the Italian government.

7 Conclusion

The recent advances in the INMAPS process have been summarized and the latest results from the TPAC and FORTIS chips have been presented. The deep p-well and the high resistivity epitaxial layers solve some of the most important limitations of MAPS technology in terms of full CMOS capability and charge collection efficiency. The CHERWELL chip using INMAPS and new design approaches has just been received and a conceptual design study for an INMAPS based chip for Super$B$ has been presented.

8 Acknowledgment

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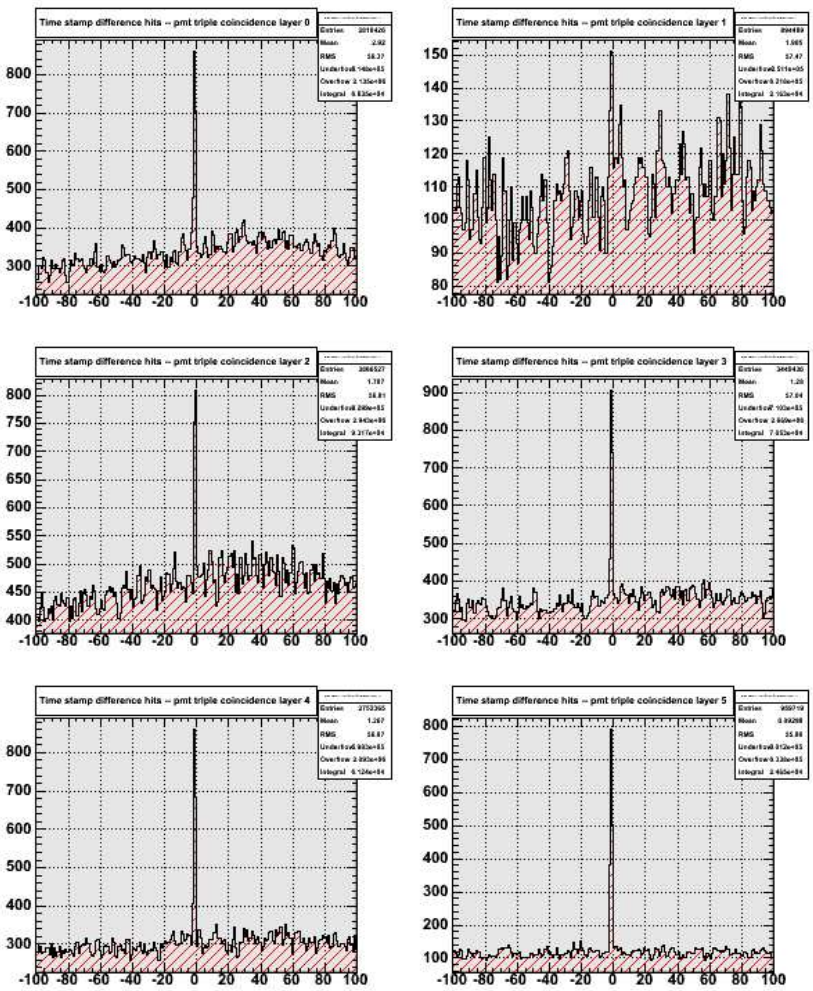

Figure 6: .The time difference between a scintillator triple coincidence and the hits in the TPAC for the 6 planes in the TPAC stack. Five of them are made with a deep p-well, while the sixth (upper right) is using standard CMOS technology.

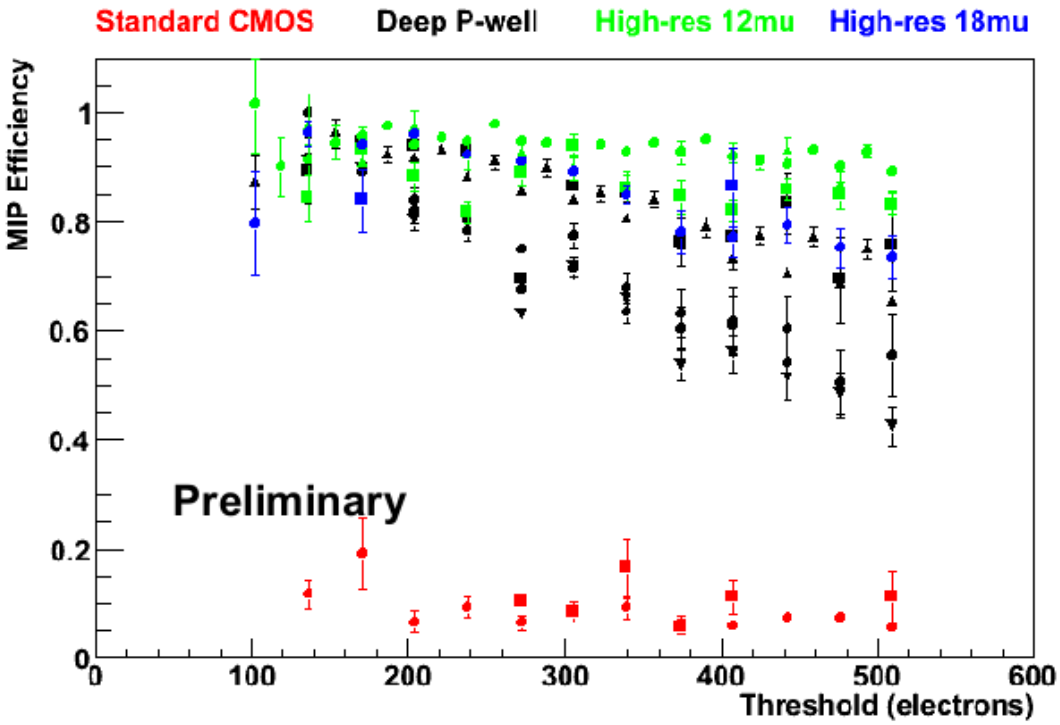

Figure 7: .The MIP detection efficiency as a function of the comparator threshold for different process variants of TPAC 1.2; no deep p-well implant, deep p-well implant and high-resistivity epitaxial layer (all 12 μm) and 18 μm high-resistivity layer [9].

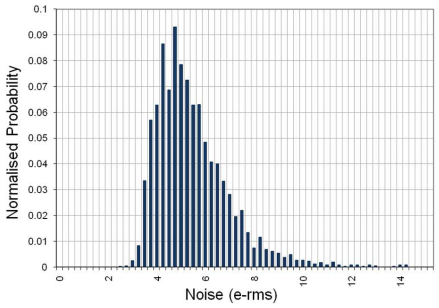

Figure 8: The noise distribution in the FORTIS B2 pixel using the Photon Transfer Curve Technique

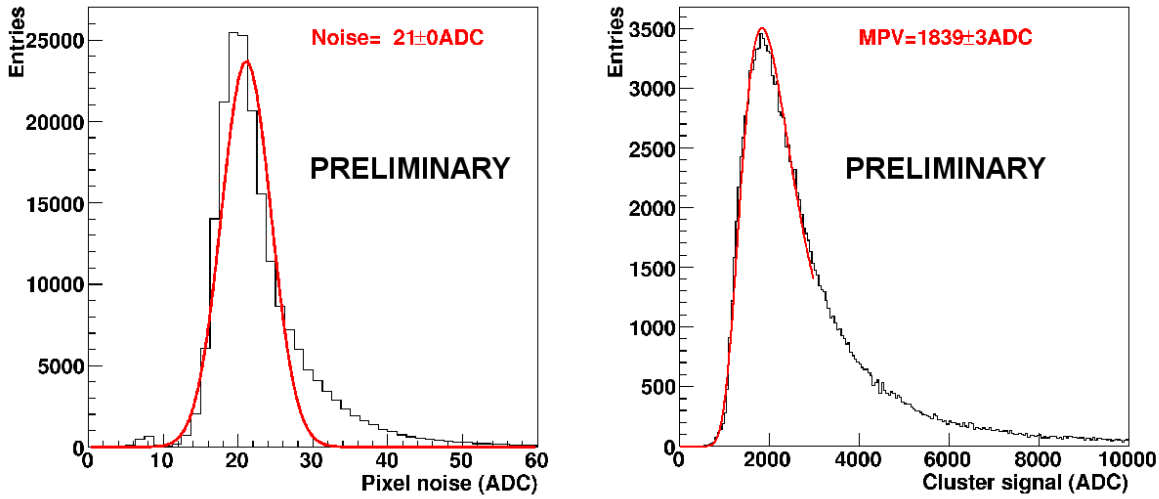

Figure 9: The average Noise (left) and signal cluster charge (right) for the C1 variant of Standard CMOS Fortis 1.1

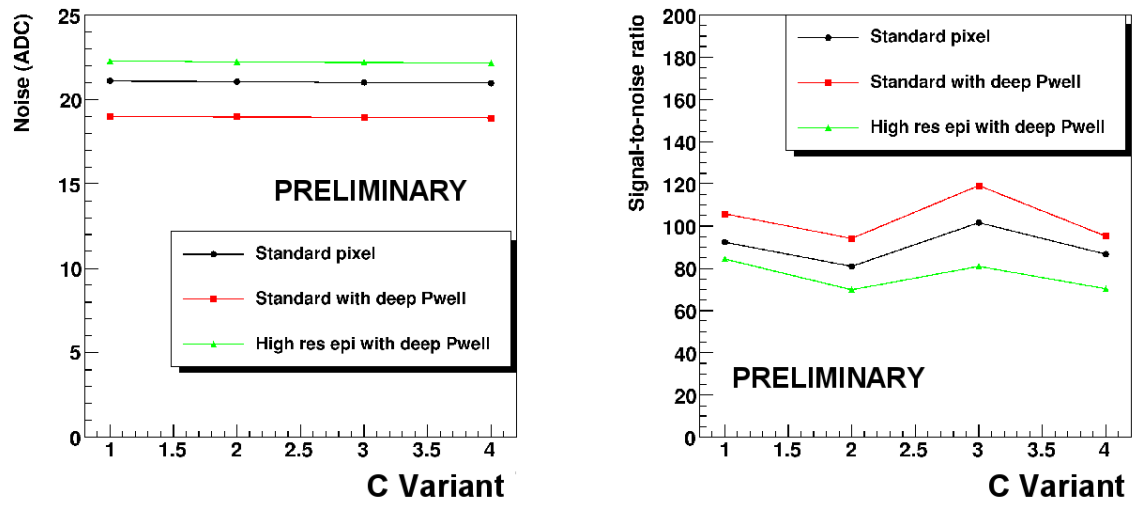

Figure 10: The average noise (left) and the signal-to-noise ratio (right) for the four C pixel variants of Fortis 1.1. The three lines indicate the different processing variants.

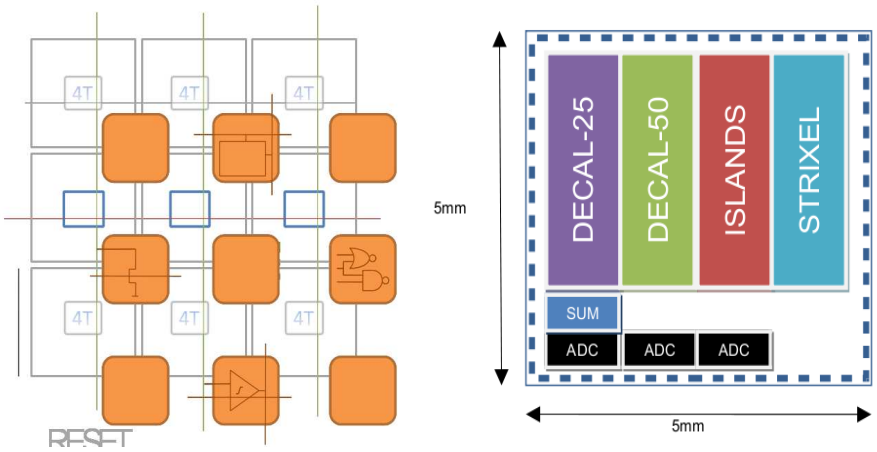

Figure 11: The embedded electronics island approach as it has been envisaged in CHERWELL. The islands (orange) are located in between the 4T pixels (left). The floor plan of the CHERWELL chip with the four different variants (right).

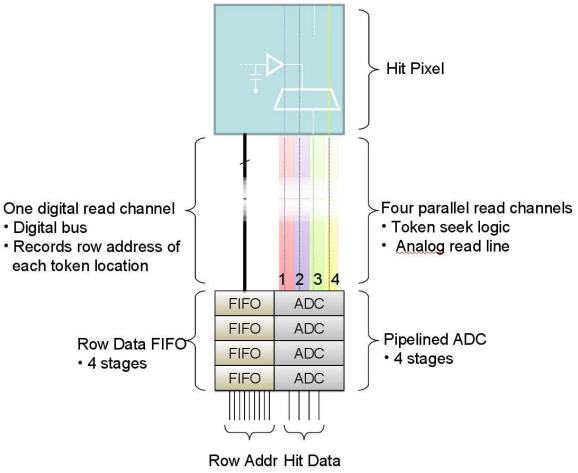

Figure 12: The TPAC for Super$B$ design showing one pixel and the column-end logic with the four-stage pipelined ADC,the row-data fifo and the token-seek logic.