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A large scale prototype for a SiW electromagnetic calorimeter for a future linear collider - EUDET Module

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Abstract

The CALICE collaboration is preparing large scale prototypes for highly granular calorimeters for detectors to be operated at a future linear electron positron collider. During the years 2010-2012 a prototype of a SiW electromagnetic calorimeter will be assembled which in terms of dimensions and layout meets already most of the requirements given by the linear collider physics program and hence the detector design. In particular the front end electronics will be embedded into the layer structure of the calorimeter and have to fit within alveolar layers with less than 1 cm in height. In this contribution the design of the prototype is presented and the steps towards its realisation will be presented. First results on thermal dissipation and mechanical stress the module will suffer from can be reported. These results were obtained with a first version of the module at the end of 2009.

1 Introduction

The next major worldwide project in high energy particle physics will be a linear electron positron collider at the TeV scale. This machine will complement and extend the scientific results of the LHC currently operated at CERN. The most advanced proposal for this linear collider is the *I*nternational *L*inear *C*ollider, *ILC*. Here, electron and positrons will be collided at centre-of-mass energies between 0.2 and 1 TeV. The detectors which will be installed around the interaction point are required to achieve a jet energy resolution of $30\%/\sqrt{E}$, thus a factor two better than the energy resolution achieved for a typical detector at LEP. The reconstruction of the final state of the e^+e^- will be based on so-called *p*article *f*low *a*lgorithms, *PFA*. The goal is to reconstruct every single particle of the final state which in turn demands a perfect association of the signals in the tracking systems with those in the calorimeters. As a consequence this requires a perfect tracking of the particle trajectories even in the calorimeters. To meet these requirements the detectors have to cover the whole solid angle and have to feature an unprecedented high granularity.

2 Towards a technological prototype for the SiW electromagnetic calorimeter

The application of PFA requires a perfect reconstruction of the particle trajectories in the calorimeter. For this, the calorimeters have to be placed inside the coil of the superconductive solenoid of the detectors. This puts tight constraints on the available space for the installation of the detectors. The design of the detector components and notably of the calorimeters have to take the following guidelines into account

- Optimisation of the number of calorimeter cells.
- Choice of the absorber material and the infra-structural components such as cooling, power supplies, readout cables and the very front end electronics.

For the electromagnetic calorimeter which surrounds the tracking chambers these criteria has lead to the choice of tungsten with a radiation length of X_0=3.5 mm, a Molière of R_M=9 mm and an interaction length of λ_I=96 mm. In the years 2005 and 2009 the CALICE collaboration has performed beam campaigns at DESY, CERN and FNAL in order to demonstrate the principle of highly granular calorimeters and to confront the concept of particle flow with real data. For these beam test campaigns a small *physics prototype* [1] was constructed. The first results of the data analysis have been published in three articles [1, 2, 3]. The next prototype, also called EUDET Module, has been conceived during the year 2008 [5] and enters now its construction phase. It addresses, more than the first prototype, the engineering challenges which come along with the realisation of highly granular calorimeters. The key parameters of the new prototype are

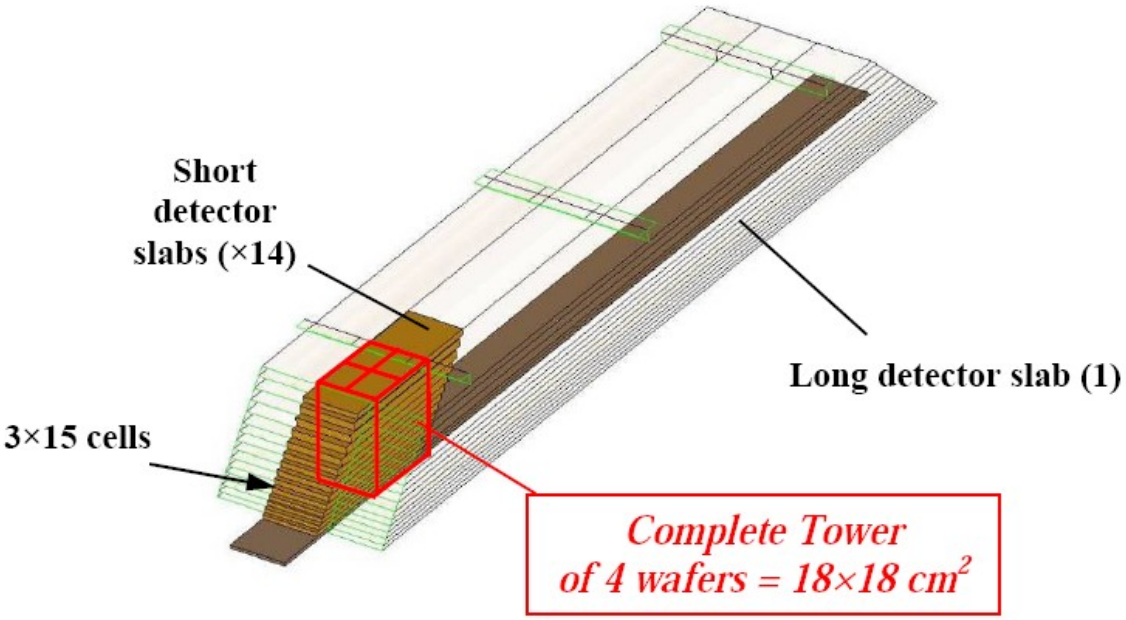

Figure 1: *A schematic 3D view of the technological prototype.*

- Size of an individual cell of 5.5x5.5 mm^2.
- A depth of 24 X_0.
- Thickness of an individual layer of 3.4 mm and 4.4 mm according to the position within the calorimeter.

2.1 Overall design

The details of design and manufacturing techniques are given elsewhere [4, 5]. Here only the most important points of the design are recalled. With a size of $1560 \times 545 \times 186\,\mathrm{mm}^3$, the technological prototype has similar dimensions as the modules envisaged for e.g. the ILD detector [6]. Figure 1, shows the design of the alveolar structure with 3 columns of alveoli. The sensitive layers are mounted onto both sides of a H shaped board which incorporates part of the tungsten absorber, see also below. Such an entity is called a *slab*. The slabs will be inserted into the middle column of the alveolar structure. The technological prototype has the following sampling at normal incidence: 22.8 X_0 are filled with 20 layers of 0.6 X_0 (2.1 mm) thick tungsten absorber plates, followed by 9 layers of 1.2 X_0 (4.2 mm) thick plates. All but two detector layers have an active area of $18 \times 18\,\mathrm{cm}^2$ segmented into read out cells, or pixels, of $5.5 \times 5.5\,\mathrm{mm}^2$ lateral size which in turn are grouped into 2×2 matrices consisting of 16×16 pixels each. Two layers are given by a *long slab* featuring 16 of these $18 \times 18\,\mathrm{cm}^2$ units. All thirty layers together will comprise 45000 readout channels in total. Table 1 lists the main parameters in comparison with those of the physics prototype.

	Physics Prototype	Technological Prototype
Subdivision	3 Structures	1 Structure
W Thickness $n \times d_W$ [mm]	$10 \times 1.4 + 10 \times 2.8 + 10 \times 4.2$	$20 \times 2.1 + 9 \times 4.2$
Depth [X_0]	24	23
Dimensions [mm^3]	$380 \times 380 \times 200$	$1560 \times 545 \times 186$
Smallest Slab Thickness [mm]	8.3	6.8
VFE	outside	inside
# Channels	9720	45360
Weight [kg]	200	700

Table 1: *A comparison of parameters of the physics prototype and the technological prototype of the SiW Ecal.*

The Figure 2 shows a sketch of the entire alveolar structure and a cross section through one slab. A most prominent change with respect to the physics prototype is that for this technological prototype the very front end electronics will be integrated into the layer structure.

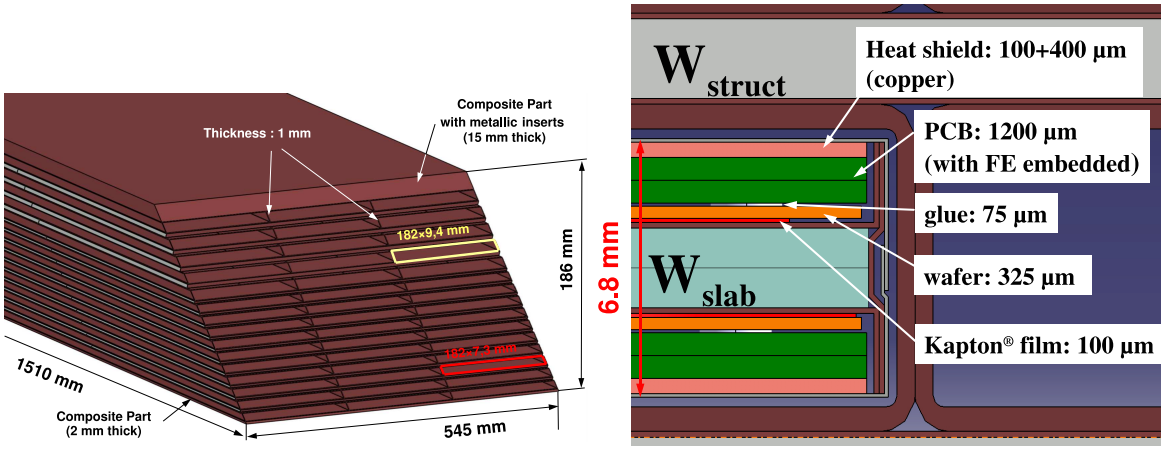

Figure 2: *Left: Alveolar structure and its dimensions which houses the sensitive parts of the technological prototype. Right: Cross Section through a slab for the technological prototype. The sensitive components and very front end electronics are mounted on two sides of a tungsten carbon composite plate. The whole slab is embedded in alveolar layers.*

This high level of compactness puts tight tolerances on the size of individual pieces of read out electronics. The ensemble of *p*rinted *c*ircuit *b*oard, *PCB* and *a*pplication *s*pecific *i*ntegrated *c*ircuit, *ASIC*, must not be higher than $1200\,\mu m$. In addition, there is no active cooling to act on the heat produced by the ASICs. Therefore, the ASICs are required to be as little power consuming as possible. As indicated above and illustrated in Figure 3, a long layer will be equipped with 8 units consisting of 1024 readout cells each.
These cells will be glued onto a PCB and equipped with the readout ASICs. The unit of Silicon Wafer, PCB and ASICs is called *a*ctive *s*ensor *u*nit or *ASU*. Each layer will be

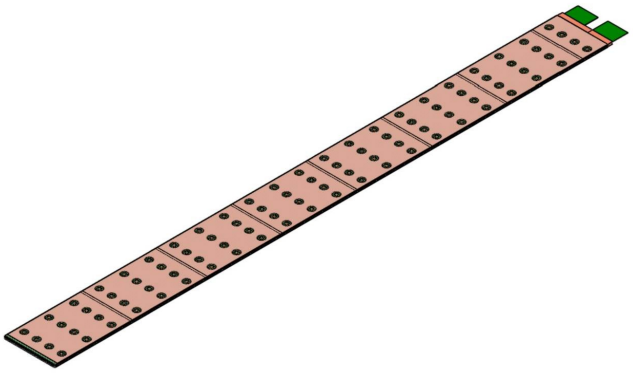

Figure 3: *Subdivision of a layer into Active Sensor Units (ASUs). The picture shows an older design with only 7 ASUs. In the current design a layer will comprise 8 ASUs.*

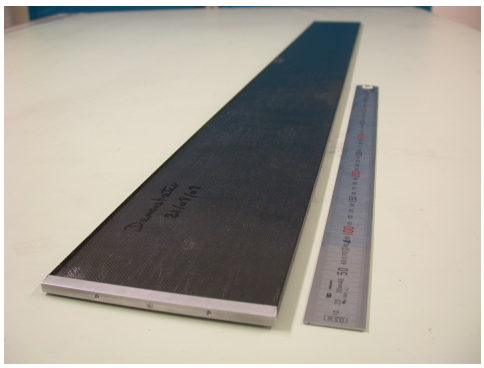

Figure 4: *H shaped board which carries the ASUs and embeds part of the absorber tungsten. The entity consisting of the H shaped board and the ASU lines is called a "slab".*

terminated by a so called *D*etector *I*nter*f*ace or *DIF* card and an adapter card. The DIF card constitutes the interface to the calorimeter data acquisition while the adapter card will host miscellaneous services like e,g, the power supply for the ASICs. The assembled layers will be mounted on both sides of the H shaped board shown in Figure 4.

2.2 Mechanical studies and realisations

The realisation of the mechanical items of the programme were subdivided into two phases. In a first step the mechanical concept was validated with a demonstrator which allowed also for an investigation of the thermal behaviour of the detector modules. After the validation phase, the construction of the actual alveolar structure started. Results obtained in these two phases are introduced in the following.

2.2.1 Mechanical demonstrator

The mechanical demonstrator has slightly smaller dimensions, $1300 \times 380 \times 70\,\mathrm{mm}^3$, than the technological prototype. It allowed, however, for the validation of the mechanical feasibility to built large modules by reusing existing material (i.e. the tungsten plates) from the physics prototype. The alveolar structure of the demonstrator is shown in Figure 5. From precise metrology, the planarity of the structure is given to be between 0.59 mm and 0.65 mm. In addition to the alveolar structure, a H shaped tungsten board dedicated to act as an absorber and to carry the ASUs has been built. For the demonstrator, this board was equipped with 9 cards allowing to study the thermal behaviour of a detector module.

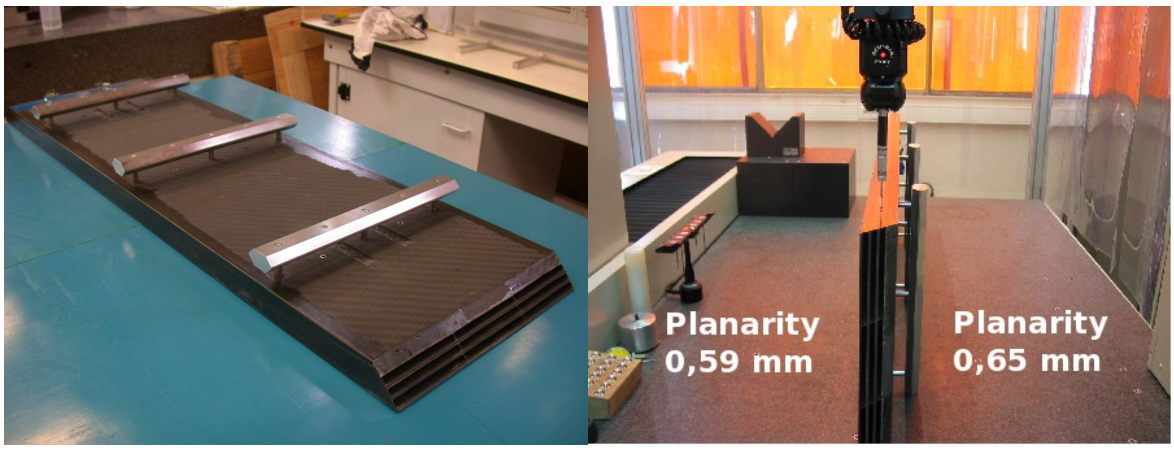

Figure 5: *Left: Alveolar structure as built for the demonstrator of the technological prototype. Right: The alveolar structure in the metrology at LAL. The numbers on both sides of the alveolar structure indicate the deviation from planarity of the structure.*

One of these cards is equipped with a steerable thermal resistor which simulates the heating ASICs. The resistor can be configured such that it dissipates 1 W at a local position which is to be compared to a total of 0.205 W expected to be generated by the ASICs along one layer. The other cards are equipped with thermometers which allow for the measurement of the temperature gradient along the layer. The extremities of the thermal slab are furnished with mock-ups of the DIF and the adaptor card which are also sources of heat. In accordance with the specifications of the TDR [5], resistors with a heat dissipation of 0.48 W for the adaptor card and more than 1.3 W for the DIF card were implemented on these cards. The interconnection between the various thermal cards was realised by heating up a tin-bismuth paste to 200^o C using a halogen lamp. The Figure 6 shows the clean interconnection between two individual cards and the complete chain of 9 interconnected boards. The technique for a proper interconnection is further developed in collaboration with industrial partners. This is made also with the perspective of a mass production needed for a full detector.
This chain of boards got finally wrapped into copper sheets supposed to evacuate the heat. Copper was used for its high heat conduction coefficient of $\lambda = 401\mathrm{W}/(\mathrm{m} \cdot \mathrm{K})$ [7]. The wrapped layer was inserted into the middle of the alveolar structure and subject to a dedicated thermal test. For this test, the other slots of the alveolar structure were also equipped with dummy slabs generating 1 W each. The Figure 7 shows the experimental setup of the thermal test. As can be seen from the figure, the thermal slab is connected to a cooling system. This cooling system consisted of copper blocks which were in turn connected to a water pipe. As it was realised, the cooling system is already very much oriented to the needs for an operation in the ILD detector. In a first step only the heating elements interior to the alveolar structure was powered. The temperature development along the thermal layer is shown in Figure 8. These and all subsequent temperatures are read off after the values have been observed to be stable for more than 30 minutes.

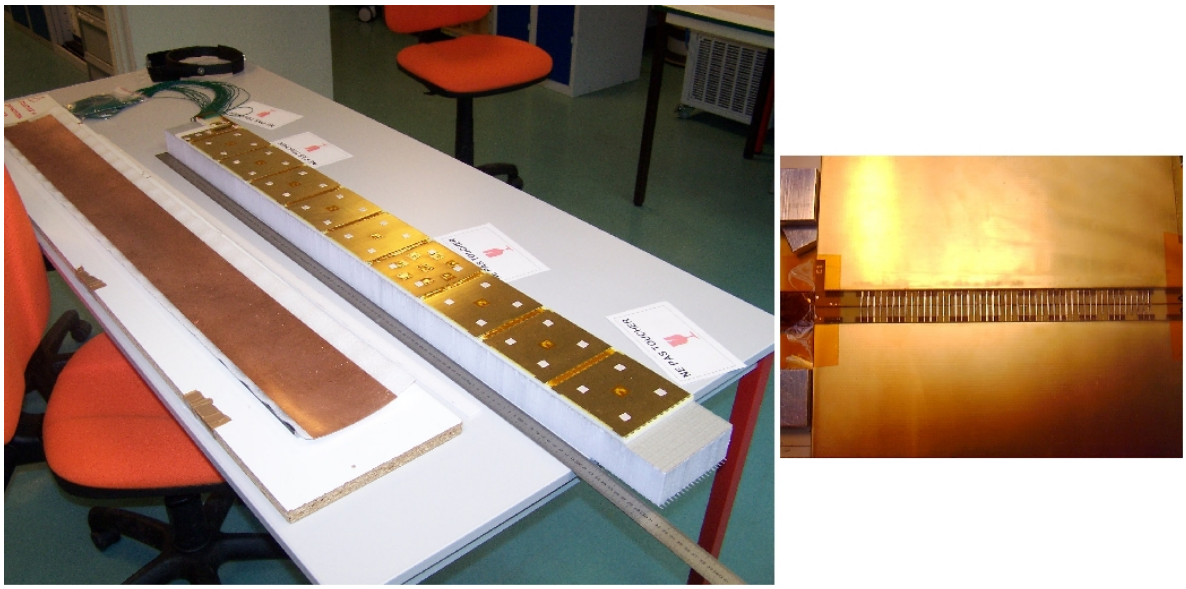

Figure 6: *Left: Thermal layer of 9 cards. The layer is wrapped into the copper foil visible to the left of the layer. Left: Interconnection between two thermal boards using the halogen lamp technique.*

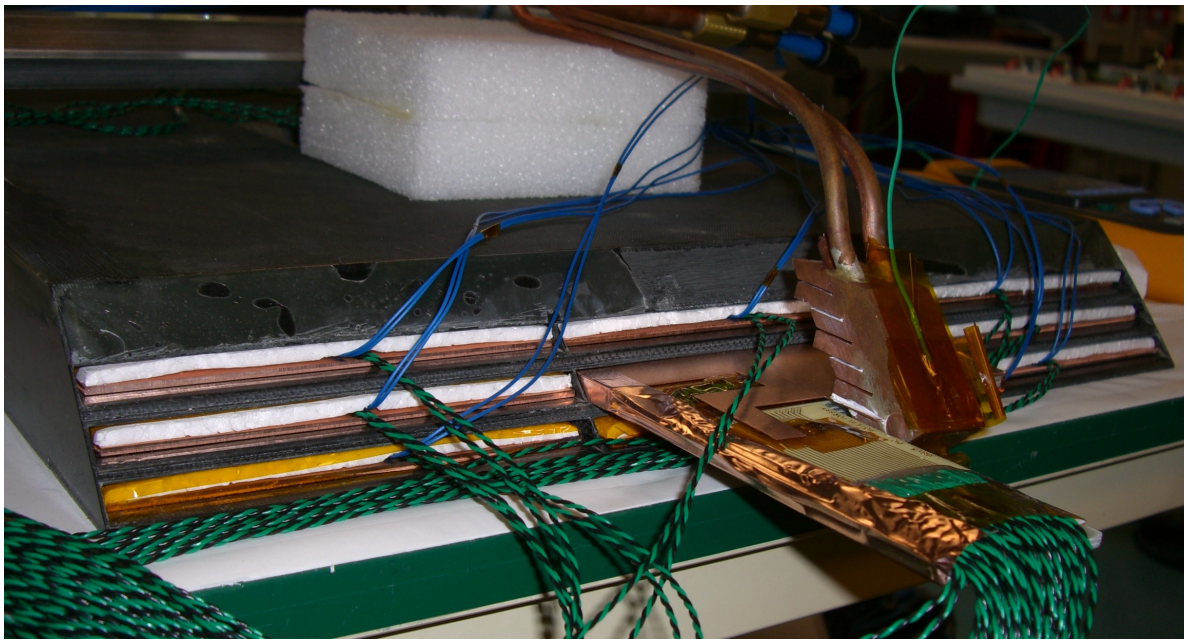

Figure 7: *Experimental setup of the thermal test with the demonstrator. The thermal layer has been inserted into the middle of the alveolar structure and is connected to a cooling system.*

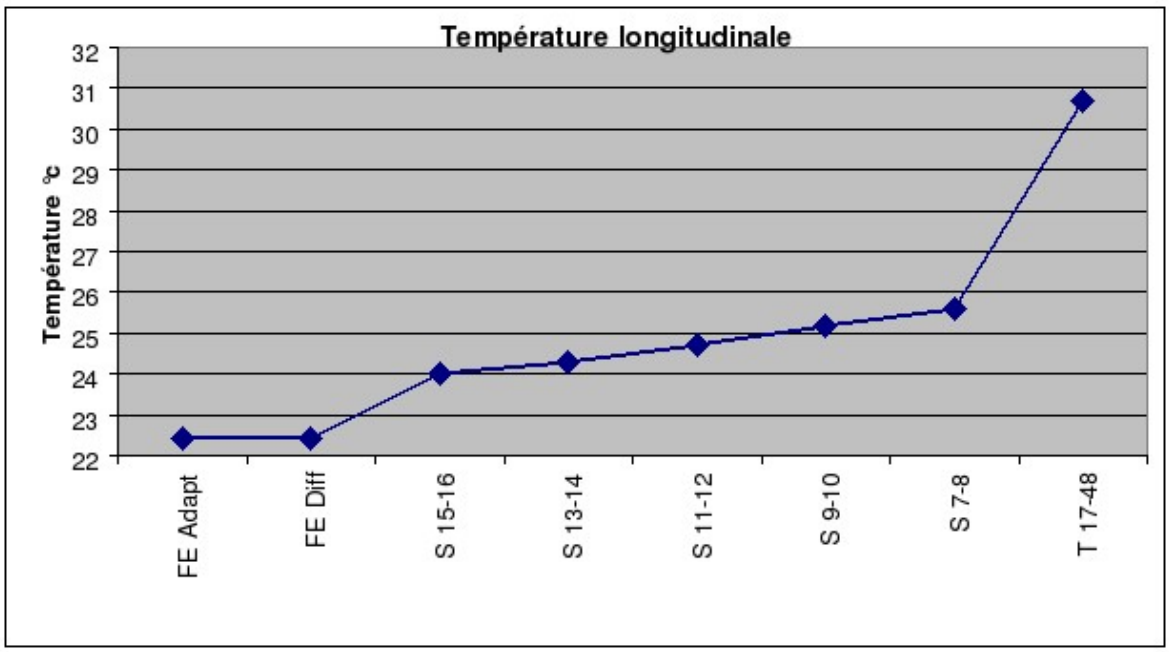

Figure 8: *Temperature development along the thermal layer upon powering the resistance located at point 17-48 with 1 W. The more left the points are, the closer they are to the cooling system.*

The temperature difference between the heated board and the outer extremity was measured to be of the order of 8^o C, the heat is partially transported by the copper layer as can be seen from temperature gradient as measured by the probes along the layer. The Table 2 shows the temperature measured in the surrounding layers as well as on top of the alveolar structure. The temperature on top of the structure was found to be 1.5^o C higher than the ambient temperature which indicates that the alveolar structure contributes significantly to the heat transfer.

Ambient Temperature	22		
Alveolar Slot	Left	Middle	Right
External		23.5	
Upper	24.8	24.8	24.6
Lower	25	30.7	25.2
Bottom	25.1	25.2	25.1

Table 2: *Temperatures in ^{o}C measured in the different alveolar slots when heating each layer with 1 W.*

The temperature gradient when powering the DIF and adaptor card is shown in Figure 9. As can be seen, the cooling system allows for maintaining these devices as temperatures of at maximum 55^o C. The thermal test with the demonstrator gave input to a simulation of the thermal behaviour of the EUDET module. Including a safety margin, it is assumed

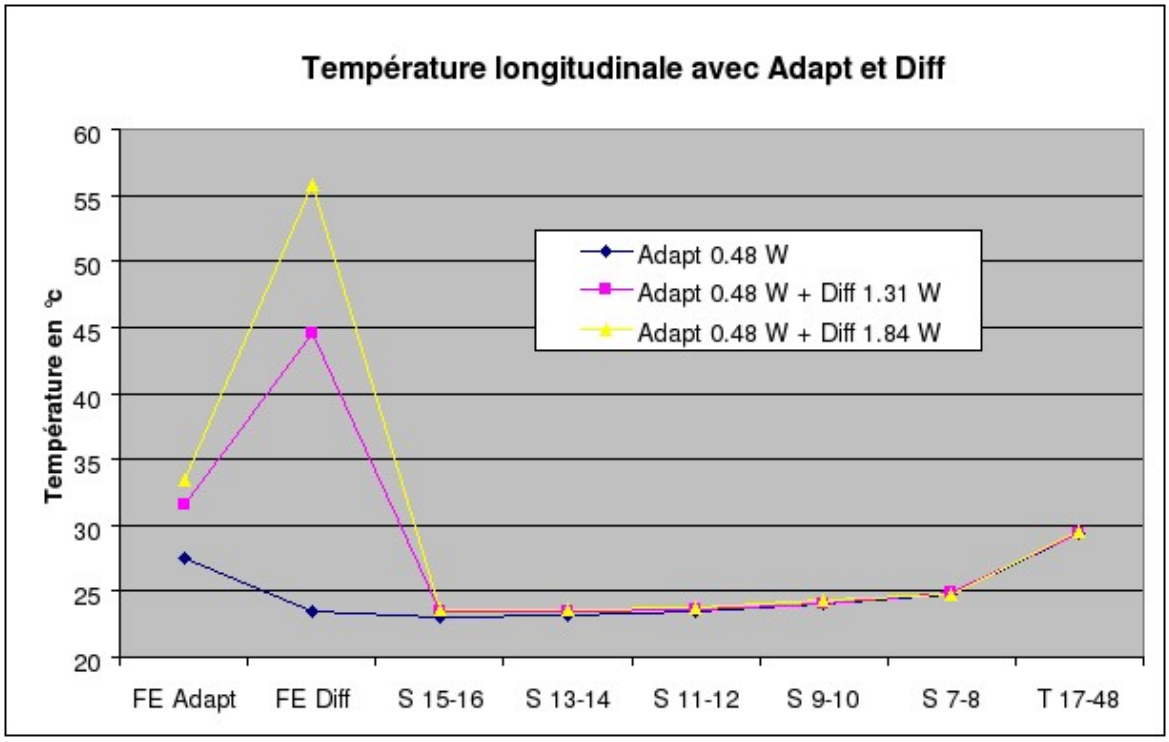

Figure 9: *Temperature development along the thermal layer upon powering the cards mimicking the DIF and adaptor cards. The more left the points are, the closer they are to the cooling system.*

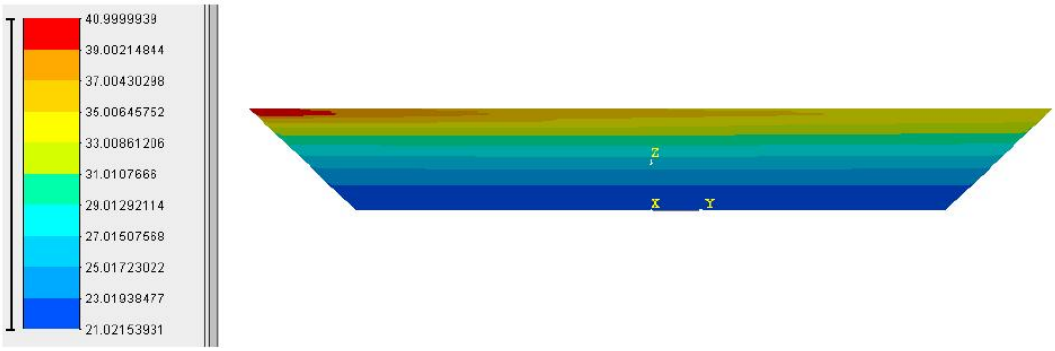

Figure 10: *Result of a simulation based on finite elements of the thermal behaviour of the EUDET Module under realistic conditions, i.e. ambient temperature of* 20^o C *and a cooling water temperature of* 18^o C.

that the long slab dissipates $20 \cdot 410$ mW, all short slabs dissipate together $20 \cdot 720$ mW while DIF and adaptor card dissipate 3 W and 1 W, respectively. The result of a finite element study which includes also natural convection is given in Figure 10.
For an ambient temperature of 20^o C and a cooling water temperature of 20^o C, the largest temperature is about 42^o C which is reached as expected close to the DIF and adaptor card. The temperature difference between this point and the other extremity of the slab is 7^o C. The cooling system for the EUDET Module which will look similar to that employed for the demonstrator will be dimensioned taking these results into account. Beyond the EUDET Module, the result will deliver important information on the thermal behaviour of the SiW Ecal modules in the final detector and its influence on other detectors. It will be included in the *Detail Base Line Design* of the ILD detector foreseen for 2012. In conclusion, it can be stated that the construction and the studies with the demonstrator have proved the mechanical feasibility to construct structures with dimensions as foreseen for an ILC detector. The mechanical concept for the SiW Ecal can therefore considered to be fully validated.

2.2.2 Alveolar structure for the EUDET Module

The validation with the demonstrator renders the step towards a full size structure less difficult. Indeed the production proceeds without major problems. The final structure will consist of 15 individual alveolar layers. All of these have been produced and are assembled to the final structure as shown in Figure 11. During the production process only one needed to be discarded. This proofs once again that the technique to produce the self-supporting alveolar structures is well under control. This is in turn is of vital importance for the validation of the mechanical concept of detectors for a future linear colliders. Finally it should be noted that Japanese groups which are developing an electromagnetic calorimeter base on scintillator as sensitive material will use this alveolar structure for their tests, too. This underlines the general applicability of the mechanical concept of the SiW Ecal.

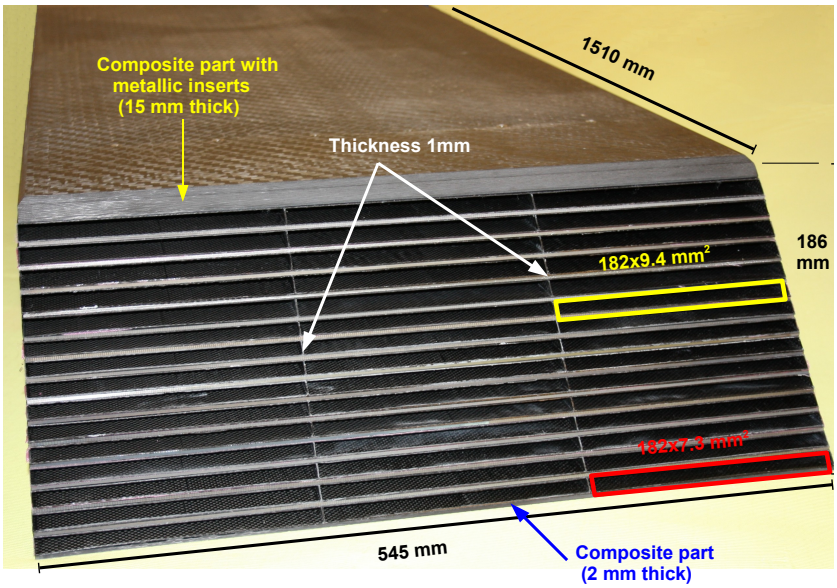

Figure 11: *Alveolar structure for the EUDET Module. Sizes and dimensions are those already shown in Figure 2 and are given here once more for convenience.*

2.3 R&D on silicon wafers

The sensitive part of an ASU of the technological prototype will consist of a matrix of 32×32 pixels distributed over 4 silicon wafers with a 16×16 segmentation. As can be seen in Figure 2 these wafers are supposed to have a thickness of only $325\,\mu$m. As the technological prototype should also constitute a first step towards industrialisation, a first batch of 40 wafers was purchased from Hamamatsu Photonics. These wafers were characterised in terms of the "usual" I-V and C-V curves to study their behaviour in terms of breakdown voltage and depletion region. All wafers show a breakdown at above 500 V. The Figure 12 shows a characterisation of a few wafers in terms of C-V. The start of the plateau shows that the wafers get saturated i.e. depleted at a voltage of around 80 V which is well away from the breakdown voltage of the wafers. The dark currents are found to be of the order 0.5μA. The yield of 100%, as obtained from the Hamamatsu Wafers, indicates that the technology to equip the SiW Ecal in an ILC detector is available.

During the operation of the physics prototype, events were observed which exhibit an unnatural square pattern of cells which carry a signal, see Figure 13. The R&D for the technological prototype addressed this issue, too. The reason for this square pattern could be traced back to a capacitive coupling between the guard ring and the pixels which induced charge into these pixels which is finally read out by VFE [8]. A remedy to suppress these square events is to segment the guard ring. It is hence decomposed into a series of capacitances which increases the effective impedance of the guard ring and thus suppresses the circulation of currents along the guard ring itself. The Figure 14 shows a picture of a segmented guard ring and the level of cross talk for different segmentations

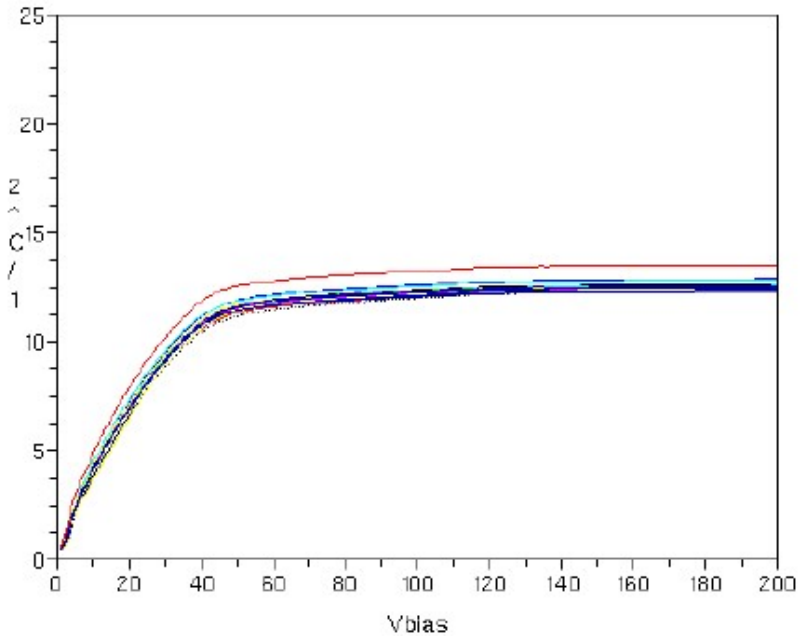

Figure 12: *Saturation curves of wafers which will be employed in the technological prototype.*

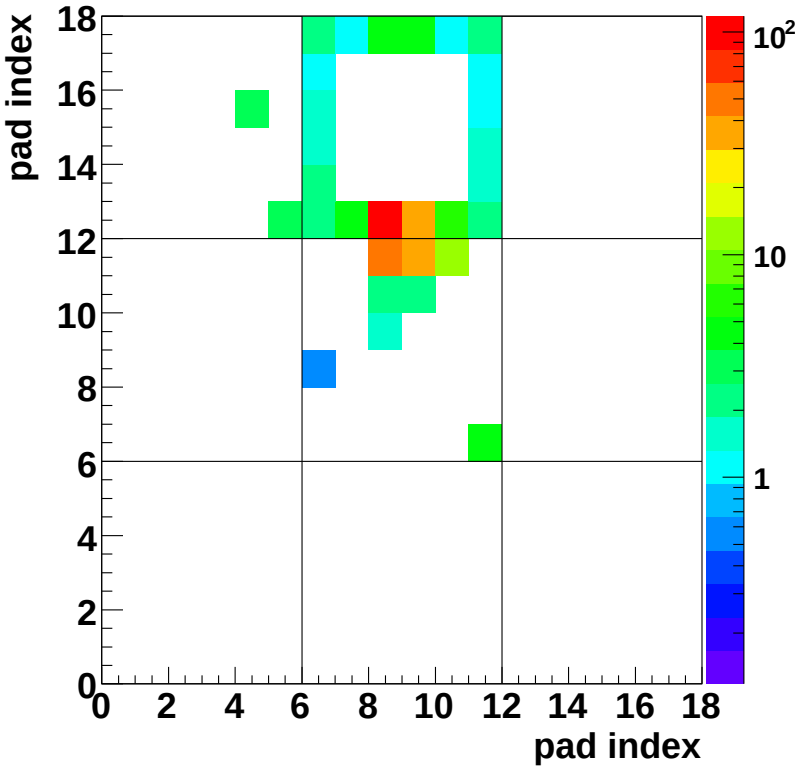

Figure 13: *Event with square pattern as observed in the physics prototype.*

of the guard ring. After segmentation the cross talk is attenuated by up to 80%. It can

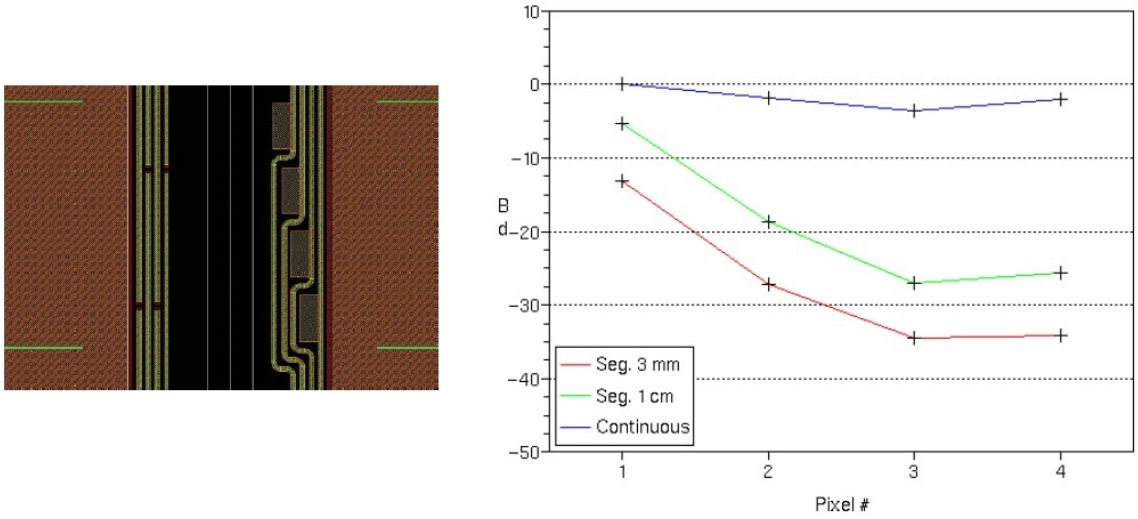

Figure 14: *Left: In its left part the photo shows a segmented guard ring. Right: The attenuation for different guard ring segmentation as observed in a test setup.*

be concluded that the origin of the square pattern is understood and can be taken into account in the future design of silicon wafers.
A major objective for the future R&D programme is to produce wafers at small price in order to reduce the cost since a surface as large as $3000\,\mathrm{m}^2$ will be needed for an ILC detector. On this contacts with major industrial partners are about to be forged. Among others the establishment of a co-operation with industry is supported within the *AIDA* project [9] within the FP7 programme on research infrastructure in Europe.

2.4 Front end electronics

The ASICs to be conceived for the EUDET Module and hence for the ILC detectors are very challenging. They integrate all of the following steps

- Pre-amplification of the charge deposited in the PIN Diode.
- Shaping of the signal.
- Digitisation and zero suppression on Chip.
- Output of a the digitised signal together with a time stamp equivalent to a bunch crossing ID.

The ASIC designed for the SiW Ecal is called *SKIROC*, which is short for *Silicon Kalorimeter Read Out Chip*. It is part of a group of ASICs conceived for the next generation of CALICE calorimeter prototypes such as an analogue hadron calorimeter [10] or a semi-digital hadron calorimeter [11, 12]. The building blocks are also employed in

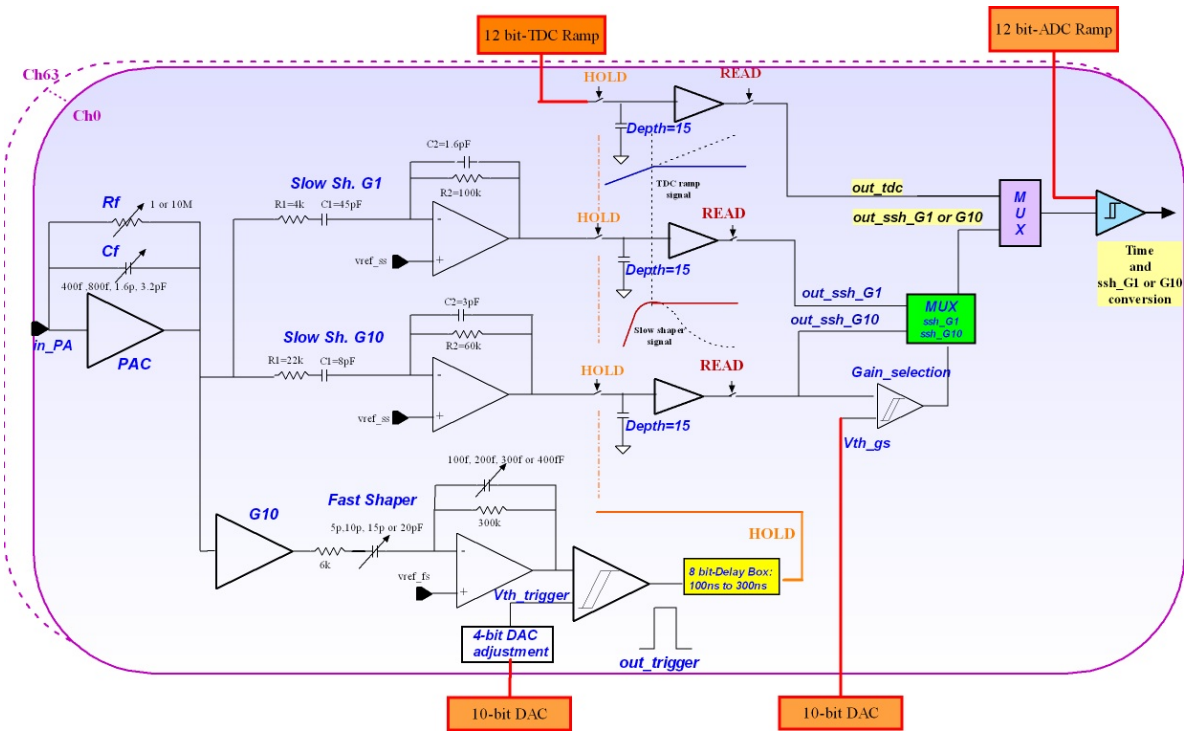

Figure 15: *Block channel diagram of one channel of the SKIROC chip. The input signal from a PIN Diode is processed from left to right.*

ASICs for application outside of particle physics. For a detailed overview see [13]. A block diagram of the SKIROC ASIC is shown in Figure 15. One ASIC is supposed to serve 64 cells with a dynamic range of 3000 MIPS for each of these cells. One of the key design issues for the ASIC is the quest for low power consumption. As outlined above, the requirement of compactness of the ILC detectors does not leave much space for service devices such as cooling. In fact as can be deferred from the basic design, parts interior to the alveolar structure practically do not benefit from any active cooling at all. Therefore, the ASICs have to be designed for ultra low power dissipation. The design value is 25 μW per channel. In order to achieve this small value, a novel technology called *power pulsing* will be applied. This technology exploits a distinct feature of the ILC beam structure. As explained above, the beam will arrive in bunch trains with a length of roughly 1 ms. Two bunch trains are mutually separated by about 199 ms. It is foreseen that the electronics will only be switched on during the one millisecond of a bunch train. For the other 200 ms the electronics will be switched off, apart from a short time after the bunch train dedicated for data acquisition. The described sequence is illustrated in Figure 16

This ASIC is conceived for the technological prototype of the analogue Hcal but shares a large number of functionality with SKIROC. The major difference is the dynamic range where SPIROC covers "only" 500 MIPS. In addition SPIROC can serve only 36 Channels. Due to the still large commonality, and in the current absence of a functional SKIROC,

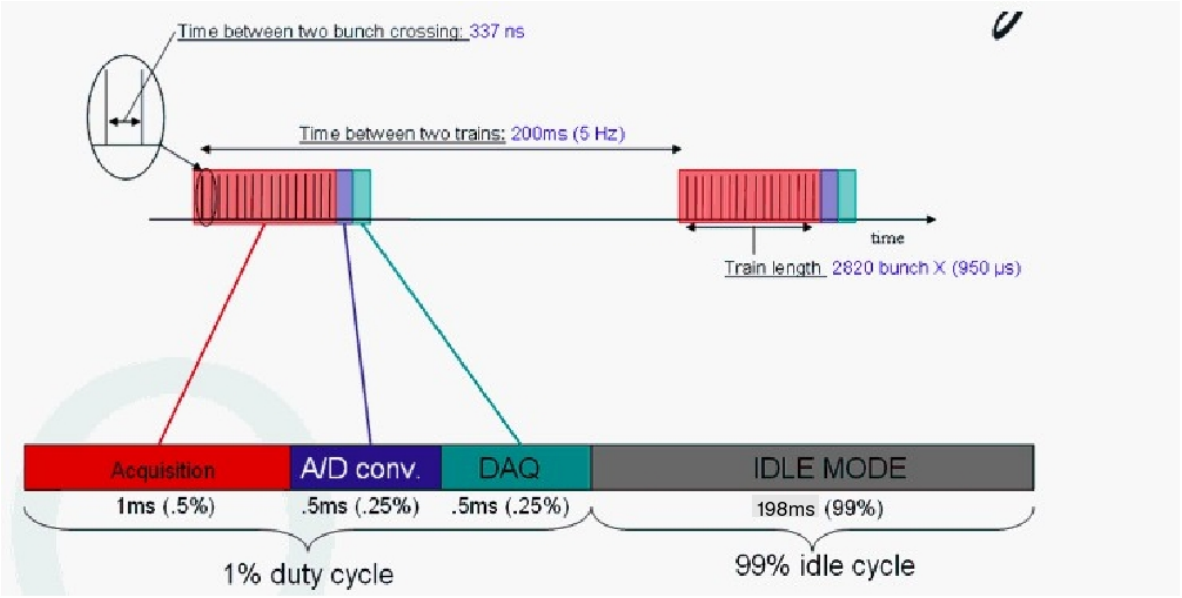

Figure 16: *Schematic illustration of the power pulsing in relation to the beam structure of the ILC beam. Apart from a short time at the beginning, the electronics will be switched off in between bunch trains.*

SPIROC was used for characterisation in terms of linearity and noise behaviour [13, 14]. The following results refer to measurements in non-power pulsed mode. As shown in Figure 17, the ADC of SPIROC is linear to ± 1 LSB over an input voltage range of about 1.2 V. At the same time, the noise level varies between 0.5 and 1 LSB. The Figure 18 shows in its left part, the residuals to the linearity fits of the individual channels and in its right part the difference between the mean of the individual channel and the mean of all channels. For the right part the means were measured at three different input voltages of 1.2,V, 2 V and 2.4 V, respectively. It is important to note that the difference remains constant independent of the input value. This shows that one can correct for this non-uniformity.

During the year 2010 around 1000 SKIROC ASICs have been produced within a dedicated production run for CALICE calorimeters. This is enough to equip the technological prototype. The ASICs are currently examined on test benches in the laboratory. Results are expected for spring 2011. Beyond the testing of the current SKIROC2 ASIC, the R&D continues with respect to a revision of the signal processing and in particular alternatives for the ADC. This work has partially already started within EUDET [15, 16]. The ASICs will be mounted onto a PCB. The PCB will be composed of eight layers which establish the connection between the silicon wafers the actual ASICs and the data acquisition system. According to the specification, the ensemble of ASIC and PCB must not be higher than 1.2 mm. It should be recalled at this point that one PCB has to serve 1024 individual cells and it is non trivial to build these dense boards. The current version of the board is called *FEV7* and serves only 36 channels. Its successor, *FEV8*, is currently conceived in collaboration with groups in South-Korea. Due to the

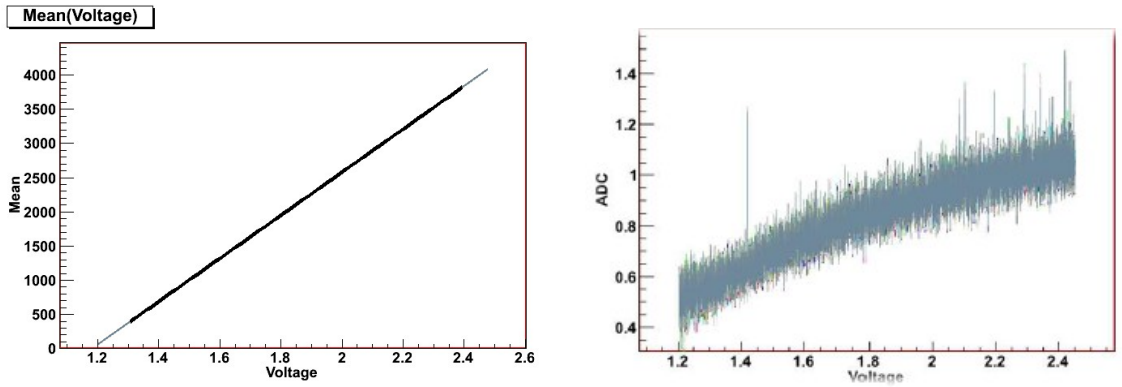

Figure 17: *Left: Linearity of the 36 Channels of the SPIROC ADC as a function of the input voltage. Right: Noise of the SPIROC ADC in ADC counts as a function of the input voltage.*

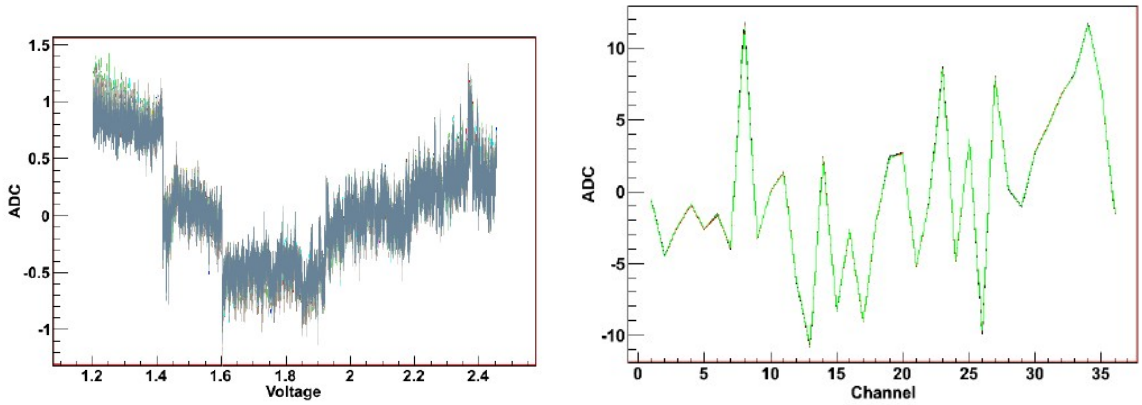

Figure 18: *Left: Residuals of the individual channels to the linear fit shown in Figure 17. Right: Deviation of the mean of an individual channel from the combined mean of all 36 channels measured for three different input voltages to the ADC. The input voltages are 1.2,V, 2 V and 2.4 V.*

tight space constraints, the ASICs cannot be packaged but have to be wire bonded onto the PCB. The Figure 19 shows a picture of four ASICs successfully bonded onto a thin PCB. The bonding was realised by the bonding lab at CERN. Right to that the Figure 20 shows a zoom into the area occupied by the ASICs. It should be noted that one of the major challenges to be solved in the near future is the planarity of the PCB. The bend on the board which might be caused by temperature coefficients of the material of the different layers deviates from exact planarity by about 2.5 mm. This is however still within industrial standards which allow for a deviation of 1% of the length of the diagonal of a board. This length is in case of the FEV boards $\sqrt{2} \cdot 18 \approx 25.5\,\text{cm}$. This issue is currently addressed in collaboration with industrial partners as well as by revising the entire assembly process of the detector.

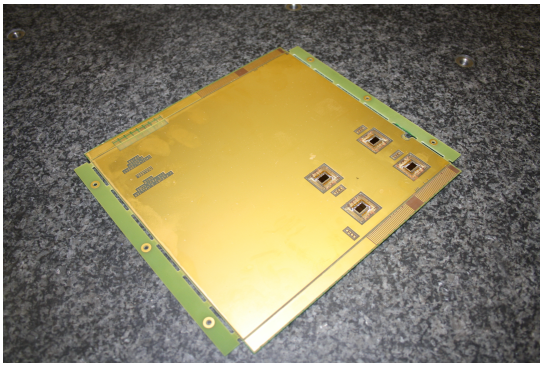

Figure 19: *PCB for the CALICE SiW electromagnetic calorimeter prototype with wire bonded readout ASICs.*

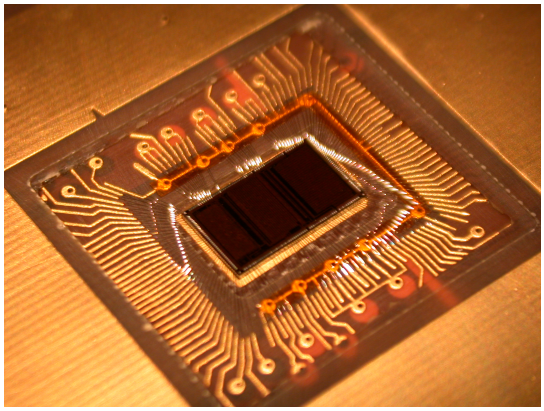

Figure 20: *Zoom into the zone occupied by the ASIC.*

The data acquisition, DAQ, which is based on custom made components in order to control cost and R&D effort for a DAQ at a future linear collider. For details on the DAQ please consult [17]. Being very generic, it can be applied to all technological prototypes currently under construction in the CALICE collaboration. Only the DIF card is customised to the actual detector type. The entire DAQ is currently going through its debugging phase before being employed in large scale beam test campaigns of CALICE calorimeter prototypes in the coming years. A first set-up containing prototype versions of the front end electronics and the DAQ system is shown in Figure 21.

3 Summary and outlook

The funding received within the EUDET programme permitted considerable progress with respect to the realisation of a technological prototype of a highly granular SiW electromagnetic calorimeter, EUDET Module, for a future linear electron positron collider. With the construction of the mechanical demonstrator and the thermal test, the mechanical concept of self-supporting absorber structures could be validated. The successful construction of the full sized structure renders of course the ultimate proof. In

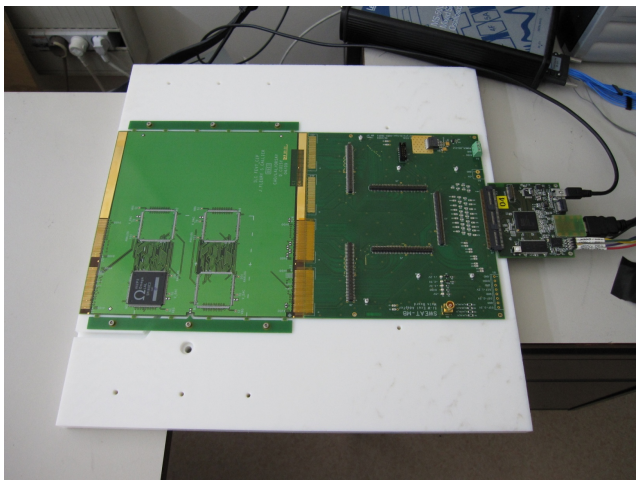

Figure 21: Early prototype of an ASU connected to the DAQ. The Detector Interface Card is the small board to the very right. Note that in contrast to Figures 19 and 20 the ASICs are still packaged

addition concepts for handling and assembly of the sensible components of the calorimeters could be developed and validated. The technology for the silicon wafers is at hand. Shortcomings observed during the operation of the physics prototype like square events could be remedied by dedicated modifications of the guard rings which surround the silicon wafers. The obtained experience allows for the start of collaborations with industrial partners in order to reduce the cost of these wafers in view of the construction of a full size electromagnetic calorimeter at a future linear collider. Good progress can be reported also on the realisation of the front end electronics comprised on the ASICs and the PCBs. Test bench results reveal the expected behaviour in terms of linearity and pedestal stability. However, the examination of the ASICs is continued in various laboratories of EUDET partners. An important aspect of this continuing R&D is the establishment of power pulsing as a viable technology for the operation of a calorimeter for a linear collider. The ASICs were successfully wire bonded onto a thin PCB. However, the planarity of the PCBs has to be improved. The PCBs are developed in collaboration with Korean groups which confirms the worldwide interest in this type of calorimeters and the challenging design. Another issue where industrial contact is fostered is the mastering of the interconnection technique
The EUDET module will be assembled during the year 2011. For this a dedicated assembly room will be fitted. This room will be equipped such that all tests necessary before going to beam tests can be conducted. Particularly, a cosmic test bench for a continuous monitoring of the detector response will be mounted. The entire R&D effort will naturally benefit from the continuing support with the AIDA programme.

Acknowledgement

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