

# Front end electronics for a TPC at future linear colliders \*

L. Jönsson

Lund University, Lund, Sweden

on behalf of the LCTPC collaboration

8.11.2010

#### Abstract

The actual status of the ALTRO readout electronics for the large protoype TPC is presented together with some results from recent measurements with three GEM-modules prepared by the Asian groups. Further, a description of a proposed MultiChip Module for the S-ALTRO electonics is given.

<sup>\*</sup>Talk given at the EUDET Annual Meeting, DESY, Germany, September 29 - October 1, 2010

### **1** Introduction

Tracking systems for experiments at future colliders, like ILC and CLIC, will need a momentum resolution that is a factor ten better than that obtained at LHC, in order to meet the next physics goals. Further an excellent two-track separation is required which allows for high resolution measurements of the jet energy using the particle-flow technique. A Time Projection Chamber (TPC) has shown very good performance in previous experiments and a lot of experience has been gained with such detectors by now. In order to meet the requirements given above it is necessary to take advantage of the recently developed micropattern avalanche chambers for the readout and have a pad size of few millimeters squared. The dimensions of the TPC will be about 4.3 meter long and 3.6 meter in diameter. The area of the end plate will thus be of the order of  $10 \text{ m}^2$  and thus will contain several million pads, which have to be read out by the front end electronics. This obvioulsy sets severe restrictions on the size and packing density of the electronics, which has to be compatible with the pad size. Present readout electronics have the analogue and digital circuits separated whereas for a future TPC they have to be integrated in a common chip in order to be consistent with the size requirements. Power consumption is another important issue which is connected to the need for power pulsing and efficient cooling.

The first step in the development of the front end electronics has been to demonstrate the proof of principle in connection with the micro pattern avalance chambers, GEM's [1] and MicroMegas [2].

### 2 The ALTRO electronics

The Lund and CERN groups have built a readout system for the large prototype TPC which is based on the ALTRO chip [3], originally developd for the ALICE experiment at the LHC. The 16 channel ALTRO chip performs analogue to digital conversion with 10 bit precision followed by various steps of digital signal processeing, including zero suppression and storage in an event buffer. The sampling can be clocked at frequences up to 40 MHz so in principle sampling at this frequency and frequencies lower by multiples of two is possible. However, at 40 MHz sampling the full resolution is not maintained for the standard ALTRO chip. A limited number of ALTRO chips were modified to allow sampling at 40 MHz with almost full precision [4]. Up to now the system has been operated during data taking at 20 MHz only. The ALTRO chip has an events storage memory of 1 k 10-bit words, which corresponds to sampled data over a depth of 50  $\mu$ s drift time at 20 MHz sampling frequency. The so called T2K gas mixture (95/3/2 % Ar/CF<sub>4</sub>/Isobutan) was used in the TPC, which gives a drift velocity of around 7 cm/ $\mu$ s at a drift field of 230 V/cm. This leads to a maximum drift length of 350 cm that can be accommodated in the ALTRO memory, which should be compared with the total length of the large prototype TPC of 60 cm.

In order to test recent technologies for gas amplification (GEM's and Micromegas for TPC readout) a new charge sensitive preamp-shaper has been developed. The programmable PCA16 [5] chip has, as the name indicates, 16 channels and offers different choices with respect to peaking time, gain, decay time and signal polarity. The new programmable analogue chip required modifications to the Front End Card, which mainly are related to the programmability of the chip. The programming of the PCA16 chip is done remotely and data for setting the parameter values are downloaded to the board controller FPGA on the FEC via the data bus on the back plane. An 8-bit shift register delivers the digital input to set the peaking time, the gain, the polarity and it also provides a possibility to bypass the shaping function. An octal DAC (Digital to Analogue Converter) controls the decay time of the output signal. The various options will make it possible to find the optimal parameter setting for a certain gas amplification system so that the specifications for the final chip production can be well defined.



Figure 1: The front end electronics and its support structure attached to the TPC. Also seen are the optical cables for the data readout and the LV supply cables.

Each FEC contains 128 channels i.e. 8 PCA16 chips and 8 ALTRO chips are mounted on each board. They are connected to the pad board via thin 30 cm long kapton cables. A Readout Control Unit (RCU) [6] governs the readout of the data via the backplane to which a maximum of 32 FEC's can be inserted. Data are sent via an optical cable to a Detector Read-Out Receiver Card (DRORC), which is placed in the Data Aquisition (DAQ) PC. The DAQ software uses the ALICE drivers and libraries for communication between the DRORC and the front end electronics via the optical link. Trigger and timing control is provided by a Trigger Logic Unit (TLU), which constitutes the central trigger unit for all sub-detectors in a beam set-up and includes an event synchronization mechanism by a distributed event sequence number. A distribution box (DBOX) receives the trigger from the TLU and sends it via the RCU to the FEC's. At the reception of the trigger the ALTRO starts storing digitized information in the event buffer, up to a predefined number of samples. The RCU reads the ALTRO event buffer and sends the data on the optical link to the DRORC, which stores it in a memory in the readout computer. The DBOX blocks the trigger system so that no new events are accepted during the whole readout cycle. At the arrival of a trigger in the DBOX, it defines a time stamp of the event that is used to synchronize it with events from other detectors. The run control is done from a graphical user interface. A monitor program creates and updates histograms in a shared memory, which is also accessible from a presenter program. A photograph of the test beam set-up is shown in Fig. 1.

The electronics pedestal and noise levels for all readout channels have been measured both initially as well as on a regular basis during data taking periods, mainly for pedestal subtraction and to check whether there are corrupt channels. The front end electronics has shown excellent noise performance. A typical measurement of one FEC with the PCA16 chip programmed to provide the longest peaking time (120 ns) and the lowest gain (12 mV/fC) is presented in Fig. 2. On the horizontal axis is given the number of the reaout channel from 0 to 127 plus N\*128, where N is the FEC-number, which is 22 in this case . The stars correspond to the ADC pedestal values, which can be read off on the left hand vertical scale, whereas the squares represent the RMS values of the pedestal measurement, which can be read off on the right hand vertical scale. The average RMS value of around 0.5 ADC counts



Figure 2: The pedestal and noise for the different channel numbers of a FEC. The stars are the mean value of the pedestal in ADC counts, corresponding to the left hand vertical scale, whereas the squares are the RMS of the pedestal measurement, related to the vertical scale on the right hand side

corresponds to the equivalent noise of 260 electrons, which includes random noise, coherent clock noise and long term variations on the scale of seconds. If the gain is increased to the highest value (27 mV/fC) the noise level increases to typcally about 1 ADC count, which corresponds to the equivalent noise of 231 electrons at this gain.

The ALTRO readout boards for a total of 10.000 channels have now been produced and tested. It was observed during a previous test run that one of the voltage regulator chips, which supplied the voltage for the original preamplifier chip (PASA) of the ALICE electronics was undersized to provide the correct operating voltage for the PCA16 chip and had to be exchanged. The performance of the front end electronics is temperature sensitive and the chips may be damaged if the temperature gets too high. To avoid this to happen and to register the board temperatures regularly, a system for monitoring the temperature has been developed and tested. A new and more efficient cooling system using compressed air has been built. Since up to 10.000 cahnnels of readout electronics has to be housed inside the TPC-magnet (PCMAG) [7] the option of water cooling was abandoned. The DAQ system has been further improved so that it now requires less manual actions and also includes automatic shut down in case of high temeratures on the chips. For the Low Voltage (LV) supply a commercial system from Delta Elektronika has been used. The low voltage distribution has been modified in order to improve the access to the front end boards.

For a test run in September 2010 three modules of GEM detectors were installed and about 7000 pads were equipped with the ALTRO readout electronics. The GEM modules had two layers of 100  $\mu m$  thick GEM layers. Such a module is shown in Fig. 3. The goals of the beam test were to measure position resolution and to perform momentum measurements of trajectories in the full volume of the TPC. The positioning of the superconducting solenoid (PCMAG) on a table that can be adjusted remotely allowed the magnet to be moved in the vertical direction, along its horizontal axis and also be rotated around the the vertical axis. This had the advantage that the TPC could be positioned in a region of the magnet where the magnetic field is the most homogenic and that the impact position of the beam could still cover the full volume of the TPC. The most important difference compared to



Figure 3: One of the GEM modules



Figure 4: Left: GEM event with one track in the 1 T B-field. Right: GEM event where the incoming electron hits the TPC catode, creating many low energy particles which curl in the B-field

previous measurements is that the drift length could be varied without suffering from large distorsion of the magnetic field, as a function of the drift distance, which was the case when the TPC was moved inside the magnet. From the first preliminar analysis of the data taken, we can for the first time present tracks which traverse the full radial distance of the TPC. Two events are presented in Fig. 4. Tracks were found by using the YokaRawMon program [8], which is based on a Kalman filter algorithm.

From this analysis the point resolution  $(\sigma_x)$  for various positions (z) over the fulldrift length were measured (Fig. 5 left) and a point resolution at zero drift distance of  $61.3 \pm 1.9 \ \mu m$  was extracted. The diffusion constant was determined by plotting the square of the pad resonse function  $(\sigma_{PR}^2)$  as a function of the drift distance (Fig. 5 right). Through the relation  $\sigma_{PR}^2(z) = \sigma_{PR}^2(0) + C_D^2 \cdot z$  the diffusion constant was calculated to be  $95.38 \pm 0.09 \ \mu m/\sqrt{cm}$ , which is compatible with the value of  $95.3 \pm 1.9 \ \mu m/\sqrt{cm}$ obtained from simulations with the Magboltz program. In addition the drift velocity was determined to be  $7.557 \pm 0.067 \ cm/\mu s$  in agreement with the Magboltz value of  $7.509 \pm 0.002 \ cm/\mu s$  calculated for a temperature of T = 290 K and pressure p = 1 bar with 200 ppm H<sub>2</sub>O.



Figure 5: Left: Position resolution as a function of drift distance. Right: The position resolution squared as a function of drift length from which the diffusion constant has been calculated

## 3 Multichip Modules for the S-ALTRO chip

In order to reach the goals of momentum resolution and two track separation for the TPC it seems necessary to have pads as small as 1x4 mm<sup>2</sup>. Thus the size of the front end electronics should not exceed this area per channel. The original plan was to mount the electronics directly onto the pad board using bump bonding to minimize the size. Preliminary studies have shown that a bump bonded 64 channel SALTRO64 chip will have a size of about 100 mm<sup>2</sup>, which means somewhat more than 1.5 mm<sup>2</sup> per channel. Including board controller, voltage regulators, optical readout and passive components it still seems feasible to meet the pad-requirement. However, the replacement of a malfunctioning chip is a difficult operation which will require advanced equipment and that the pad module is dismounted. The present prototype chip has 16 channels. Extending this to 64 channels is an expensive step and therefore all prototyping has to be made with the 16 channel version. The difficulties foreseen in the replacement of chips directly mounted on the pad module calls for alternative solutions. An interesting option, that is being investigated at the moment, would be to place the electronics on small separate boards which are connected to the pad module via micro-connectors. Since the electronics components can be mounted on both sides of such a board a first study with wire bonded SALTRO16 chips has shown that such a design is compatible with  $1x6 \text{ mm}^2$  pads, whereas the 64 channel SALTRO64 chip could be accommodated on a pad board with  $1x4 \text{ mm}^2$  pads. The pad size of  $1x6 \text{ mm}^2$  should be sufficiently small for the prototyping stage. The advantages in placing the electronics components on separate boards are listed below.

- trace routing from the pads to the SALTRO chip becomes simpler since translational routing will essentially only be necessary at the edges of the pad module.
- with fewer or no active electronics components on the pad board it will be easier to design.
- changes during the electronics prototyping will be cheaper and easier to implement and test.
- the interface between SALTRO-part and the controller/readout-part is well defined. Thus in the prototyping stage one can separate the analogue and digital functions on two boards.
- this offers good possibilities to divide responsibilities for design and production between different institutes.

the trace routing on the plug-in board will be easier compared to the trace routing in case all the electronics is placed on the pad board. The pad board will need less layers and thus becomes cheaper.
analogue and digital functions are well separated which makes it easier to optimize noise perfor-

• analogue and digital functions are well separated which makes it easier to optimize hoise performance.



Figure 6: The FEC-MCM accommodating eight SALTRO16 chips, two clock buffers and various passive components. Components in red are on the board surface facing the pad module and those in green are on the outside with respect to the pad module.

• it moves heat away from the TPC endplate.

• it facilitates service. A malfunction in the readout chain can easily be fixed by replacing the elecronics board instead of dismounting the whole pad board.

Fig. 6 shows a schematic draft of a Multi Chip Module (MCM), which accommodates eight SALTRO16 chips i.e. four on each side of the board, two buffer chips for the clock distribution and passive components. The dimensions of the board are 31.5 by 23.5 mm<sup>2</sup>, which is slightly smaller than the area covered by 32x4 pads of size 1x6 mm<sup>2</sup>. The board is connected to the pad module via four micro connectors, which elevate the boards by 4.3 mm above the pad module and therefore enable the mounting of components also on the surface facing to the pad board. The input connectors have 40 pins (32 for signals and 8 for ground) and a pin pitch of 0.4 mm. Two 60 pin connectors provide the connection to the board controller and the LV supply respectively, which are on separate boards perpendicular to the MCM in order to facilitate cooling.

In the case of the final 64 channel SALTRO64 chip a board with 8 chips seems to be optimal from a size point of view, since the buffer chips contain 8 channels each i.e. one per chip in this case. The dimensions of the chip itself have not been specified yet but for this study 12.5x 8 mm<sup>2</sup> has been chosen which is optimal to match the dimensions of the MCM. A schematic layout of such a board with wire bonded SALTRO64 chips is shown in Fig 7. In this design all the 8 SALTRO64 chips are placed on the surface facing to the pad plane together with the eight input connectors, having 80 pins each with 0.4 mm pin pitch. The rest of the electronics components are on the opposite side including the board controller, the buffer chips and the DAC. With this solution there is no need for additional insertion boards as in the case of the MCM design for the SALTRO16 chip. The dimensions of the board are 63.5 by 31.5 mm<sup>2</sup> which can be accommodated on an area covered by 64x8 pads of size 1x4 mm<sup>2</sup>. In case that the dimensions of the SALTRO64 chip will be different and/or the size will become bigger than 100 mm<sup>2</sup>, this can still be accommodated on the MCM if the SALTRO64 chips are mounted



Figure 7: The FEC-MCM accommodating eight SALTRO64 chips, clock buffers and various passive components. Components in red are on the board surface facing the pad module and those in green are on the outside with respect to the pad module.

on both sides and an additional plug-in card for the board controlling functions is introduced as in the case of the prototype MCM with the SALTRO16 chip. The connectors in the centre of the board indicate the space available for plug-in cards and the LV supply.

#### References

- [1] F. Sauli, Nucl. Instrum. Meth. A386 (1997) 531.
- [2] Y. Giomataris, Nucl. Instrum. Meth. A376 (1996) 29.
- [3] L. Musa et al., The ALICE TPC Front End Electronics, Proc. of the IEEE Nuclear Science Symposium, 20 - 25 Oct 2003, Portland.
- [4] R. Esteve Bosch, A. Jimenez de Parga, B. Mota and L. Musa, IEEE Transaction on Nuclear Science, Vol. 50 N. 6, December 2003.
- [5] L. Musa, Prototype compact readout system, EUDET-Memo 2009-31, 2009.
- [6] C. Gonzales Gutrierrez et al., The ALICE TPC Readout Control Unit, Proceeding of the 2005 IEEE Nuclear Science Symposium and Medical Imaging Conference. Puerto Rico, October 23 -29, 2005.
- [7] A. Yamamoto and Y. Makida, "Superconducting magnet for long duration flights", Proceedings of the 5th Workshop on "Ballon-borne experiment with a superconducting magnet spectrometer", KEK Japan, Nov. 30 - Dec 1, 1994.
- [8] K. Fujii, private communication.